UC1843B-SP QML Class V, Radiation Hardened Current-Mode PWM Controller

1 Features

- QML class V (QMLV) qualified, SMD 5962-86704
- 5962R8670412VYC:
  - Radiation hardness assurance (RHA) up to 100-krad(Si) total ionizing dose (TID)
- Optimized for offline and DC-to-DC converters
- Low start-up current (< 0.5 mA)
- Trimmed oscillator discharge current
- Automatic feed forward compensation
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Undervoltage lockout (UVLO) with hysteresis
- Double-pulse suppression
- High-current totem-pole output
- Internally-trimmed bandgap reference
- 500-kHz operation
- Low $R_O$ error amplifier

2 Applications

- DC-DC converters
- Supports various topologies:
  - Flyback, forward buck, boost
  - Push-pull, half-bridge, full-bridge with external interface circuit
- Available in military temperature range (–55°C to 125°C)

3 Description

The UC1843B-SP control IC is a radiation hardened pin-for-pin compatible version of the UC1843A-SP. Providing the necessary characteristics to control current-mode switched-mode power supplies, this device has improved features. Start-up current is specified to be less than 0.5 mA and oscillator discharge is trimmed to 8.3 mA. During UVLO, the output stage can sink at least 10 mA at less than 1.2 V for $V_{CC}$ over 5 V.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UC1843B-SP</td>
<td>CFP/HKU (10)</td>
<td>6.48 mm × 7.02 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2019) to Revision A Page

• Changed the package image in the Pin Configuration and Functions ......................... 3
• Changed <10 mA To: <17 mA in Figure 6 ........................................................................ 10
5 Pin Configuration and Functions

HKU Package
10-Pin CFP
Top View

<table>
<thead>
<tr>
<th>PIN Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN</td>
</tr>
<tr>
<td>---</td>
</tr>
<tr>
<td>Comp</td>
</tr>
<tr>
<td>VFB</td>
</tr>
<tr>
<td>ISENSE</td>
</tr>
<tr>
<td>RT/CT</td>
</tr>
<tr>
<td>NC</td>
</tr>
<tr>
<td>Gnd</td>
</tr>
<tr>
<td>Output</td>
</tr>
<tr>
<td>VCC</td>
</tr>
<tr>
<td>VREF</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>30</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_I$</td>
<td>-0.3</td>
<td>6.3</td>
<td>V</td>
</tr>
<tr>
<td>$I_O$</td>
<td>±1</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>$P_D$</td>
<td>1</td>
<td>W</td>
<td></td>
</tr>
<tr>
<td>$T_{lead}$</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground. Currents are positive in, negative out of the specified terminal.

(3) Current limiting this input will allow for higher supply voltages.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(ESD)}$</td>
<td>±4000</td>
<td>V</td>
</tr>
<tr>
<td>$V_{(ESD)}$</td>
<td>±1000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>12</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>$I_O$</td>
<td>0</td>
<td>200</td>
<td>mA</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>0</td>
<td>200</td>
<td>mA</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>UC1843B-SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>HKU (CFP)</td>
<td>UNIT</td>
</tr>
<tr>
<td>10 PINS</td>
<td></td>
</tr>
<tr>
<td>$R_{UA}$</td>
<td>51.9</td>
</tr>
<tr>
<td>$R_{UJC(bot)}$</td>
<td>6.6</td>
</tr>
<tr>
<td>$R_{UJ}$</td>
<td>31.5</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>5.42</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>31</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
6.5 Electrical Characteristics

$V_{CC} = 15 \, V^{(1)}$, $R_T = 10 \, k\Omega$, $C_T = 3.3 \, nF$, $T_A = T_J = -55^\circ C$ to $125^\circ C$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>REFERENCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage</td>
<td>$T_J = 25^\circ C$, $I_O = 1 , mA$</td>
<td>4.85</td>
<td>5</td>
<td>5.1</td>
<td>V</td>
</tr>
<tr>
<td>Line regulation</td>
<td>$V_IN = 12$ to $25 , V$</td>
<td>6</td>
<td>20</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Load regulation</td>
<td>$I_O = 1$ to $20 , mA$</td>
<td>6</td>
<td>25</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Temperature stability$^{(2)(3)}$</td>
<td></td>
<td>0.2</td>
<td>0.4</td>
<td></td>
<td>mV/$^\circ C$</td>
</tr>
<tr>
<td>Total output variation$^{(2)}$</td>
<td>Over line, load, and temperature</td>
<td>4.85</td>
<td>5.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output noise voltage</td>
<td>$10 , Hz \leq f \leq 10 , kHz$, $T_J = 25^\circ C$</td>
<td>50</td>
<td></td>
<td></td>
<td>$\mu V$</td>
</tr>
<tr>
<td>Long-term stability</td>
<td>1000 hours, $T_A = 125^\circ C^{(2)}$</td>
<td>5</td>
<td>25</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Short-circuit output current</td>
<td></td>
<td>$-30$</td>
<td>$-100$</td>
<td>$-180$</td>
<td>mA</td>
</tr>
<tr>
<td><strong>OSCILLATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Initial accuracy</td>
<td>$T_J = 25^\circ C^{(4)}$</td>
<td>47</td>
<td>52</td>
<td>57</td>
<td>kHz</td>
</tr>
<tr>
<td>Voltage stability</td>
<td>$V_{CC} = 12$ to $25 , V$</td>
<td>0.2%</td>
<td>1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature stability</td>
<td>$T_J = -55^\circ C$ to $125^\circ C^{(2)}$</td>
<td>5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Amplitude peak-to-peak</td>
<td>V pin 4$^{(2)}$</td>
<td>1.7</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Discharge current</td>
<td>V pin 4 = 2 V$^{(5)}$</td>
<td>$T_J = 25^\circ C$</td>
<td>7.8</td>
<td>8.3</td>
<td>8.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_J = \text{Full range}$</td>
<td>7.5</td>
<td>8.8</td>
<td></td>
</tr>
<tr>
<td><strong>ERROR AMPLIFIER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input voltage</td>
<td>$V_{Comp} = 2.5 , V$</td>
<td>2.45</td>
<td>2.50</td>
<td>2.55</td>
<td>V</td>
</tr>
<tr>
<td>Input bias current</td>
<td></td>
<td>$-0.3$</td>
<td>$-1$</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>Open-loop voltage gain</td>
<td>$V_O = 2$ to $4 , V$</td>
<td>65</td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Unity-gain bandwidth</td>
<td>$T_J = 25^\circ C^{(2)}$</td>
<td>0.7</td>
<td>1</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>PSRR</td>
<td>$V_{CC} = 12$ to $25 , V$</td>
<td>60</td>
<td>70</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output sink current</td>
<td>$V_{FB} = 2.7 , V$, $V_{Comp} = 1.1 , V$</td>
<td>2</td>
<td>6</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Output source current</td>
<td>$V_{FB} = 2.3 , V$, $V_{Comp} = 5 , V$</td>
<td>$-0.5$</td>
<td>$-0.8$</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>High-level output voltage</td>
<td>$V_{FB} = 2.3 , V$, $R_L = 15 , k\Omega$ to ground</td>
<td>5</td>
<td>6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low-level output voltage</td>
<td>$V_{FB} = 2.7 , V$, $R_L = 15 , k\Omega$ to $V_{REF}$</td>
<td>0.7</td>
<td>1.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>CURRENT SENSE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain$^{(6)(7)}$</td>
<td></td>
<td>2.85</td>
<td>3</td>
<td>3.15</td>
<td>V/V</td>
</tr>
<tr>
<td>Maximum input signal</td>
<td>$V_{Comp} = 5 , V^{(6)}$</td>
<td>0.9</td>
<td>1.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>PSRR</td>
<td>$V_{CC} = 12$ to $25 , V^{(6)}$</td>
<td>70</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input bias current</td>
<td></td>
<td>$-2$</td>
<td>$-10$</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>Delay to output</td>
<td>$V_{ISENSE} = 0$ to $2 , V^{(2)}$</td>
<td>150</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) Adjust $V_{CC}$ above the start threshold before setting at $15 \, V$.
(2) Parameters ensured by design and/or characterization, if not production tested.
(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temperature Stability} = \frac{V_{REF}^{\text{max}} - V_{REF}^{\text{min}}}{T_{J}^{\text{max}} - T_{J}^{\text{min}}},$$

where $V_{REF}^{\text{max}}$ and $V_{REF}^{\text{min}}$ are the maximum and minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(4) Output frequency equals oscillator frequency.
(5) This parameter is measured with $R_T = 10 \, k\Omega$ to $V_{REF}$. This contributes approximately 300 $\mu A$ of current to the measurement. The total current flowing into the $R_T$ or $C_T$ pin will be approximately 300 $\mu A$ higher than the measured value.
(6) Parameter measured at trip point of latch with $V_{FB} = 0 \, V$.
(7) Gain defined as: $G = \Delta V_{Comp} / \Delta V_{ISENSE}$; $V_{ISENSE} = 0$ to $0.8 \, V$. 
Electrical Characteristics (continued)

\(V_{CC} = 15\ V^{(1)},\ R_T = 10\ k\Omega,\ C_T = 3.3\ nF,\ T_A = T_J = -55^\circ\text{C} \text{ to } 125^\circ\text{C} (\text{unless otherwise noted})\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output low-level voltage</td>
<td>(I_{\text{SINK}} = 20\ mA)</td>
<td>0.1</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(I_{\text{SINK}} = 200\ mA)</td>
<td>1.5</td>
<td>2.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output high-level voltage</td>
<td>(I_{\text{SOURCE}} = -20\ mA)</td>
<td>13</td>
<td>13.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(I_{\text{SOURCE}} = -200\ mA)</td>
<td>12</td>
<td>13.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Rise time</td>
<td>(C_L = 1\ nF,\ T_J = 25^\circ\text{C}^{(2)})</td>
<td>50</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Fall time</td>
<td>(C_L = 1\ nF,\ T_J = 25^\circ\text{C}^{(2)})</td>
<td>50</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>UVLO saturation</td>
<td>(V_{CC} = 5\ V,\ I_{\text{SINK}} = 10\ mA)</td>
<td>0.7</td>
<td>1.2</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

UNDERVOLTAGE LOCKOUT

<table>
<thead>
<tr>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start threshold</td>
<td>7.8</td>
<td>8.4</td>
<td>9</td>
<td>V</td>
</tr>
<tr>
<td>Minimum operation voltage after turnon</td>
<td>7</td>
<td>7.6</td>
<td>8.2</td>
<td>V</td>
</tr>
</tbody>
</table>

PWM

<table>
<thead>
<tr>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum duty cycle</td>
<td>94%</td>
<td>96%</td>
<td>100%</td>
<td></td>
</tr>
<tr>
<td>Minimum duty cycle</td>
<td></td>
<td></td>
<td>0%</td>
<td></td>
</tr>
</tbody>
</table>

TOTAL STANDBY CURRENT

<table>
<thead>
<tr>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start-up current</td>
<td></td>
<td></td>
<td>0.3</td>
<td>mA</td>
</tr>
<tr>
<td>Operating supply current</td>
<td>(V_{FB} = V_{\text{SENSE}} = 0\ V)</td>
<td>11</td>
<td>17</td>
<td>mA</td>
</tr>
<tr>
<td>(V_{CC}) Zener voltage</td>
<td>(I_{\text{CC}} = 25\ mA)</td>
<td>30</td>
<td>34</td>
<td>V</td>
</tr>
</tbody>
</table>

6.6 Typical Characteristics

![Figure 1. Output Saturation Characteristics](image-url)
7 Detailed Description

7.1 Overview
The UC1843B-SP control IC is a pin-for-pin compatible improved version of the UC1843A-SP. Providing the necessary characteristics to control current-mode switched-mode power supplies, this device has improved features. Start-up current is specified to be less than 0.5 mA and oscillator discharge is trimmed to 8.3 mA. During UVLO, the output stage can sink at least 10 mA at less than 1.2 V for $V_{CC}$ over 5 V.

7.2 Functional Block Diagram

7.3 Feature Description
UC1843B-SP is a current mode controller, used to support various topologies such as forward, flyback, buck, and boost. Using an external interface circuit will also support half-bridge, full-bridge, and push-pull configurations.

Figure 2 shows the two-loop current-mode control system. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way, the error signal actually controls peak inductor current. This contrasts with voltage control in which the error signal directly controls pulse width without regard to inductor current.

Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; that is, the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier’s dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.
Feature Description (continued)

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the purposes of small signal analysis (see Figure 3). The two pole control to output frequency response of these converters is reduced to a single-pole (filter capacitor in parallel with load) response. One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gain bandwidth than would be possible with pulse-width control, giving the supply improved small signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler, as shown in Figure 4.

Capacitor $C_i$ and resistor $R_i$, in Figure 4(A), add a low frequency zero, which cancels one of the two control to output poles of non-current mode converters. For large signal load changes, in which converter response is limited by inductor slew rate, the error amplifier saturates while the inductor is catching up with the load. During this time, $C_i$ charges to an abnormal level. When the inductor current reaches its required level, the voltage on $C_i$ causes a corresponding error in supply output voltage. The recovery time is $R_iC_i$, which may be long. However, the compensation network of Figure 4(B) can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of $C_i$.

Current limiting is greatly simplified with current mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

![Two-Loop Current-Mode Control System](image-url)
Feature Description (continued)

Figure 3. Inductor Looks Like a Current Source to Small Signals

A. Direct duty cycle control
B. Current mode control

Figure 4. Required Error Amplifier Compensation for Continuous Inductor Current Designs

7.3.1 UVLO

The UVLO circuit ensures that \( V_{CC} \) is adequate to make the UC1843B-SP fully operational before enabling the output stage. Figure 5 shows that the UVLO turnon and turnoff thresholds are fixed internally at 8.4 V and 7.6 V, respectively. The 0.6-V hysteresis prevents \( V_{CC} \) oscillations during power sequencing.

Figure 6 shows supply current requirements. Start-up current is < 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as shown in Figure 7. During normal circuit operation, \( V_{CC} \) is developed from auxiliary winding, \( W_{Aux} \), with \( D_1 \) and \( C_{IN} \). However, at start-up, \( C_{IN} \) must be charged to 8.4 V through \( R_{IN} \). With a start-up current of 1 mA, \( R_{IN} \) can be as large as 100 k\( \Omega \) and still charge \( C_{IN} \) when \( V_{AC} = 90 \text{-V RMS (low line)} \). Power dissipation in \( R_{IN} \) would then be less than 350 mW even under high line (\( V_{AC} = 130 \text{-V RMS} \)) conditions.

During UVLO, the output driver is in a low state. While it does not exhibit the same saturation characteristics as normal operation, it can easily sink 1 mA, enough to ensure the MOSFET is held off. For efficient operations, an LDO can take the place of \( R_{IN} \) and be disabled during the operation of the device.
Feature Description (continued)

![Figure 5. UVLO Turnon and Turnoff Threshold](image1)

NOTE: During UVLO, the output driver is biased to sink minor amounts of current.

![Figure 6. Supply Current Requirements](image2)

Figure 6. Supply Current Requirements

![Figure 7. Providing Power to the UC1843B-SP](image3)

Figure 7. Providing Power to the UC1843B-SP
Feature Description (continued)

7.3.2 Reference
As highlighted in the Functional Block Diagram, UC1843B-SP incorporates a 5-V internal reference regulator with ±2% set point variation over temperature.

7.3.3 Totem-Pole Output
The UC1843B-SP PWM has a single totem-pole output which can be operated to ±1-A peak for driving MOSFET gates, and a 200-mA average current for bipolar power U-100A transistors. Cross conduction between the output transistors is minimal, the average added power with \( V_{\text{IN}} = 30 \text{ V} \) is only 80 mW at 200 kHz.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage \( V_C \) by the peak current rating of the IC’s totem-pole. Without this resistor, the peak current is limited only by the \( \text{dV/dT} \) rate of the totem-pole switching and the FET gate capacitance. Adding resistance will increase the switching losses of the converter, but will often reducing ringing and switching noise.

The use of a Schottky diode from the PWM output to ground prevents the output voltage from going excessively below ground, causing instabilities within the IC. To be effective, the diode selected should have a forward drop of less than 0.3 V at 200 mA. Most 1- to 3-A Schottky diodes exhibit these traits above room temperature. Placing the diode as physically close to the PWM as possible enhances circuit performance. Implementation of the complete drive scheme is shown in Figure 8 through Figure 10. Transformer-driven circuits also require the use of the Schottky diodes to prevent a similar set of circumstances from occurring on the PWM output. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Figure 8 through Figure 10 show suggested circuits for driving MOSFETs and bipolar transistors with the UC1843B-SP output. The simple circuit of Figure 8 can be used when the control IC is not electrically isolated from the MOSFET turnon and turnoff to ±1 A. It also provides damping for a parasitic tank circuit formed by the FET input capacitance and series wiring inductance. Schottky diode, \( D_1 \), prevents the output of the IC from going far below ground during turnoff.

Figure 9 shows an isolated MOSFET drive circuit which is appropriate when the drive signal must be level shifted or transmitted across an isolation boundary. Bipolar transistors can be driven efficiently with the circuit of Figure 10. Resistors \( R_1 \) and \( R_2 \) fix the on-state base current while capacitor \( C_1 \) provides a negative base current pulse to remove stored charge at turnoff.

Because the UC1843B-SP series has only a single output, an interface circuit is needed to control push-pull, half-bridge, or full-bridge topologies. The UC1706 dual output driver with internal toggle flip-flop performs this function. The Typical Application section shows a typical application for these two ICs. Increased drive capability for driving numerous FETs in parallel, or other loads can be accomplished using one of the UC1705/7-SP driver ICs.
Feature Description (continued)

Figure 8. Direct MOSFET Drive

Figure 9. Isolated MOSFET Drive
7.4 Device Functional Modes

The UC1843B-SP uses fixed frequency, peak current mode control. An internal oscillator initiates the turnon of the driver to high-side power switch. The external power switch current is sensed through an external resistor and is compared via internal comparator. The voltage generated at the COMP pin is stepped down via internal resistors (as shown in the Functional Block Diagram). When the sensed current reaches the stepped down COMP voltage, the high-side power switch is turned off.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
UC1843B-SP can be used as a controller to design various topologies such as buck, boost, flyback, and forward. Using an external interphase circuit can also support push-pull, half-bridge, and full-bridge topologies.

8.2 Typical Application

Figure 11. Typical Application Schematic

8.2.1 Design Requirements
See Table 1 for parameter values.

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATIONS</th>
</tr>
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<tbody>
<tr>
<td>Input Power Supply</td>
<td>20 to 40 VDC</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>5 VDC</td>
</tr>
<tr>
<td>Output Current</td>
<td>0 to 10 A</td>
</tr>
<tr>
<td>Output Current Pre-load</td>
<td>100 mA</td>
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<tr>
<td>Operating Temperature</td>
<td>25°C</td>
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<td>Switching Frequency of UC1843B-SP</td>
<td>200 kHz</td>
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<tr>
<td>Peak Input Current Limit</td>
<td>12 A</td>
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<tr>
<td>Bandwidth</td>
<td>~4 kHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>~80°</td>
</tr>
</tbody>
</table>
8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency

Choosing a switching frequency has a trade off between efficiency and bandwidth. Higher switching frequencies will have larger bandwidth, but a lower efficiency than lower switching frequencies. A switching frequency of 200 kHz was chosen as a trade off between bandwidth and efficiency. Using Equation 1, \( R_T \) and \( C_T \) were chosen to be 7.15 k\( \Omega \) and 1200 pF, respectively.

\[
f_{\text{osc}} \approx \frac{1.72}{R_T \times C_T} 
\]

\[
f_{\text{osc}} \approx \frac{1.72}{7.15 \times 1200 \text{ pF}} = 200 \text{ kHz} 
\]

8.2.2.2 Transformer

The transformer of the design consists of two major values, turns ratio and primary side inductance. There is no minimum limit to the turns ratio of the transformer, just a maximum limit. The equation below will give the turns ratio as a function of duty cycle, which if you put in the maximum duty cycle of the converter will give you a maximum turns ratio. The UC1843B-SP design targeted a duty cycle of 50%, which is somewhat low for this controller. The suggested value would be around 70% duty cycle to take advantage of the fact the UC1843B-SP has full duty cycle range. The equation of the turns ratio of the transformer is Equation 3.

\[
N_{\text{PSMAX}} = \frac{V_{\text{IN}} \times D_{\text{MIN}}}{(V_{\text{OUT}} + V_{\text{VIN}}) \times (1 - D_{\text{MIN}})} 
\]

\[
N_{\text{PSMAX}} = \frac{20 \times V \times 0.5}{(5 \times V \times 0.7 \times V) \times (1 - 0.5)} = 3.5
\]

Often the turns ratio will slightly change in design due to how the transformer is manufactured. For the UC1843B-SP design a turns ratio of 3.33 was used. Another turns ratio that is important is the turns ratio of the auxiliary winding. The auxiliary winding is found by figuring out what positive voltage is needed from the auxiliary winding. Picking what voltage the auxiliary winding should have lets one pick the turns ratio from the secondary to the auxiliary winding, which in turn allows for the turns ratio from primary to auxiliary to be found. The equation for the turns ratio for the auxiliary winding is Equation 5.

\[
N_{\text{PA}} = \frac{N_{\text{PB}} \times ((V_{\text{IN}} + V_{\text{VIN}}))}{V_{\text{IN}}} 
\]

\[
N_{\text{PA}} = \frac{3.33 \times (5 \times V \times 0.7 \times V)}{13 \times V} = 1.46
\]

An auxiliary winding of 1.43 was used for the UC1843B-SP design due to manufacturing constraints. The primary inductance of the transformer is found from picking an appropriate ripple current. A higher inductance will often mean reduced current ripple, thus lower EMI and noise, but a higher inductance will also increase physical size and limit the bandwidth of the design. A lower inductance will do the opposite, increasing current ripple, lowering EMI, lowering noise, decreasing physical size, and increasing the limited bandwidth of the design. The percent ripple current can be anywhere from 20% to 80% depending on the design. The equation for finding the primary inductance from the percentage ripple current is Equation 7.

\[
L_{\text{PRI}} = \frac{V_{\text{IN}} \times D_{\text{MIN}}}{V_{\text{IN}} \times D_{\text{MAX}} \times \left(\frac{40 \times V \times 0.25^2}{5 \times V \times 10 \times 0.2} \times 200 \text{ kHz} \times 0.4\right)} 
\]

\[
L_{\text{PRI}} = 25 \text{ } \mu\text{H}
\]

There are quite a few physical limitations when making transformers, so often this inductance will change slightly. For the UC1843B-SP design a primary inductance of 21 \( \mu\text{H} \). This corresponds to a percent ripple of around 0.475. The peak and primary currents of the transformer are also generally useful for figuring out the physical structure of the transformer. See the following equations for proper calculations.

\[
l_{\text{Ripple}} = \frac{V_{\text{IN}} \times D_{\text{MIN}}}{V_{\text{IN}} \times D_{\text{MAX}}} 
\]

\[
l_{\text{Ripple}} = \frac{5 \times 10 \times A \times 0.475}{40 \times V \times 0.25} = 2.375 \text{ A}
\]

\[
l_{\text{HI Peak}} = \frac{V_{\text{IN}} \times I_{\text{HI}}}{V_{\text{IN}} \times D_{\text{MAX}} \times D_{\text{MIN}}} + \frac{l_{\text{Ripple}}}{2} 
\]

\[
l_{\text{HI Peak}} = \frac{5 \times V \times 10 \times A}{20 \times V \times 0.5 \times 0.8} + \frac{2.375}{2} = 7.44 \text{ A}
\]

\[
l_{\text{HRMS}} = \left| D \times \left(\frac{V_{\text{IN}} \times I_{\text{HI}}}{V_{\text{IN}} \times D_{\text{MAX}}}\right)^2 + \frac{l_{\text{Ripple}}}{3}\right|
\]

\[
l_{\text{HRMS}} = 3.75 \text{ A}
\]
8.2.2.3 RCD Diode Clamp

For the UC1843B-SP design a resistor and capacitor are used. The resistor and capacitor is generally a value that is found through testing, but starting values can be obtained. To figure out the resistor and capacitor needed for the RCD clamp, one must first pick how much the node is allowed to overshoot. The equation for finding the voltage of the clamp is Equation 17.

\[ V_{clamp} = K_{clamp} \times N_{ps} \times (V_{out} + V_{Diode}) \]  

Note that \( K_{clamp} \) is recommended to be 1.5 as this will allow for only around 50% overshoot. Knowing the parasitic inductance of the transformer and how much the snubber voltage is allowed to change over the switching cycle, can allow one to figuring out starting values for the resistor and capacitor using Equation 18 and Equation 19.

\[ R_{clamp} = \frac{V_{clamp}^2}{\Delta V_{clamp} \times \Delta f_{clamp} \times f_{sec}} \]  
\[ C_{clamp} = \frac{V_{clamp}}{\Delta V_{clamp} \times R_{clamp} \times f_{sec}} \]

A starting value of 10% is generally used for \( \Delta V_{clamp} \).

8.2.2.4 Output Diode

The voltage stress by the converter on the diode can be found with Equation 20.

\[ V_{DiodeStress} = V_{out} + \frac{V_{MAX}}{N_{ps}} \]  
\[ V_{DiodeStress} = 50 \times 10^3 + \frac{60 \times 10^3}{3.33} = 17 \text{ V} \]

Note that any diode picked should have a voltage rating of well above this value as it does not include parasitic spikes in the equation. The UC1843B-SP diode was picked to have a voltage rating of 60 V.

8.2.2.5 Output Filter and Capacitor

The output capacitance value is picked such that there is enough capacitance for the required voltage ripple and output current load step. The UC1843B-SP design uses equations Equation 22 and Equation 24 to find a minimum capacitance.

\[ C_{out} > \frac{I_{OUT} \times D_{MAX}}{V_{out} \times t_{sec}} \]  
\[ C_{out} > \frac{10 \times 10^3 \times 50 \times 10^3}{50 \times 10^3 \times 200 \times 10^3} = 500 \text{ \mu F} \]
\[ C_{out} > \frac{\Delta I_{MAX}}{2\pi \times f_{sec} \times f_{sec}} \]  
\[ C_{out} > \frac{10 \times 10^3}{2\pi \times 10^3 \times 2 \times 2 \times 10^3} = 1 \text{ mF} \]

A value of around 1145 \mu F was chosen to keep output voltage ripple low. Note that the output voltage ripple in the design was further decreased by adding an output filter and by adding an inductor after a small portion of the output capacitance. Six ceramic capacitors were picked to be placed before the output filter and then the large tantalum capacitors with some small ceramics were added to be part of the output filter. The initial ceramics will help with the initial current ripple, but have a very large output voltage ripple. This voltage ripple will be attenuated by the inductor and capacitor combination placed between the ceramic capacitors and the output. The equations below allow for finding the amount of attenuation that will come from a specific output filter inductance.

\[ F_{resonant} = \frac{1}{2\pi \times L_{resonant} \times C_{out}} \]

In the design an inductance of 500 nH was chosen to attenuate the output voltage ripple and the attenuation was sufficient for the design.
Sometimes the output filter can cause peaking at high frequencies, this can be damped by adding a resistor in parallel with the inductor. For the UC1843B-SP design, 0.5 Ω was used as a very conservative value. The resistance needed to damp the peaking can be calculated using the following equations:

\[
\begin{align*}
F_{\text{resonant}} &= \frac{1}{2\pi \times 0.5 \times 1127 \ \mu F} = 6.7 \ \text{kHz} \\
F_{\text{Zero}} &= \frac{1}{2\pi \times C_{\text{aux}} \times ESR_{\text{aux}}} \\
F_{\text{Zero}} &= \frac{1}{2\pi \times 1127 \ \mu F \times 0.009 \ \Omega} = 15.69 \ \text{kHz} \\
\text{Attenuation}_{SW} &= 40 \times \log_{10} \left( \frac{f_{\text{resonant}}}{f_{\text{zero}}} \right) - 20 \times \log_{10} \left( \frac{f_{\text{SW}}}{f_{\text{zero}}} \right) \\
\text{Attenuation}_{SW} &= 40 \times \log_{10} \left( \frac{200 \ \text{kHz}}{6.7 \ \text{kHz}} \right) - 20 \times \log_{10} \left( \frac{200 \ \text{kHz}}{15.69 \ \text{kHz}} \right) = 36.88 \ \text{dB}
\end{align*}
\]

8.2.2.6 Compensation

The poles and zeros of a flyback converter can be found with the following equations:

\[
\begin{align*}
\omega_0 &= \sqrt{\frac{2 \left( C_{\text{Core}} + C_{\text{Aux}} \right)}{L_{\text{Core}} \times C_{\text{Core}} \times C_{\text{Aux}}}} \quad \text{(32)} \\
\omega_0 &= \left( \frac{500 \ \text{nH} \times 19 \ \mu F}{1127 \ \mu F} \right) = 463 \ \text{kHz} \quad \text{(33)} \\
R_{\text{Filter}} &= \frac{R_s \times L_{\text{Core}} \times \left( C_{\text{Core}} + C_{\text{Aux}} \right)}{L_{\text{Core}} \times \left( C_{\text{Core}} + C_{\text{Aux}} \right) - \left( L_{\text{Core}} \times C_{\text{Core}} \right)} \quad \text{(34)} \\
R_{\text{Filter}} &= \frac{0.5 \times 500 \ \text{nH} \times (19 \ \mu F + 1127 \ \mu F)}{0.25 \times (500 \ \text{nH} \times 19 \ \mu F)} = 0.232 \ \Omega \quad \text{(35)}
\end{align*}
\]

8.2.2.7 Sense Resistor and Slope Compensation

The sense resistor is used to sense the ripple current from the transformer as well as shutdown the switching cycle if the peak current of the converter is allowed to get too high. The voltage threshold of the CS pin is around 1 V, thus the equation to find the sense resistor from the peak current is shown in Equation 44.
Note that \( I_{\text{limit}} \) should be greater than \( I_{\text{PriPeak}} \), and that the voltage offset from the slope compensation will be dependant on the amount of slope compensation in the design. The value of 0.075 \( \Omega \) for the sense resistance was found to be the optimum value adding some headroom for slope compensation offset of 0.1 V. Slope compensation was implemented with a BJT being turned off and on by the RC pin of the device. The BJT was placed between the REF pin and a resistor divider to the CS pin. The optimum slope compensation value can be found from the following equations after picking a value for the top of the divider:

\[
S_c = \frac{V_{\text{cs}} \times R_s \times C_{\text{op}}}{L_{\text{op}} \times N_{\text{op}}}
\]

\[
S_c = \frac{5 \times 0.075 \times 21 \times 3.33}{21 \times 3.33} = 16088
\]

\[
S_{\text{bac}} = \frac{f_{\text{bac}} \times V_{\text{bac}}}{D_{\text{bac}}}
\]

\[
S_{\text{bac}} = \frac{200 \times 1.7 \times 0.25}{1} = 1360000
\]

\[
R_{\text{cs}} = \frac{R_{\text{op}} \times N_{\text{op}} - 1}{S_{\text{bac}}}
\]

\[
R_{\text{cs}} = \frac{1.47 \times 1000}{1360000} - 1 = 141 \Omega
\]

The UC1843B-SP design uses a much higher resistor of 1.47 k\( \Omega \), but this is an attempt to be very conservative. Note that the bottom resistor can be used as part of a filter to the CS pin as well, which is implemented in the design using a capacitor near the CS pin. Care was taken such that the RC filter would not filter the switching frequency by having the RC time constant be a decade less than the switching frequency.

### 8.2.3 Application Curves

![Figure 12. Switch Node of Flyback Converter](image)

For the test in Figure 12, 40 V was applied to the input and 10 A was drawn from the output. Ringing can be present on the switching node if the converter is run in discontinuous conduction mode rather than the continuous conduction mode the design was run with.
Figure 13. Load Step Down With 40 V<sub>IN</sub>
Figure 14. Load Step Up With 40 V\text{IN}

For tests shown in and , 40 V was applied to the input and a load step was applied to the output. The load step applied was from 0 A to 10 A and 10 A to 0 A. Note that those currents do not include the 0.1-A pre-load. The curves show that the stability of the design due to the lack of ringing during the load step.
9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 8 V and 32 V. This input supply should be well regulated. If the input supply is located more than a few inches from the UC1843B-SP converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A tantalum capacitor with a value of 100 µF is a typical choice; however, this varies heavily on the start up circuitry of the device. This is because the input voltage to the device will decrease during start up and the input capacitance will have to provide enough charge to allow the UC1843B-SP to initially switch.

Figure 15. Flyback Regulator

10 Layout

10.1 Layout Guidelines

Always try to use a low EMI inductor with a ferrite closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low EMI characteristics and are located a farther away from the low-power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

10.1.1 Feedback Traces

Try to run the feedback trace as far as possible from the inductor and noisy power traces. The designer should also make the feedback trace as direct as possible and somewhat thick. These two guidelines sometimes involve a trade-off, but keeping the trace away from inductor EMI and other noise sources is the more critical guideline. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

10.1.2 Input/Output Capacitors

When using a low-value ceramic input filter capacitor, locate it as close as possible to the $V_{IN}$ pin of the IC. This eliminates as much trace inductance effects as possible and gives the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case, it should also be positioned as close as possible to the IC.

10.1.3 Compensation Components

External compensation components for stability should also be placed close to the IC. TI recommends to also use surface mount components for the same reasons discussed for the filter capacitors. These should not be located very close to the inductor either.
Layout Guidelines (continued)

10.1.4 Traces and Ground Planes

Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere. The inductor, output capacitors, and output diode should be as close as possible to each other. This helps reduce the EMI radiated by the power traces due to the high-switching currents through them. This also reduces lead inductance and resistance, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This reduces noise by reducing ground loop errors and absorbing more of the EMI radiated by the inductor.

For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are located) and the signal plane (where the feedback and compensation and components are located) for improved performance. On multi-layer boards, vias are required to connect traces and different planes. Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states: one state when the switch is on and one when the switch is off. During each state there is a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

10.2 Layout Example

NOTE: High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 16. Open-Loop Laboratory Test Fixture
11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates
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11.5 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# PACKAGE INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<tbody>
<tr>
<td>5962R8670412V9A</td>
<td>PREVIEW</td>
<td>XCEPT</td>
<td>KGD</td>
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<td>TBD</td>
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<td>R8670412VYC</td>
<td>UC1843B-SP</td>
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(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The terminals are gold plated.
5. This drawing does not comply with MIL STD 1835. Do not use this package for compliant product.
6. Metal lid is connected to back side pad metalization.
EXAMPLE BOARD LAYOUT

HKU0010A

CFP - 2.63mm max height

CERAMIC DUAL FLATPACK

HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X
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