Rad-Tolerant Class-V, Precision Analog Controller

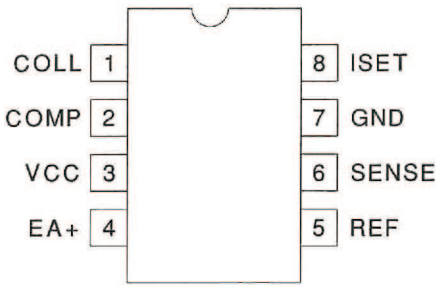
Check for Samples: UC19432-SP

FEATURES

- **QML-V Qualified, SMD 5962-09233**
- **Rad Tolerant: 30 kRad(Si) TID** (1)
  - **TID Dose Rate = 10 mRad/sec**
- **Programmable Transconductance for Optimum Current Drive**
- **Accessible 1.3 V precision Reference**
- **Both Error Amplifier Inputs Available**
- **0.7% Overall Reference Tolerance**
- **0.4% Initial Accuracy**
- **2.4-V to 24-V Operating Supply Voltage and User Programmable Reference**
- **Reference Accuracy Maintained for Entire Range of Supply Voltage**
- **Superior Accuracy and Easier Compensation for Optoisolator Application**
- **Low Quiescent Current (0.5 mA Typ)**

(1) Radiation tolerance is a typical value based upon initial device qualification. Radiation Lot Acceptance Testing is available - contact factory for details.

JG PACKAGE
(TOP VIEW)



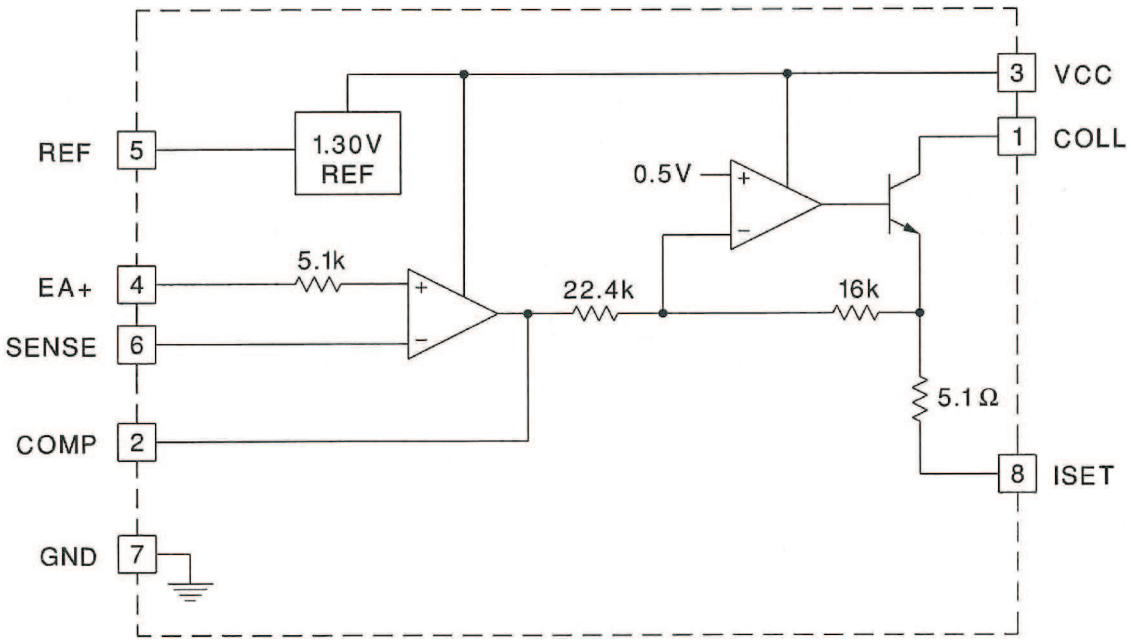
DESCRIPTION

The UC19432 is an adjustable precision analog controller with 100-mA sink capability if the ISET pin is grounded. A resistor between ISET and ground will modify the transconductance while decreasing the maximum current sink. This will add further control in the optocoupler configuration. The trimmed precision reference along with the non-inverting error amplifier inputs are accessible for custom configuration. A sister device, the UC19431 adjustable shunt regulator, has an on-board resistor network providing six preprogrammed voltage levels, as well as exernal programming capability.

ORDERING INFORMATION

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP-8	5962-0923301VPA	UC19432-SP

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
VCC	Supply voltage	24	V
V_{COLL}	Regulated output	24	V
SENSE, EA+	EA input	6	V
COMP	EA compensation	6	V
REF	Reference output	6	V
I_{COLL}	Output sink current (continuous or time average)	125	mA
ISET	Output source current (continuous or time average)	–125	mA
	Power dissipation at $T_A \leq 25°C$ Derate 8 mW/°C for $T_A > 25°C$	1	W
	Storage temperature range	–65 to 150	°C
	Junction temperature	–55 to 150	°C
	Lead temperature (soldering, 10 seconds)	300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, COLL output = 2.4 V to 24 V, VCC = 15 V, I_{COLL} = 10 mA, $T_A = T_J$ = –55°C to 125°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference voltage tolerance	T_A = 25°C, V_{COLL} = 5 V	1.295	1.3	1.305	V
Reference temperature tolerance	V_{COLL} = 5 V	1.291	1.3	1.309	V
Reference line regulation	VCC = 2.4 V to 24 V, V_{COLL} = 5 V		10	38	mV
Reference load regulation	I_{COLL} = 10 mA TO 50 mA, V_{COLL} = 5 V		10	38	mV
Reference sink current				10	µA
Reference source current		-10			µA
EA input bias current		–0.5	–0.2		µA
EA input offset voltage		-4		4	mV
EA+ Operational voltage limitations		0.9		1.6	V
EA output current sink (internally limited)		16			µA
EA output current source				-0.8	mA
Minimum operating current	VCC = 24 V, V_{COLL} = 5 V		0.5	0.8	mA
Collector current limit(1)	V_{COLL} = VCC = 24 V, Ref = 1.3 V, ISET = GND		130	155	mA
Collector saturation	I_{COLL} = 20 mA	0.7	1.1	1.5	V
Transconductance (gm)(1) (2)	VCC = 2.4 V to 24 V, V_{COLL} = 3 V, ISET = GND	–170	–140	–110	mS
Error amplifier AVOL		60	90		dB
Error amplifier GBW		1.5	3		MHz
Transconductance amplifier GBW			3		MHz

(1) Programmed transconductance and collector current limit equations are specified in the ISET pin description.
(2) Measured as $\Delta I_{COLL}/\Delta V_{COMP}$ for I_{COLL} = 5 mA to 20 mA.

PIN DESCRIPTIONS

COLL The collector of the output transistor with a maximum voltage of 24 V. This pin is the output of the transconducance amplifier. The overall open loop voltage gain of the transconductance amplifier is gm x R_L, where gm is designed to be –140 mS ±30 mS and R_L represents the output load.

COMP The output of the error amplifier and the input to the transconductance amplifier. This pin is available to compensate the high frequency gain of the error amplifier. It is internally voltage limited to approximately 2 V.

EA+ The non-inverting input to the error amplifier.

GND The reference and power ground for the device. The power ground of the output ransistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

ISET The current set pin for the transconductance amplifier. The transconductance will be –140 mS as specified in the electrical table if this pin is grounded. If a resistance, R_L, is added to the ISET pin, the resulting new transconductance is calculated using Equation 1. The maximum current will be approximated by Equation 2.

$$gm = \frac{-0.714}{(5.1\ \Omega + R_L)} \quad (1)$$

$$I_{MAX} = \frac{0.65\ V}{5.1\ \Omega + R_L} \quad (2)$$

REF The output of the trimmed precision reference. It can source or sink 10 µA and still maintain less than ±1% output variation.

SENSE The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point. The error amplifier uses the SENSE input to compare against the 1.3-V on-chip reference.

The SENSE pin is also used as the under-voltage lockout (UVLO). It is intended to keep the chip from operating until the internal reference is properly biased. The threshold is approximately 1 V. It is important that once the UVLO is released, the error amplifier can drive the transconductance amplifier to stabilize the loop. If a capacitor is connected between the SENSE and COMP pins to create a pole, it will limit the slew rate of the error amplifier. To increase the bandwidth and ensure startup a low load current, it is recommended to create a zero along with the pole as shown in he UC19431 shunt regulator application. The error amplifier must slew 2 V to drive the transconductance amplifier initially on.

VCC The power connection for the device. The minimum to maximum operating voltage is 2.4 V to 24 V. The quiescent current is typically 0.5 mA.

OVER-VOLTAGE COMPARATOR APPLICATION

The signal V_{IN} senses the input voltage. As long as the input voltage is less than 5.5 V, the output is equal to the voltage on V_{IN}. During this region of operation, the diode is reversed biased which keeps the EA+ pin at 1.3 V. When V_{IN} exceeds the over-voltage threshold of 5.5 V, the output is driven low. This forward biases the diode and creates hyseresis by changing the threshold to 4.5 V.

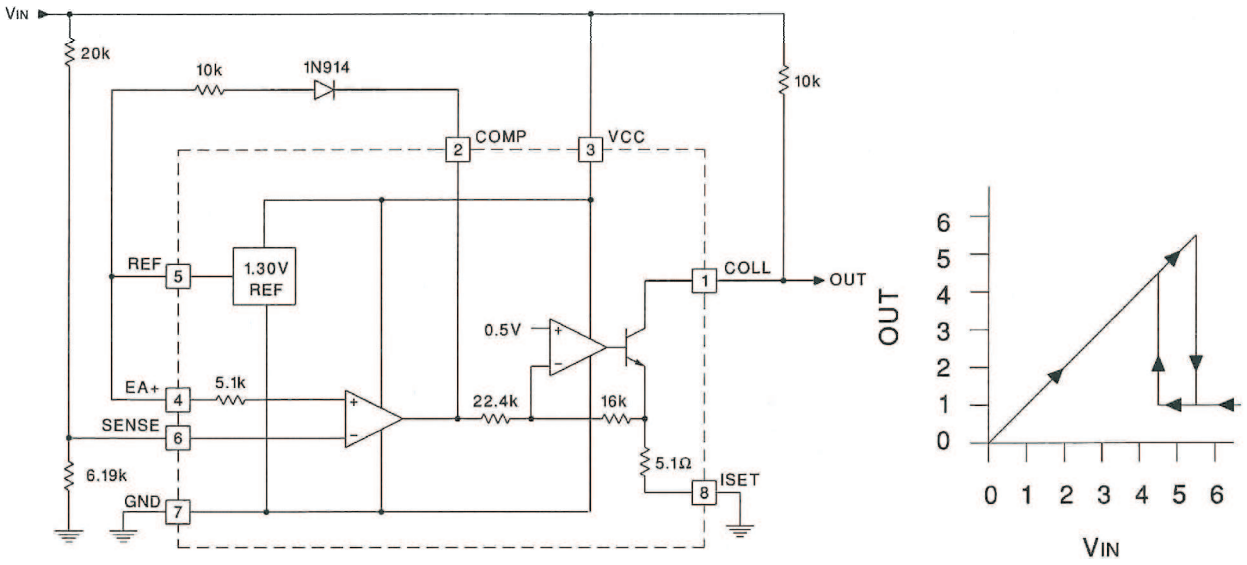


Figure 1. 5.5-V Over-Voltage Comparator With Hysteresis

OPTOCOUPLER APPLICATION

The optocoupler application shown in Figure 2 takes advantage of the accessible pins REF and ISET. The ISET pin has a 33-Ω resistor to ground that protects the optocoupler by limiting the current to about 16 mA. This also lowers the transconductance to approximately 19 mS. The ability to adjust the transconducance gives the designer further control of the loop gain. The REF pin is available to satisfy any high precision voltage requirements.

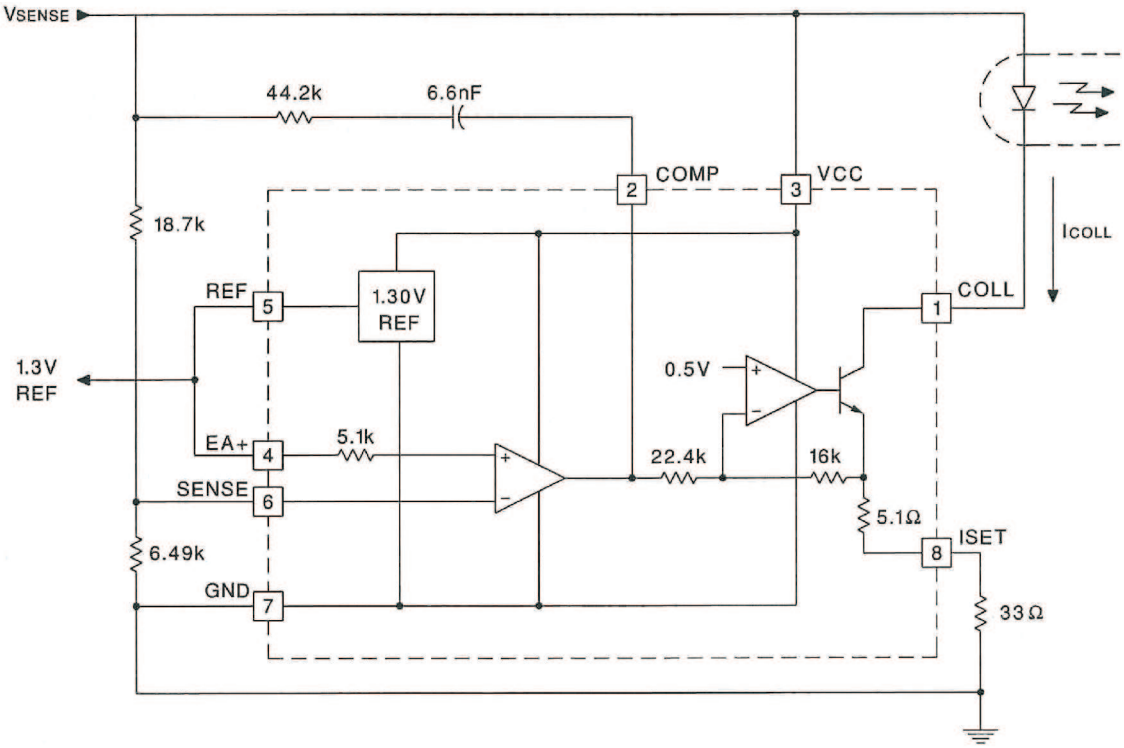


Figure 2. 5-V Optocoupler Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0923301VPA	ACTIVE	CDIP	JG	8	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	0923301VPA UC19432-SP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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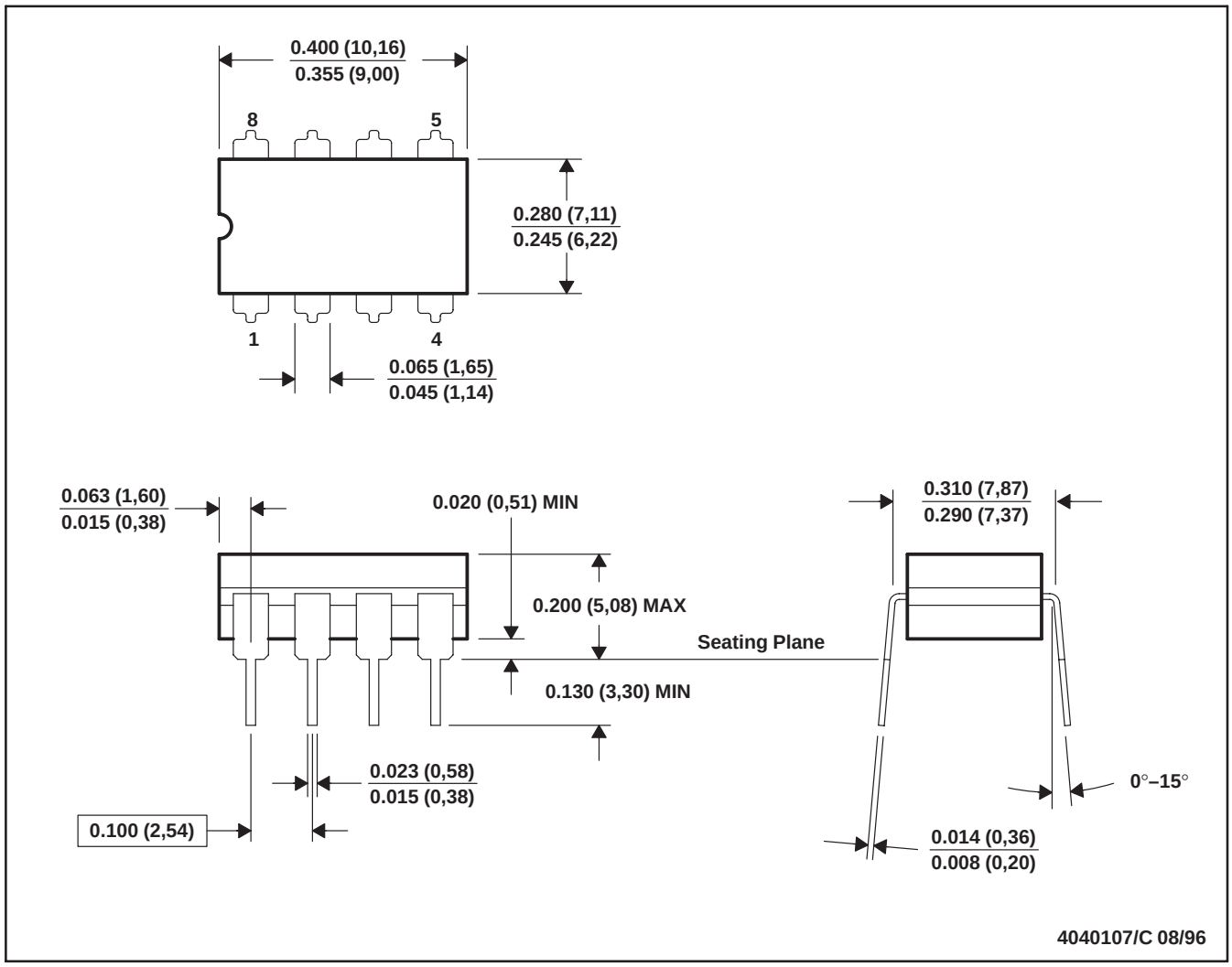
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

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