

# Buck Pulse Width Modulator Stepdown Voltage Regulator

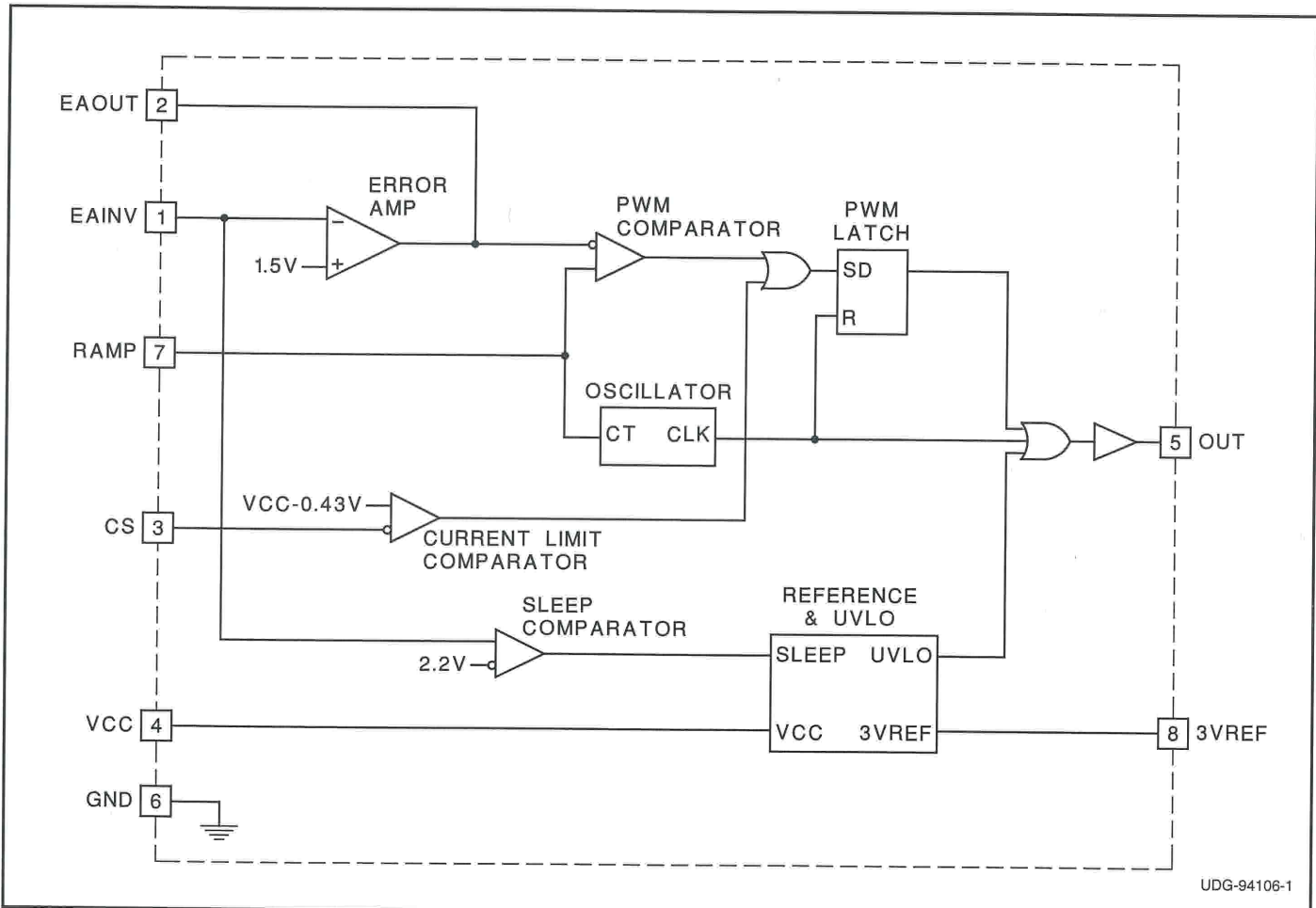
## FEATURES

- Simple Single Inductor Buck PWM Stepdown Voltage Regulation
- Drives External PMOS Switch
- Contains UVLO Circuit
- Includes Pulse-by-Pulse Current Limit
- Low 50 $\mu$ A Sleep Mode Current

## DESCRIPTION

The UC3573 is a Buck pulse width modulator which steps down and regulates a positive input voltage. The chip is optimized for use in a single inductor buck switching converter employing an external PMOS switch. The block diagram consists of a precision reference, an error amplifier configured for voltage mode operation, an oscillator, a PWM comparator with latching logic, and a 0.5A peak gate driver. The UC3573 includes an undervoltage lockout circuit to insure sufficient input supply voltage is present before any switching activity can occur, and a pulse-by-pulse current limit. Input current can be sensed and limited to a user determined maximum value. In addition, a sleep comparator interfaces to the UVLO circuit which turns the chip off when the input voltage is below the UVLO threshold. This reduces the supply current to only 50 $\mu$ A, making the UC3573 ideal for battery powered applications.

## BLOCK DIAGRAM

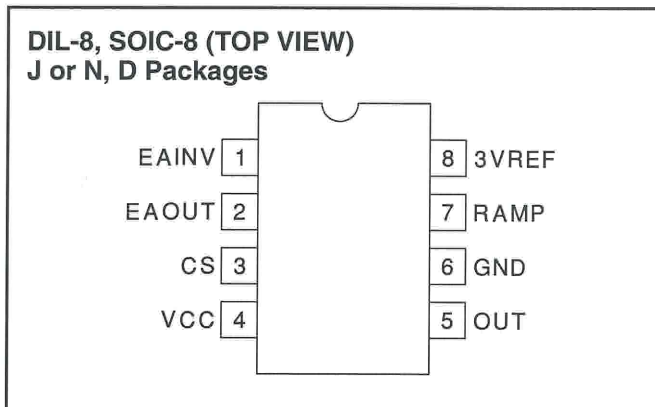


## ABSOLUTE MAXIMUM RATINGS

VCC	35V
EAINV	-0.6V to VCC
I <sub>EAOUT</sub>	25mA
RAMP	-0.3V to 4V
CS	-0.3V to VCC
I <sub>OUT</sub>	-0.7A to 0.7A
I <sub>3VREF</sub>	-15mA
Storage Temperature	-65°C to +150°C
Junction Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

## CONNECTION DIAGRAMS



**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified, these parameters apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1573,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2573, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3573,  $V_{CC} = 5\text{V}$ ,  $C_T = 680\text{pF}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Reference Section</b>					
3VREF		2.94	3	3.06	V
Line Regulation	$V_{CC} = 4.75$ to $30\text{V}$		1	10	mV
Load Regulation	$I_{3VREF} = 0$ to $-5\text{mA}$		1	10	mV
<b>Oscillator Section</b>					
Frequency	$V_{CC} = 5\text{V}$ , $30\text{V}$	85	100	115	kHz
<b>Error Amp Section</b>					
EAINV	EAOUT = $2\text{V}$	1.45	1.5	1.55	V
I <sub>EAINV</sub>	EAOUT = $2\text{V}$		-0.2	-1	$\mu\text{A}$
AVOL	EAOUT = $0.5\text{V}$ to $3\text{V}$	65	90		dB
EAOUT High	EAINV = $1.4\text{V}$	3.6	4	4.4	V
EAOUT Low	EAINV = $1.6\text{V}$		0.1	0.2	V
I <sub>EAOUT</sub>	EAINV = $1.4\text{V}$ , EAOUT = $2\text{V}$	-350	-500		$\mu\text{A}$
	EAINV = $1.6\text{V}$ , EAOUT = $2\text{V}$	7	20		mA
Unity Gain Bandwidth	$T_J = 25^\circ\text{C}$ , $F = 10\text{kHz}$	0.6	1		MHz
<b>Current Sense Comparator Section</b>					
Threshold (referred to VCC)		-0.39	-0.43	-0.47	V
Input Bias Current	CS = VCC		150	800	nA
CS Propagation Delay			400		ns
<b>Gate Drive Output Section</b>					
OUT High Saturation	$I_{OUT} = 0$		0	0.3	V
	$I_{OUT} = -10\text{mA}$		0.7	1.5	V
	$I_{OUT} = -100\text{mA}$		1.5	2.5	V
OUT Low Saturation	$I_{OUT} = 10\text{mA}$		0.1	0.4	V
	$I_{OUT} = 100\text{mA}$		1.5	2.2	V
Rise Time	$T_J = 25^\circ\text{C}$ , $C_{LOAD} = 1\text{nF} + 3.3\text{ Ohms}$		30	80	ns
Fall Time	$T_J = 25^\circ\text{C}$ , $C_{LOAD} = 1\text{nF} + 3.3\text{ Ohms}$		30	80	ns
<b>Pulse Width Modulator Section</b>					
Maximum Duty Cycle	EAINV = $1.4\text{V}$		92	96	%
Minimum Duty Cycle	EAINV = $1.6\text{V}$			0	%
Modulator Gain	EAOUT = $1.5\text{V}$ to $2.5\text{V}$	25	35	45	%/V
<b>Undervoltage Lockout Section</b>					
Start Threshold		3.5	4.2	4.5	V
Hysteresis		100	200	300	mV

**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified, these parameters apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1573,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2573, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3573,  $V_{CC} = 5\text{V}$ ,  $C_T = 680\text{pF}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Sleep Mode Section</b>					
Threshold		1.8	2.2	2.6	V
<b>Supply Current Section</b>					
$I_{VCC}$	$V_{CC} = 30\text{V}$		9	12	mA
$I_{VCC}$	$V_{CC} = 30\text{V}, E_{AINV} = 3\text{V}$		50	150	$\mu\text{A}$

## PIN DESCRIPTIONS

**3VREF:** Precision 3V reference. Bypass with 100nF capacitor.

**CS:** Peak current limit sense pin. Senses the current across a current sense resistor placed between  $V_{CC}$  and source of the PMOS Buck switch. OUT will be held high (PMOS buck switch off) if  $V_{CC} - CS$  exceeds 0.4V.

**EAINV:** Inverting input to error amplifier. VOUT sense feedback connected to this pin. The non-inverting input of the error amplifier is internally connected to:

$$\frac{3VREF}{2} \text{ Volts.}$$

Connecting the EAINV pin to an external voltage greater than 2.6V commands the chip to go into a low current sleep mode.

**EAOUT:** Output of error amplifier. Use EAOUT and EAINV for loop compensation components.

**GND:** Circuit Ground.

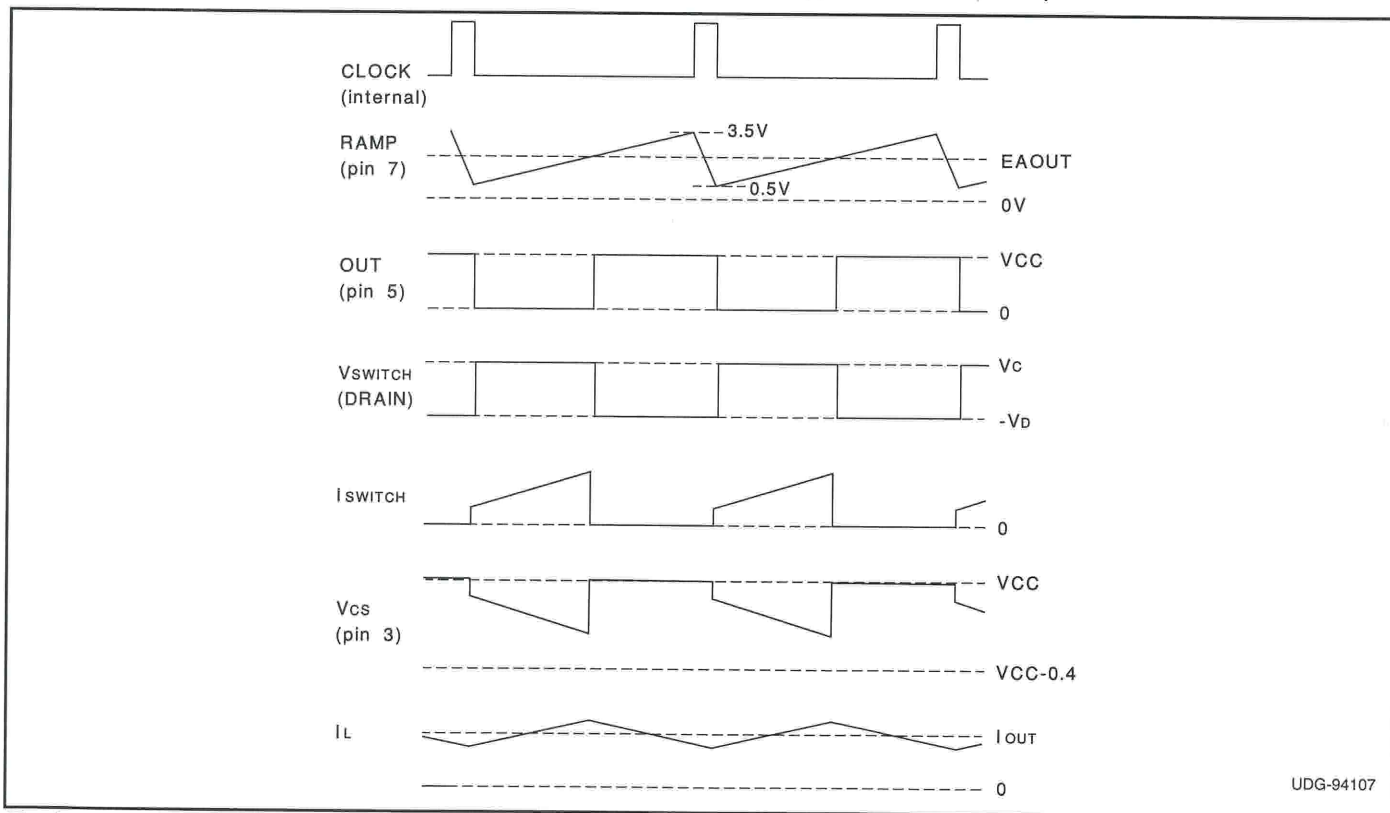
**OUT:** Gate drive for external PMOS switch connected between  $V_{CC}$  and the flyback inductor. OUT drives the gate of the PMOS switch between  $V_{CC}$  and GND.

**RAMP:** Oscillator and ramp for pulse width modulator. Frequency is set by a capacitor to GND by the equation

$$F = \frac{1}{15k \cdot C_{RAMP}}$$

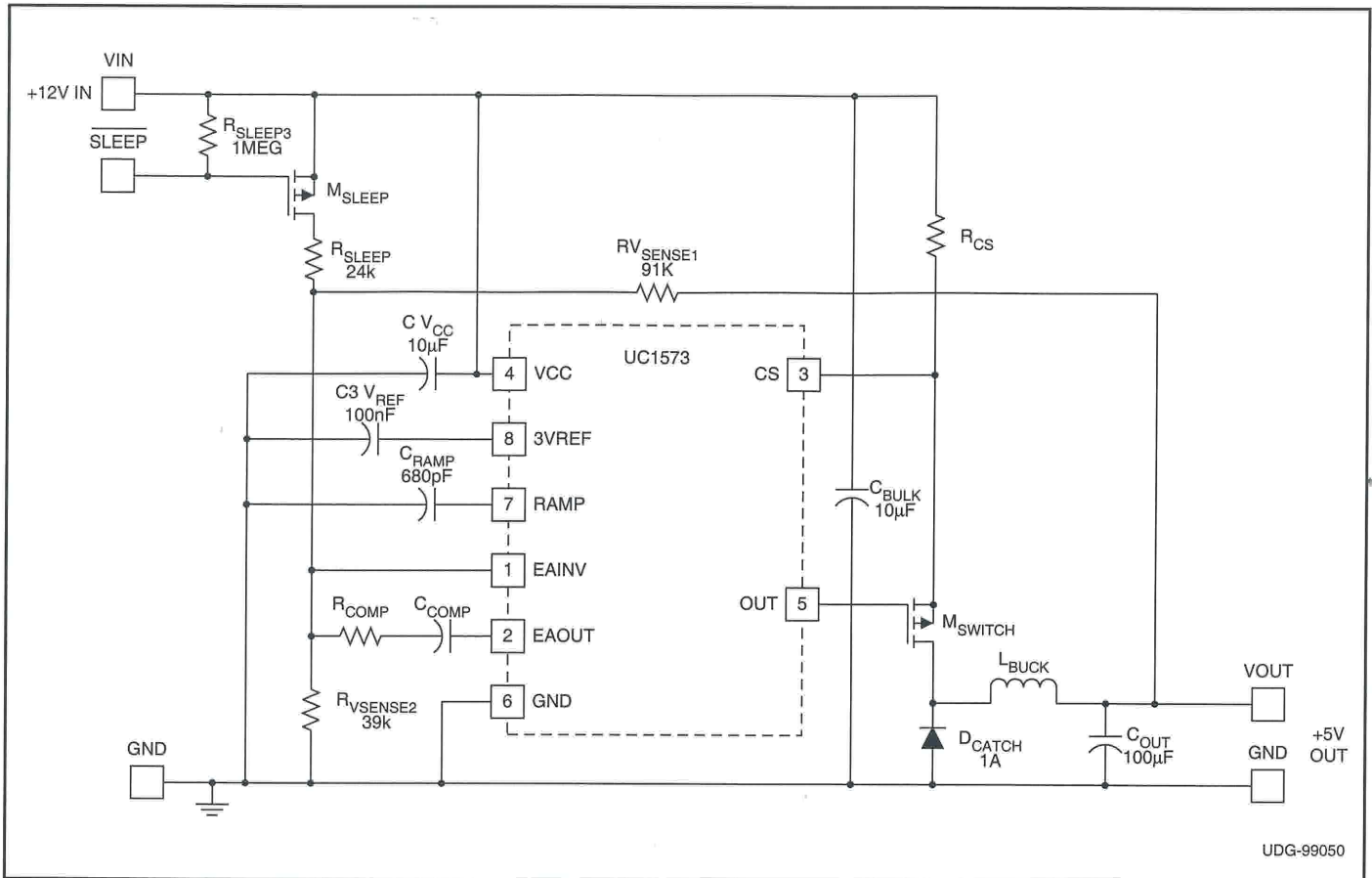
Recommended operating frequency range is 10kHz to 200kHz.

**VCC:** Input voltage supply to chip. Range is 4.75V to 30V. Bypass with a 1 $\mu\text{F}$  capacitor.



Typical Waveforms.

**TYPICAL APPLICATION: 12V TO 5V BUCK CONVERTER**



**REVISION HISTORY**

SLUS346 to SLUS346A, July 2010:

Changed Supply Current I<sub>VCC</sub> units from A to μA

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">UC2573D</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2573D
<a href="#">UC2573DTR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2573D
<a href="#">UC3573D</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3573D
<a href="#">UC3573DTR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3573D

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2573DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3573DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2573DTR	SOIC	D	8	2500	340.5	338.1	20.6
UC3573DTR	SOIC	D	8	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UC2573D	D	SOIC	8	75	507	8	3940	4.32
UC2573DG4	D	SOIC	8	75	507	8	3940	4.32
UC3573D	D	SOIC	8	75	507	8	3940	4.32





D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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