UCC21220, UCC21220A 4-A/6-A, Dual-Channel Basic and Functional Isolated Gate Driver With High Noise Immunity

1 Features

- Supports basic and functional isolation
- CMTI greater than 100-V/ns
- 4-A peak source, 6-A peak sink output
- Switching parameters:
  - 40-ns maximum propagation delay
  - 5-ns maximum delay matching
  - 5.5-ns maximum pulse-width distortion
  - 35-µs maximum VDD power-up delay
- Up to 18-V VDD output drive supply
  - 5-V and 8-V VDD UVLO Options
- Operating temp. range (T_A) –40°C to 125°C
- Narrow body SOIC-16 (D) package
- Rejects input pulses shorter than 5-ns
- TTL and CMOS compatible inputs
- Safety-related certifications:
  - 4242-V_{PK} isolation per DIN V VDE V 0884-11:2017-01 and DIN EN 61010-1 (planned)
  - 3000-V_{RMS} isolation for 1 minute per UL 1577
  - CQC certification per GB4943.1-2011 (planned)

2 Applications

- Server power supplies
- Solar inverter, solar power optimizer
- Telecom brick converter
- Wireless infrastructure
- Industrial transportation and robotics

3 Description

The UCC21220 and UCC21220A devices are basic and functional isolated dual-channel gate drivers with 4-A peak-source and 6-A peak-sink current. They are designed to drive power MOSFETs and GaNFETs in PFC, Isolated DC/DC, and synchronous rectification applications, with fast switching performance and robust ground bounce protection through greater than 100-V/ns common-mode transient immunity (CMTI).

These devices can be configured as two low-side drivers, two high-side drivers, or half-bridge drivers. Two outputs can be paralleled to form a single driver which doubles the drive strength for heavy load conditions due to the best-in-class delay matching performance.

Protection features include: DIS pin shuts down both outputs simultaneously when it is set high; INA/B pin rejects input transient shorter than 5-ns; both inputs and outputs can withstand –2-V spikes for 200-ns, all supplies have undervoltage lockout (UVLO), and active pull down protection clamps the output below 2.1-V when unpowered or floated.

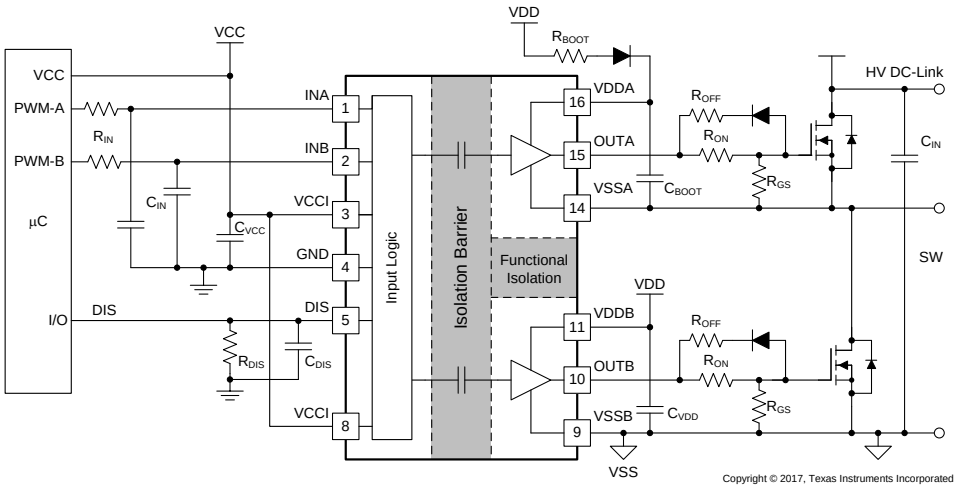
With these features, these devices enable high efficiency, high power density, and robustness in a wide variety of power applications.

Device Information[1]

PART NUMBER	PACKAGE	UVLO
UCC21220	SOIC (16)	8-V
UCC21220A	SOIC (16)	5-V

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2018) to Revision E — **Page**

- Changed Features, Applications, and Description sections ... 1
- Changed from Functional Diagram to Typical Application ... 1
- Added UL certificate number ... 9
- Added maximum VCCI Power-up Delay Time: UVLO Rise to OUTA, OUTB ... 11
- Added maximum VDDA, VDDB Power-up Delay Time: UVLO Rise to OUTA, OUTB ... 11

Changes from Revision C (August 2018) to Revision D — **Page**

- Changed the marketing status of the UCC21220A from Product Preview to initial release. ... 1

Changes from Revision B (May 2018) to Revision C — **Page**

- Added 5V VDD UVLO threshold and hysteresis graph in *Typical Characteristics* section ... 12

Changes from Revision A (December 2017) to Revision B — **Page**

- Added UCC21220A Advance Information device. ... 1
- Changed DTI from 16µm to 17µm in *Insulation Specifications* table ... 8

Copyright © 2017–2019, Texas Instruments Incorporated

Changes from Original (November 2017) to Revision A **Page**

- Changed *Maximum Pulse-Width Distortion* from "5-ns" to "5.5-ns" in *Features* section 1
- Changed data sheet status from *Advance Information* to *Production Data* 1
- Clarified descriptions in *Pin Functions* table 5
- Separated figure titles and condition statements in *Typical Characteristics* section 12
- Added typical timing specifications to *Power-up UVLO Delay to OUTPUT* section 17
- Added guideline to *Layout Guidelines* section 35

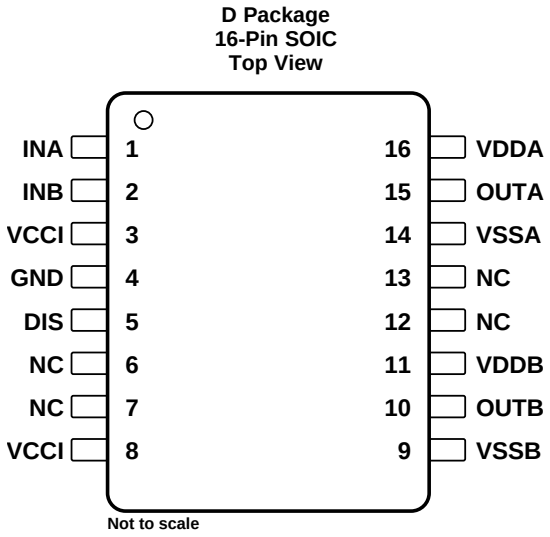
Copyright © 2017–2019, Texas Instruments Incorporated

5 Device Comparison Table

DEVICE OPTIONS	UVLO	RECOMMENDED VDD SUPPLY MIN.	PACKAGE
UCC21220D	8-V	9.2-V	Narrow Body SOIC-16
UCC21220AD	5-V	6.0-V	Narrow Body SOIC-16

Copyright © 2017–2019, Texas Instruments Incorporated

6 Pin Configuration and Functions



Pin Functions

PIN		I/O(1)	DESCRIPTION
DIS	5	I	Disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using a ≈ 1-nF low ESR/ESL capacitor close to DIS pin when connecting to a µC with distance.
GND	4	P	Primary-side ground reference. All signals in the primary side are referenced to this ground.
INA	1	I	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
INB	2	I	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
NC	6		No internal connection.
	7		
	12		
	13		
OUTA	15	O	Output of driver A. Connect to the gate of the A channel FET or IGBT.
OUTB	10	O	Output of driver B. Connect to the gate of the B channel FET or IGBT.
VCCI	3	P	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible.
VCCI	8	P	This pin is internally shorted to pin 3.
VDDA	16	P	Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible.
VDDB	11	P	Secondary-side power for driver B. Locally decoupled to VSSB using a low ESR/ESL capacitor located as close to the device as possible.
VSSA	14	P	Ground for secondary-side driver A. Ground reference for secondary side A channel.
VSSB	9	P	Ground for secondary-side driver B. Ground reference for secondary side B channel.

(1) P = power, G = ground, I = input, O = output

Copyright © 2017–2019, Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input bias pin supply voltage	VCCI to GND	–0.5	6	V
Driver bias supply	VDDA-VSSA, VDDB-VSSB	–0.5	20	V
Output signal voltage	OUTA to VSSA, OUTB to VSSB	–0.5	V_{VDDA}+0.5, V_{VDDB}+0.5	V
	OUTA to VSSA, OUTB to VSSB, Transient for 200 ns(2)	–2	V_{VDDA}+0.5, V_{VDDB}+0.5	V
Input signal voltage	INA, INB, DIS to GND	–0.5	V_{VCCI}+0.5	V
	INA, INB Transient to GND for 200ns(2)	–2	V_{VCCI}+0.5	V
Junction temperature, T_J (3)		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Values are verified by characterization and are not production tested.
(3) To maintain the recommended operating conditions for T_J, see the Thermal Information.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
VCCI	VCCI Input supply voltage		3	5.5	V
VDDA, VDDB	Driver output bias supply	UCC21220 – 8V UVLO Version	9.2	18	V
		UCC21220A – 5V UVLO Version	6.0	18	V
T_J	Junction Temperature		–40	130	°C
T_A	Ambient Temperature		–40	125	°C

Copyright © 2017–2019, Texas Instruments Incorporated

7.4 Thermal Information

THERMAL METRIC(1)		UCC21220, UCC21220A	UNIT
		D (SOIC)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Power Ratings

			VALUE	UNIT
P_D	Power dissipation	VCCI = 5.5 V, VDDA/B = 12 V, INA/B = 3.3 V, 5.4 MHz 50% duty cycle square wave 1.0-nF load	1825	mW
P_{DI}	Power dissipation by transmitter side		15	mW
P_{DA}, P_{DB}	Power dissipation by each driver side		905	mW

Copyright © 2017–2019, Texas Instruments Incorporated

7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance(1)	Shortest pin-to-pin distance through air	> 4	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	> 4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group		I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
		Rated mains voltage ≤ 600 V_{RMS}	I-II	
DIN V VDE V 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	990	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test;	700	V_{RMS}
		DC Voltage	990	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 7800\ V_{PK}$ (qualification)	6000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	<5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	<5	
		Method b1; At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$; t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	<5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 sin (2πft), f =1 MHz	0.5	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S =150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 3000 V_{RMS}, t = 60 s. (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 3600 V_{RMS}, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

Copyright © 2017–2019, Texas Instruments Incorporated

7.7 Safety-Related Certifications

VDE	UL	CQC
Certified according to DIN V VDE V 0884-11:2017-01 and DIN EN 61010-1 (VDE 0411-1):2011-07	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011
Basic Insulation Maximum Transient Overvoltage, 4242 V_{PK}; Maximum Repetitive Peak Voltage, 990 V_{PK}; Maximum Surge Isolation Voltage, 6000 V_{PK}	Single protection, 3000 V_{RMS}	Basic insulation, Altitude ≤ 5000 m, Tropical Climate, 660 V_{RMS} maximum working voltage
Planned for certification	Certificate Number: E181974	Planned for certification

7.8 Safety-Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	SIDE	MIN	TYP	MAX	UNIT
I_S	Safety output supply current	$R_{\theta JA}$ = 68.5ºC/W, $V_{VDDA/B}$ = 12 V, T_J = 150°C, T_A = 25°C See Figure 1	DRIVER A, DRIVER B			75	mA
P_S	Safety supply power	$R_{\theta JA}$ = 68.5ºC/W, V_{VCCI} = 5.5 V, T_J = 150°C, T_A = 25°C See Figure 2	INPUT			15	mW
			DRIVER A			905	
			DRIVER B			905	
			TOTAL			1825	
T_S	Safety temperature (1)					150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the ***Thermal Information*** table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

Copyright © 2017–2019, Texas Instruments Incorporated

7.9 Electrical Characteristics

V_{VCCI} = 3.3 V or 5.0 V, 0.1-µF capacitor from VCCI to GND and 1uF capacitor from VDDA/B to VSSA/B, V_{VDDA} = V_{VDDB} = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, T_A = –40°C to +125°C, unless otherwise noted(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCCI}	VCCI quiescent current	V_{INA} = 0 V, V_{INB} = 0 V		1.5	2.0	mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB quiescent current	V_{INA} = 0 V, V_{INB} = 0 V		1.0	1.8	mA
I_{VCCI}	VCCI operating current	(f = 500 kHz) current per channel		2.5		mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB operating current	(f = 500 kHz) current per channel, C_{OUT} = 100 pF, V_{VDDA}, V_{VDDB} = 12 V		2.5		mA
VCC SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VCCI_ON}	UVLO Rising threshold		2.55	2.7	2.85	V
V_{VCCI_OFF}	UVLO Falling threshold		2.35	2.5	2.65	V
V_{VCCI_HYS}	UVLO Threshold hysteresis			0.2		V
UCC21220A VDD SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS (5-V UVLO Version)						
V_{VDDA_ON}, V_{VDDB_ON}	UVLO Rising threshold		5.0	5.5	5.9	V
V_{VDDA_OFF}, V_{VDDB_OFF}	UVLO Falling threshold		4.7	5.2	5.6	V
V_{VDDA_HYS}, V_{VDDB_HYS}	UVLO Threshold hysteresis			0.3		V
UCC21220 VDD SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS (8-V UVLO Version)						
V_{VDDA_ON}, V_{VDDB_ON}	UVLO Rising threshold		8	8.5	9	V
V_{VDDA_OFF}, V_{VDDB_OFF}	UVLO Falling threshold		7.5	8	8.5	V
V_{VDDA_HYS}, V_{VDDB_HYS}	UVLO Threshold hysteresis			0.5		V
INA, INB AND DISABLE						
V_{INAH}, V_{INBH}, V_{DISH}	Input high threshold voltage		1.6	1.8	2	V
V_{INAL}, V_{INBL}, V_{DISL}	Input low threshold voltage		0.8	1	1.25	V
V_{INA_HYS}, V_{INB_HYS}, V_{DIS_HYS}	Input threshold hysteresis			0.8		V
OUTPUT						
I_{OA+}, I_{OB+}	Peak output source current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement		4		A
I_{OA-}, I_{OB-}	Peak output sink current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement		6		A
R_{OHA}, R_{OHB}	Output resistance at high state	I_{OUT} = –10 mA, R_{OHA}, R_{OHB} do not represent drive pull-up performance. See t_{RISE} in Switching Characteristics and Output Stage for more details.		5		Ω
R_{OLA}, R_{OLB}	Output resistance at low state	I_{OUT} = 10 mA		0.55		Ω
V_{OHA}, V_{OHB}	Output voltage at high state	V_{VDD} = 12 V, I_{OUT} = –10 mA		11.95		V
V_{OLA}, V_{OLB}	Output voltage at low state	V_{VDD} = 12 V, I_{OUT} = 10 mA		5.5		mV
V_{OAPDA}, V_{OAPDB}	Driver output (V_{OUTA}, V_{OUTB}) active pull down	V_{VDDA} and V_{VDDB} unpowered, I_{OUTA}, I_{OUTB} = 200 mA		1.75	2.1	V

(1) Current direction in the testing conditions are defined to be positive into the pin and negative out of the specified terminal (unless otherwise noted).
(2) Parameters that has only typical values, are not production tested and guaranteed by design.

Copyright © 2017–2019, Texas Instruments Incorporated

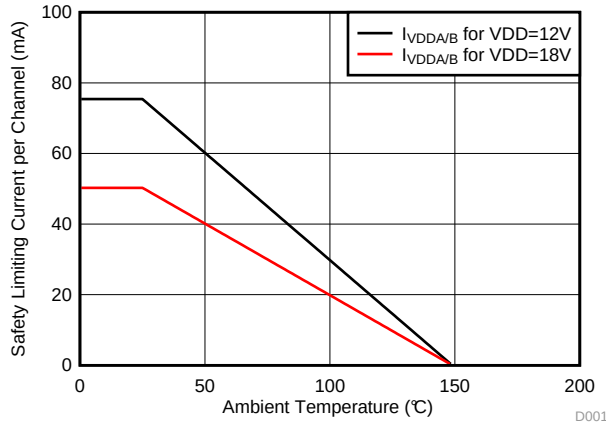
7.10 Switching Characteristics

V_{VCCI} = 3.3 V or 5.5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, load capacitance C_{OUT} = 0 pF, T_J = –40°C to +125°C, unless otherwise noted(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}	Output rise time, see Figure 28	C_{VDD} = 10 µF, C_{OUT} = 1.8 nF, V_{VDDA}, V_{VDDB} = 12 V, f = 1 kHz		5	16	ns
t_{FALL}	Output fall time, see Figure 28	C_{VDD} = 10 µF, C_{OUT} = 1.8 nF , V_{VDDA}, V_{VDDB} = 12 V, f = 1 kHz		6	12	ns
t_{PWmin}	Minimum input pulse width that passes to output, see Figure 25 and Figure 26	Output does not change the state if input signal less than t_{PWmin}		10	20	ns
t_{PDHL}	Propagation delay at falling edge, see Figure 27	INx high threshold, V_{INH}, to 10% of the output		28	40	ns
t_{PDLH}	Propagation delay at rising edge, see Figure 27	INx low threshold, V_{INL}, to 90% of the output		28	40	ns
t_{PWD}	Pulse width distortion in each channel, see Figure 27	$\lvert t_{PDLHA} - t_{PDHLA} \rvert$, $\lvert t_{PDLHB} - t_{PDHLB} \rvert$			5.5	ns
t_{DM}	Propagation delays matching, $\lvert t_{PDLHA} - t_{PDLHB} \rvert$, $\lvert t_{PDHLA} - t_{PDHLB} \rvert$, see Figure 27	f = 1 MHz			5	ns
$t_{VCCI+ to OUT}$	VCCI Power-up Delay Time: UVLO Rise to OUTA, OUTB, See Figure 30	INA or INB tied to VCCI		40	59	µs
$t_{VDD+ to OUT}$	VDDA, VDDB Power-up Delay Time: UVLO Rise to OUTA, OUTB See Figure 31	INA or INB tied to VCCI		22	35	µs
$\lvert CM_H \rvert$	High-level common-mode transient immunity (See CMTI Testing)	Slew rate of GND vs. VSSA/B, INA and INB both are tied to GND or VCCI; V_{CM}=1000 V;	100			V/ns
$\lvert CM_L \rvert$	Low-level common-mode transient immunity (See CMTI Testing)	Slew rate of GND vs. VSSA/B, INA and INB both are tied to GND or VCCI; V_{CM}=1000 V;	100			V/ns

(1) Parameters that has only typical values, are not production tested and guaranteed by design.

7.11 Thermal Derating Curves



Current in Each Channel with Both Channels Running Simultaneously

Figure 1. Thermal Derating Curve for Limiting Current Per VDE

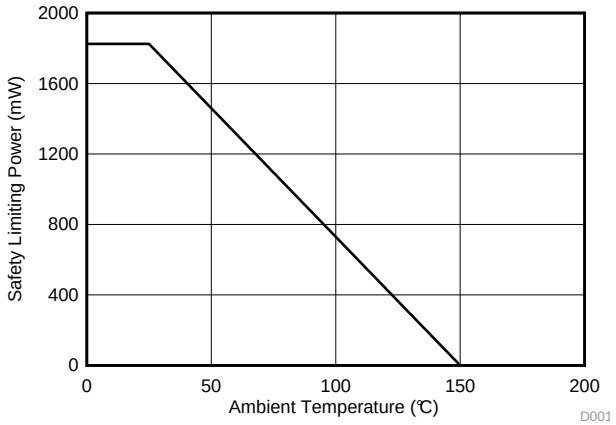
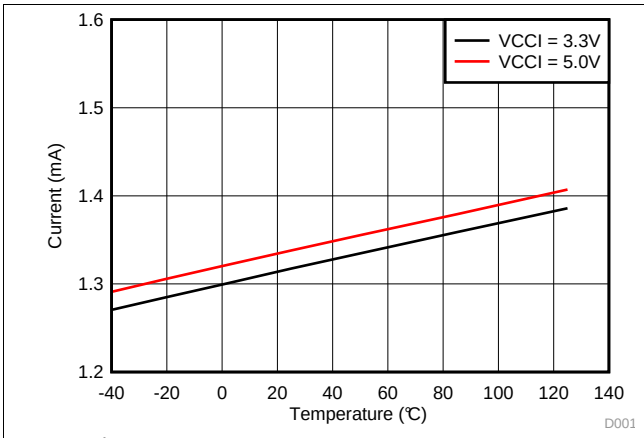


Figure 2. Thermal Derating Curve for Limiting Power Per VDE

7.12 Typical Characteristics

VDDA = VDDB = 12 V, VCCI = 3.3 V or 5.0 V, T_A = 25°C, C_L=0pF unless otherwise noted.



No Load INA = INB = GND

Figure 3. VCCI Quiescent Current

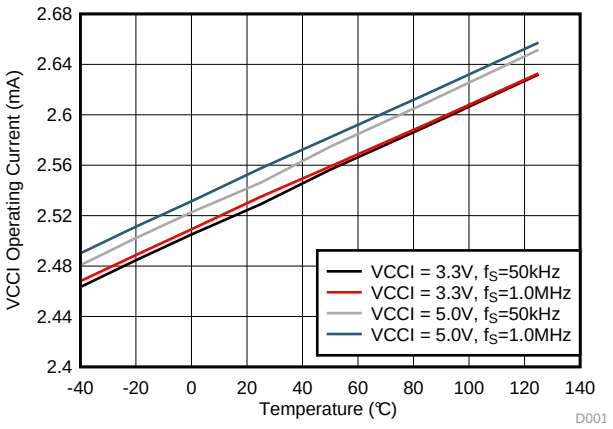


Figure 4. VCCI Operating Current - I_{VCCI}

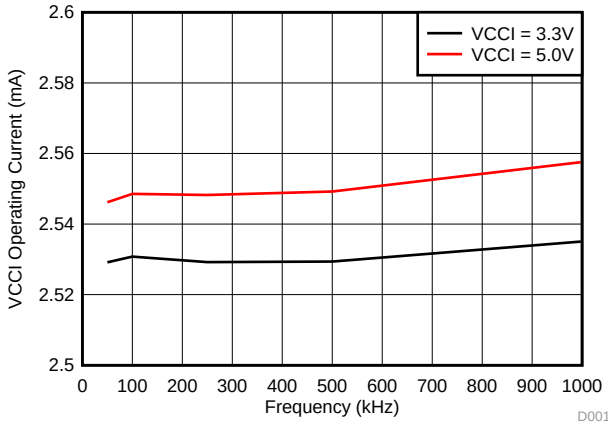
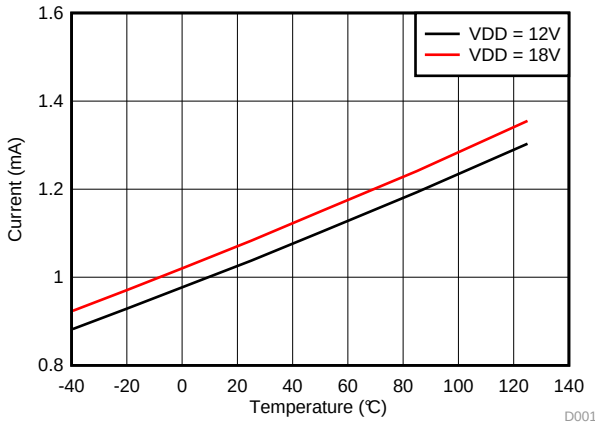
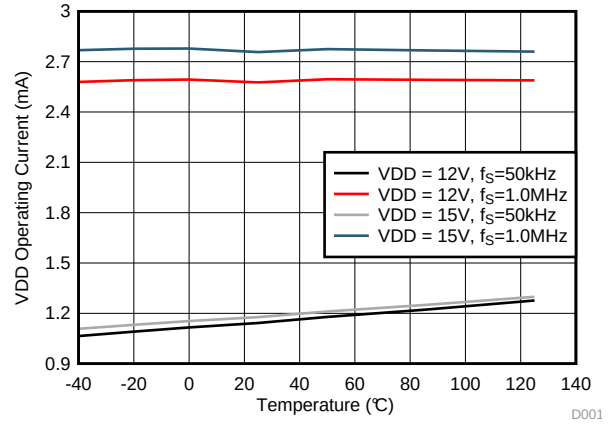


Figure 5. VCCI Operating Current vs. Frequency



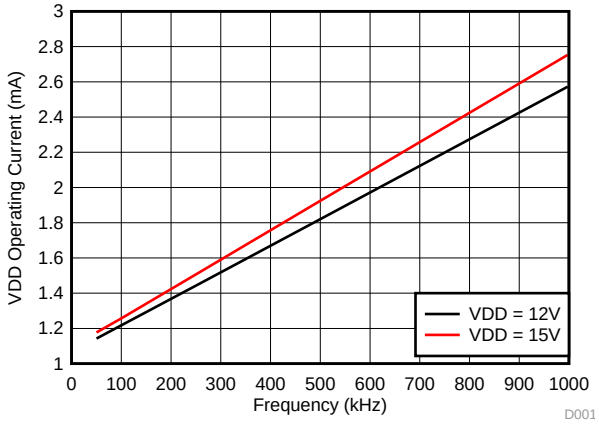
No Load INA = INB = GND

Figure 6. VDD Per Channel Quiescent Current (I_{VDDA}, I_{VDDB})



No Load

Figure 7. VDD Per Channel Operating Current - $I_{VDDA/B}$)



No Load INA and INB both switching

Figure 8. Per Channel Operating Current ($I_{VDDA/B}$) vs. Frequency

Copyright © 2017–2019, Texas Instruments Incorporated

Typical Characteristics (continued)

VDDA = VDDB = 12 V, VCCI = 3.3 V or 5.0 V, T_A = 25°C, C_L=0pF unless otherwise noted.

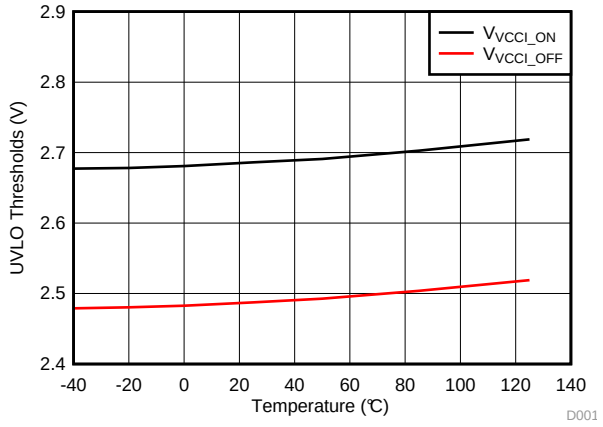


Figure 9. VCCI UVLO Threshold Voltage

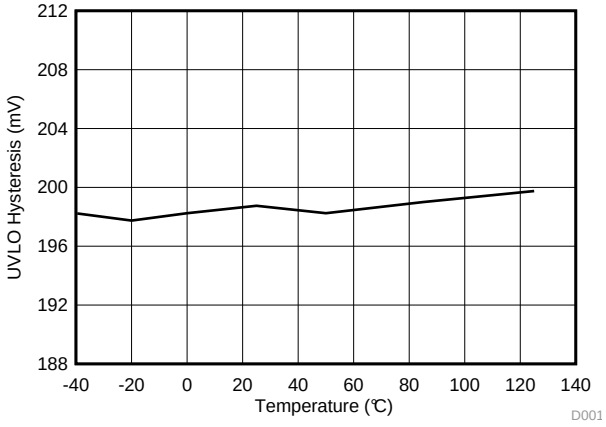


Figure 10. VCCI UVLO Threshold Hysteresis Voltage

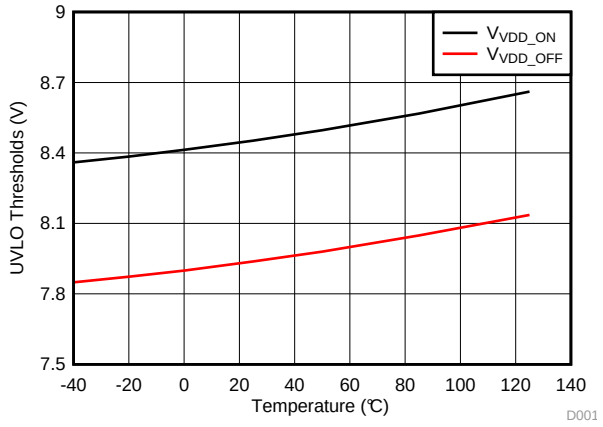


Figure 11. 8V VDD UVLO Threshold Voltage

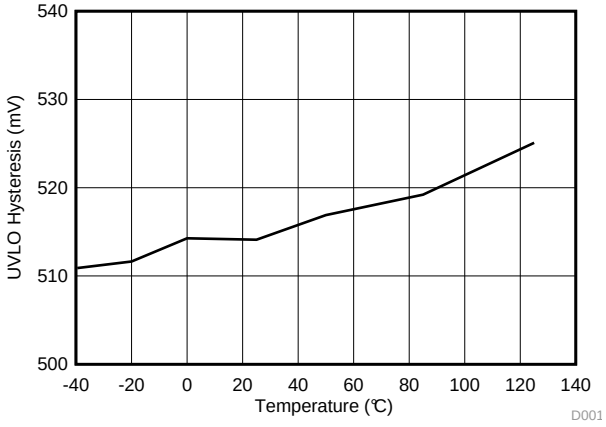


Figure 12. 8V VDD UVLO Threshold Hysteresis

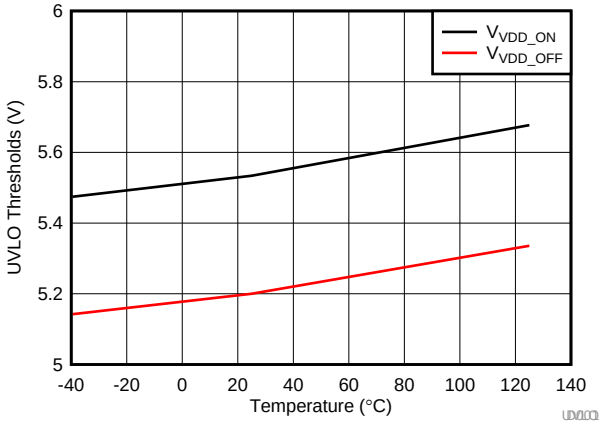


Figure 13. 5V VDD UVLO Threshold Voltage

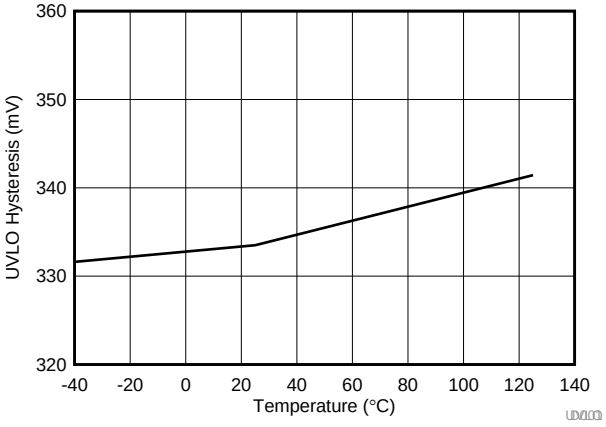


Figure 14. 5V VDD UVLO Threshold Hysteresis

Typical Characteristics (continued)

VDDA = VDDB = 12 V, VCCI = 3.3 V or 5.0 V, T_A = 25°C, C_L=0pF unless otherwise noted.

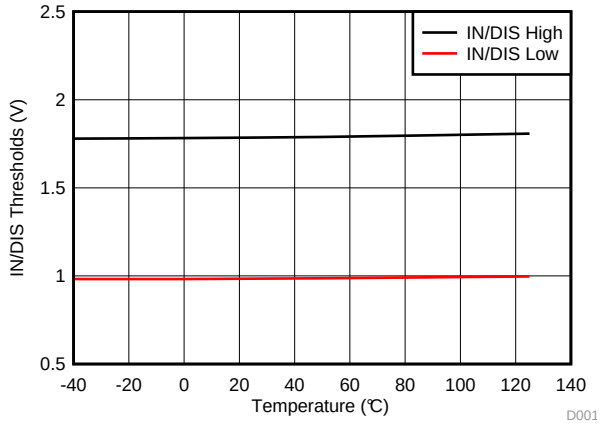


Figure 15. INA/INB/DIS High and Low Threshold Voltage

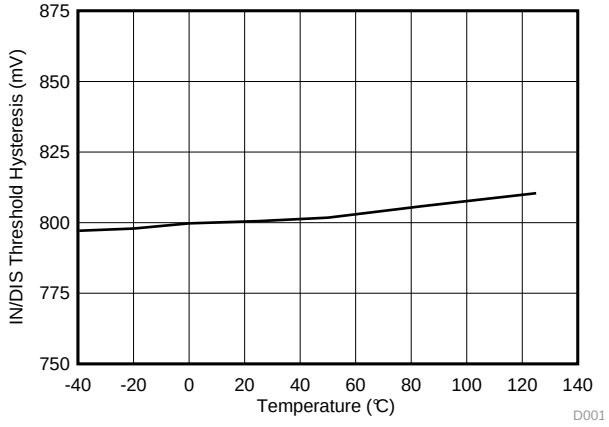


Figure 16. INA/INB/DIS High and Low Threshold Hysteresis

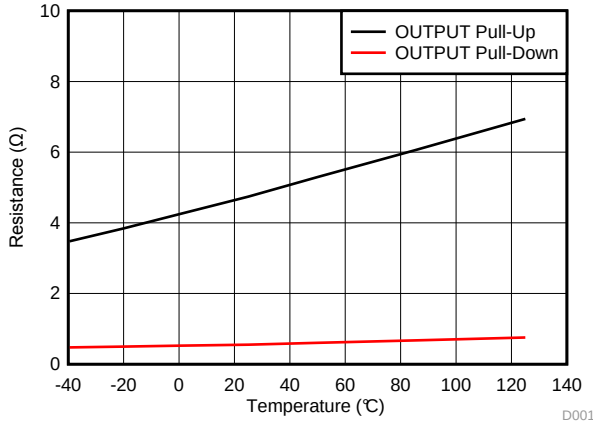


Figure 17. OUT Pullup and Pulldown Resistance

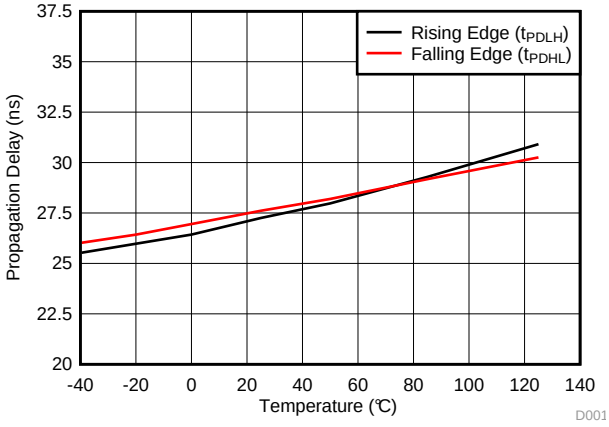


Figure 18. Propagation Delay, Rising and Falling Edge

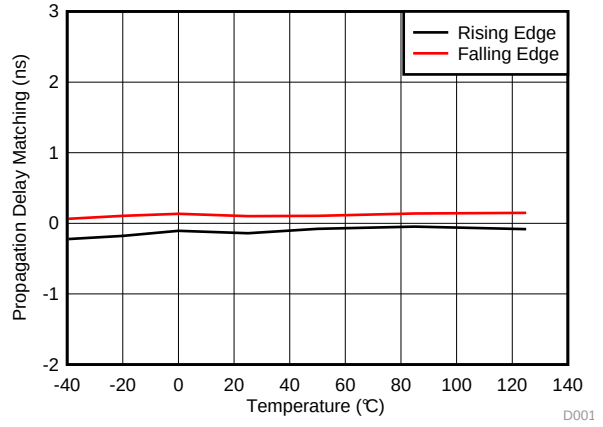
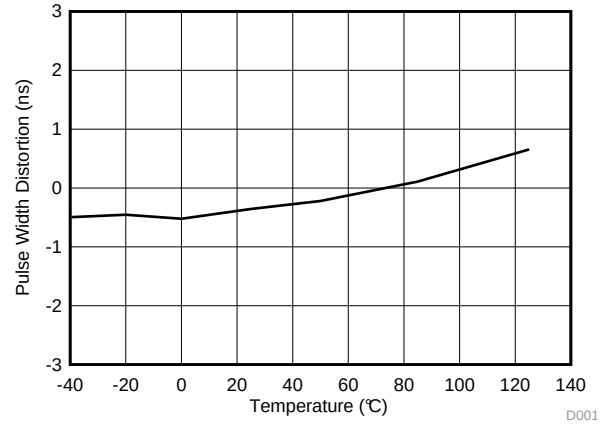


Figure 19. Propagation Delay Matching, Rising and Falling Edge



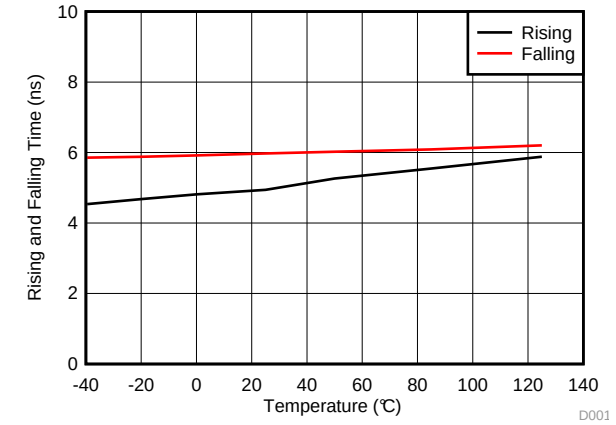
$t_{PDLH} - t_{PDHL}$

Figure 20. Pulse Width Distortion

Copyright © 2017–2019, Texas Instruments Incorporated

Typical Characteristics (continued)

VDDA = VDDB = 12 V, VCCI = 3.3 V or 5.0 V, T_A = 25°C, C_L=0pF unless otherwise noted.



C_L = 1.8 nF

Figure 21. Rise Time and Fall Time

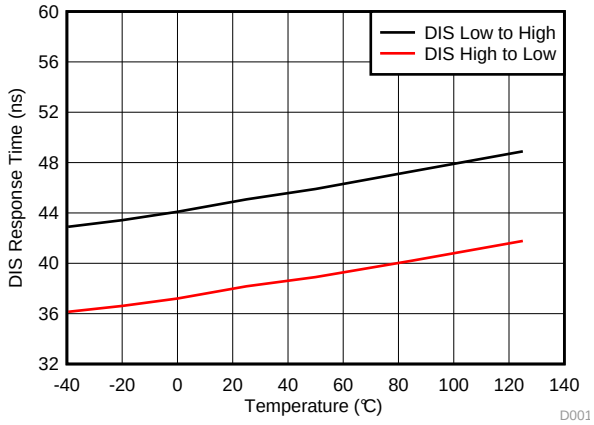


Figure 22. DISABLE Response Time

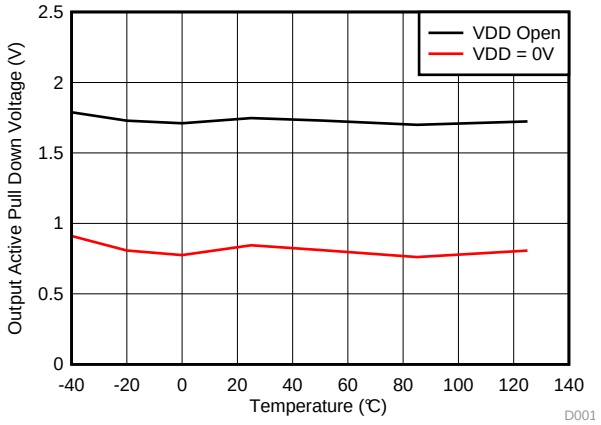


Figure 23. OUTPUT Active Pulldown Voltage

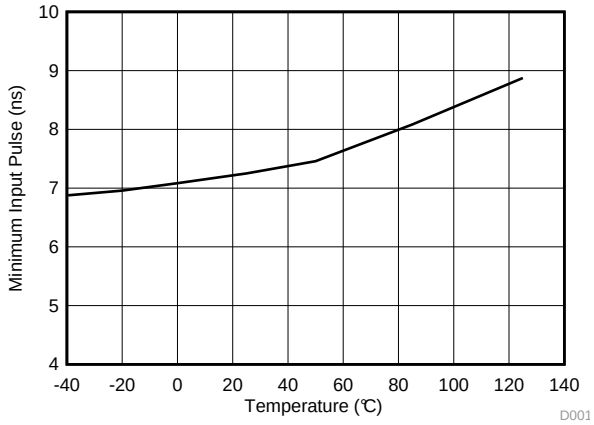


Figure 24. Minimum Pulse that Changes Output

8 Parameter Measurement Information

8.1 Minimum Pulses

A typical 5-ns deglitch filter removes small input pulses introduced by ground bounce or switching transients. To change the output stage on OUTA or OUTB, one has to assert longer pulses than $t_{PW(min)}$, typically 10 ns, to guarantee an output state change. see Figure 25 and Figure 26 for detailed information of the operation of deglitch filter.

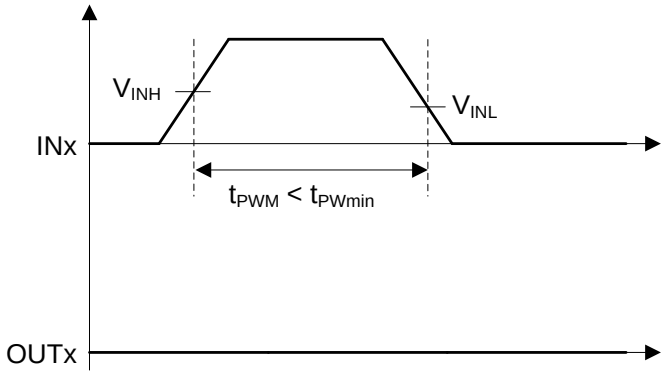


Figure 25. Deglitch Filter – Turn ON

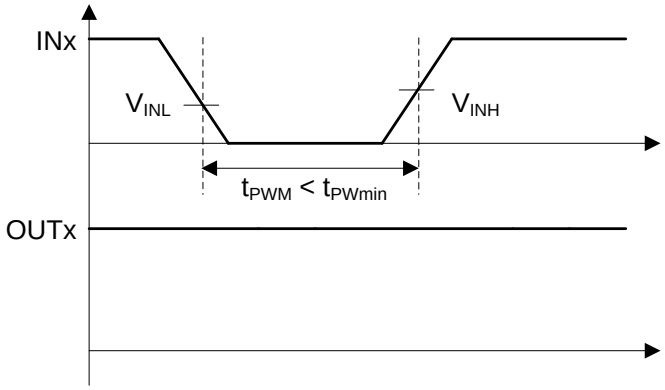


Figure 26. Deglitch Filter – Turn OFF

8.2 Propagation Delay and Pulse Width Distortion

Figure 27 shows how one calculates pulse width distortion (t_{PWD}) and delay matching (t_{DM}) from the propagation delays of channels A and B. It can be measured by ensuring that both inputs are in phase.

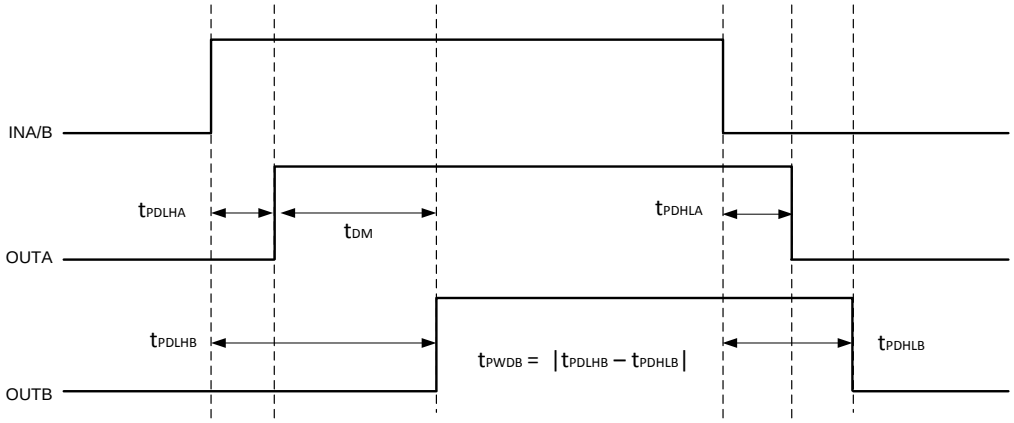


Figure 27. Delay Matching and Pulse Width Distortion

8.3 Rising and Falling Time

Figure 28 shows the criteria for measuring rising (t_{RISE}) and falling (t_{FALL}) times. For more information on how short rising and falling times are achieved see Output Stage

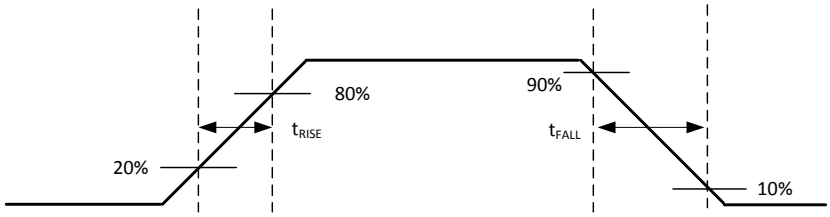


Figure 28. Rising and Falling Time Criteria

Copyright © 2017–2019, Texas Instruments Incorporated

8.4 Input and Disable Response Time

Figure 29 shows the response time of the disable function. For more information, see Disable Pin .

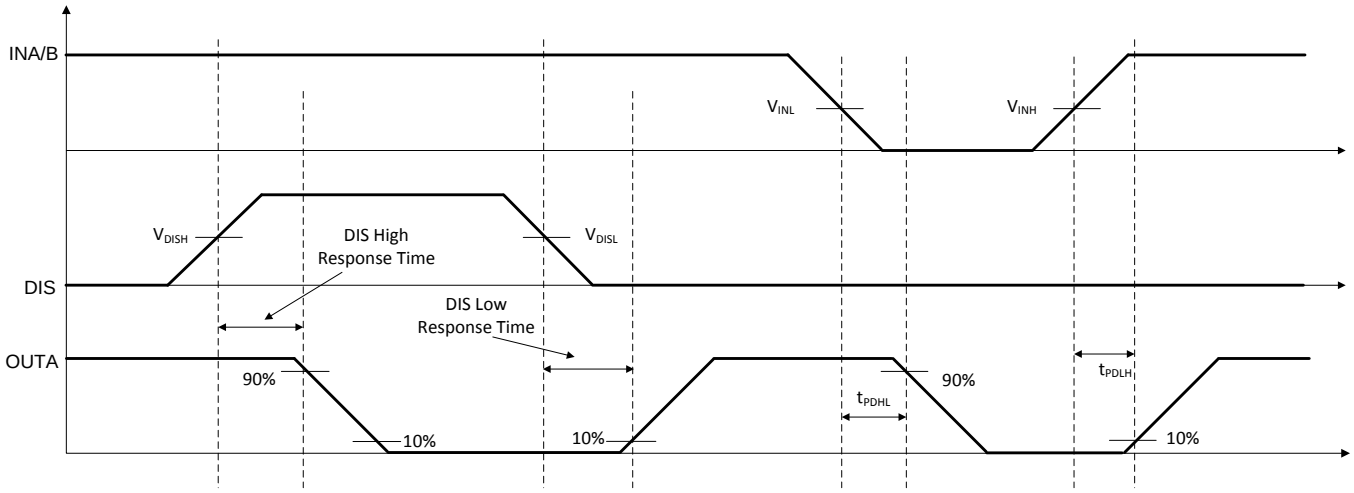


Figure 29. Disable Pin Timing

8.5 Power-up UVLO Delay to OUTPUT

Before the driver is ready to deliver a proper output state, there is a power-up delay from the UVLO rising edge to output and it is defined as $t_{VCCI+\ to\ OUT}$ for VCCI UVLO, which is 40 µs typically, and $t_{VDD+\ to\ OUT}$ for VDD UVLO, which is 22 µs typically. It is recommended to consider proper margin before launching PWM signal after the driver VCCI and VDD bias supply is ready. Figure 30 and Figure 31 show the power-up UVLO delay timing diagram for VCCI and VDD.

If INA or INB are active before VCCI or VDD have crossed above their respective on thresholds, the output will not update until $t_{VCCI+\ to\ OUT}$ or $t_{VDD+\ to\ OUT}$ after VCCI or VDD crossing its UVLO rising threshold. However, when either VCCI or VDD receive a voltage less than their respective off thresholds, there is <1µs delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during VCCI or VDD brownouts.

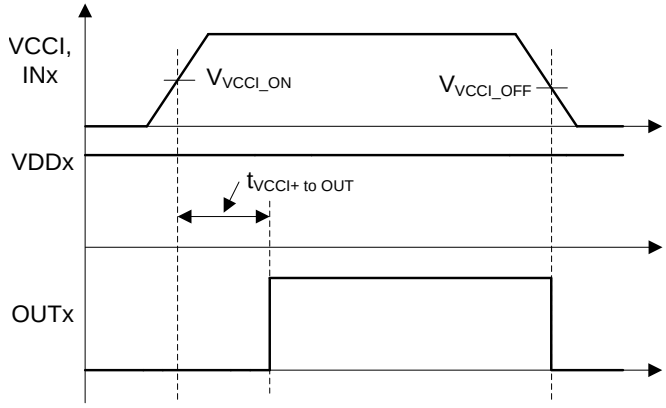


Figure 30. VCCI Power-up UVLO Delay

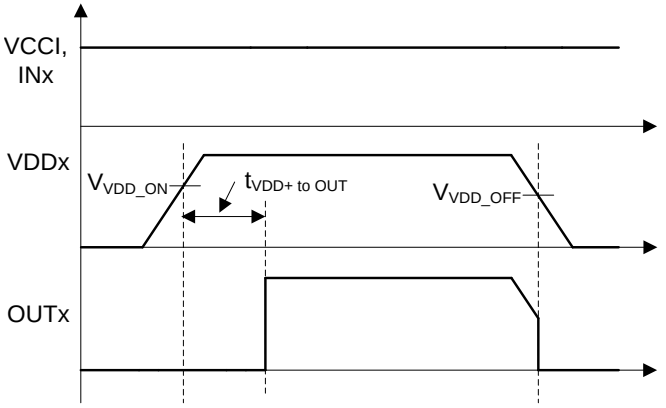
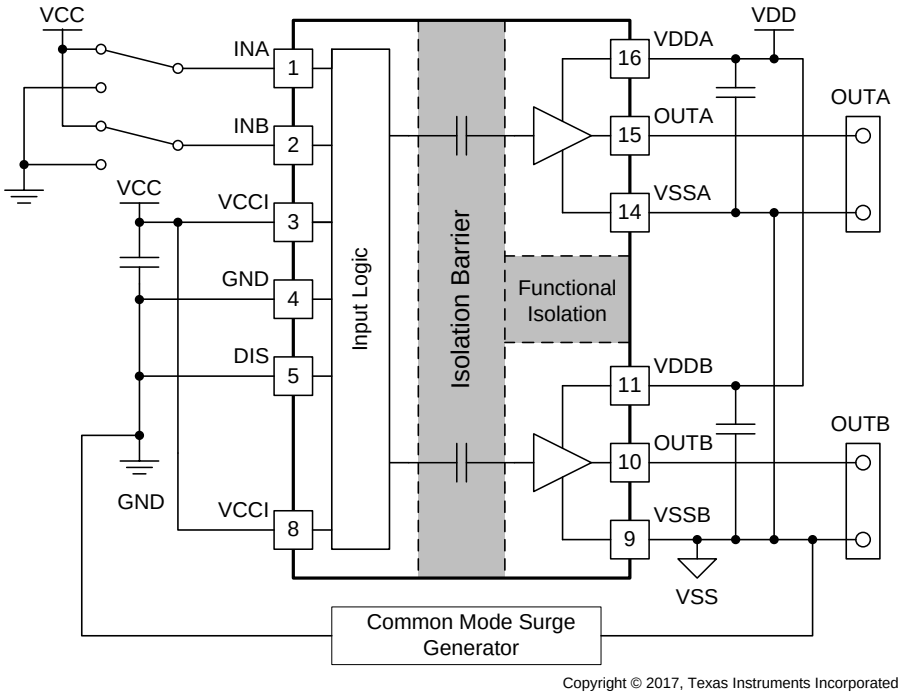


Figure 31. VDDA/B Power-up UVLO Delay

8.6 CMTI Testing

Figure 32 is a simplified diagram of the CMTI testing configuration.



Copyright © 2017, Texas Instruments Incorporated

Figure 32. Simplified CMTI Testing Setup

Copyright © 2017–2019, Texas Instruments Incorporated

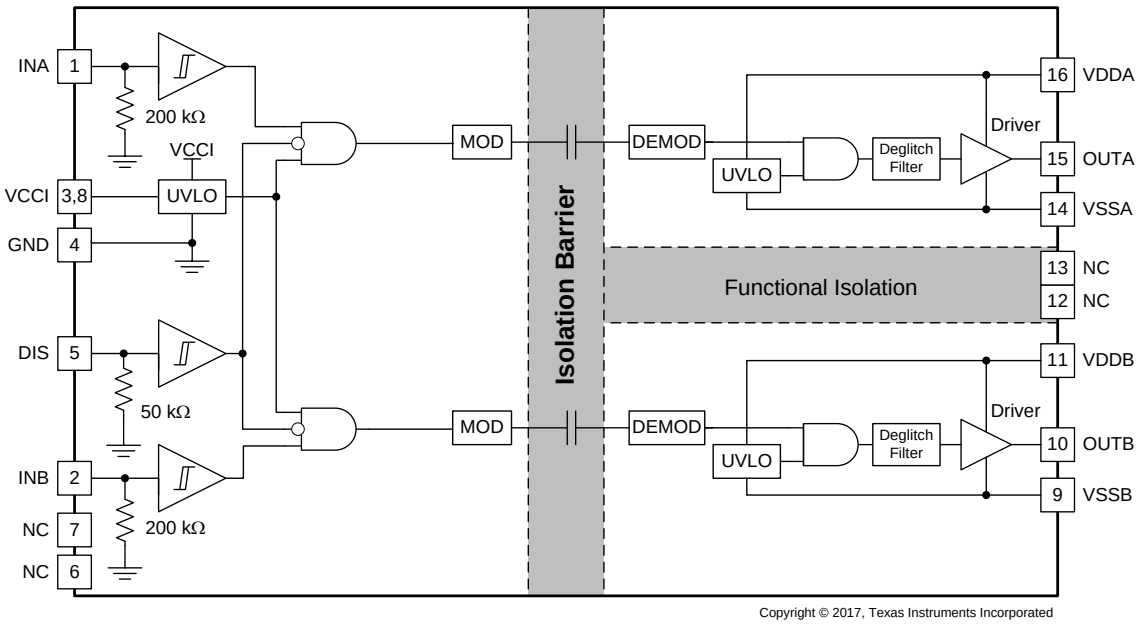
9 Detailed Description

9.1 Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA.

The UCC21220, UCC21220A are flexible dual gate drivers which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors. UCC21220 and UCC21220A have many features that allow it to integrate well with control circuitry and protect the gates it drives such as: disable pin, and under voltage lock out (UVLO) for both input and output voltages. The UCC21220, UCC21220A also hold its outputs low when the inputs are left open or when the input pulse is not wide enough. The driver inputs are CMOS and TTL compatible for interfacing with digital and analog power controllers alike. Each channel is controlled by its respective input pins (INA and INB), allowing full and independent control of each of the outputs.

9.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

9.3 Feature Description

9.3.1 VDD, VCCI, and Under Voltage Lock Out (UVLO)

The UCC21220 and UCC21220A have an internal under voltage lock out (UVLO) protection feature on the supply circuit blocks between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than V_{VDD_ON} at device start-up or lower than V_{VDD_OFF} after start-up, the VDD UVLO feature holds the effected output low, regardless of the status of the input pins (INA and INB).

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (Illustrated in Figure 33). In this condition, the upper PMOS is resistively held off by R_{Hi-Z} while the lower NMOS gate is tied to the driver output through R_{CLAMP}. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically around 1.5V, when no bias power is available.

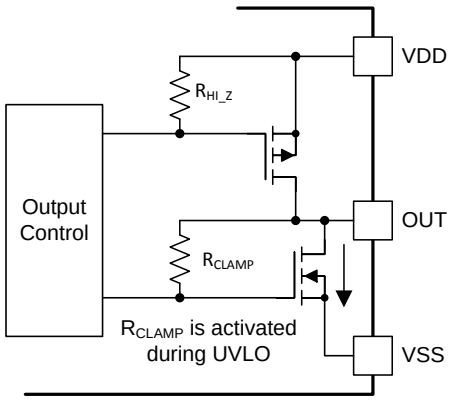


Figure 33. Simplified Representation of Active Pull Down Feature

The VDD UVLO protection has a hysteresis feature (V_{VDD_HYS}). This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept small drops in bias voltage, which is bound to happen when the device starts switching and operating current consumption increases suddenly.

The input side of the UCC21220 and UCC21220A also have an internal under voltage lock out (UVLO) protection feature. The device isn't active unless the voltage, VCCI, is going to exceed V_{VCCI_ON} on start up. And a signal will cease to be delivered when that pin receives a voltage less than V_{VCCI_OFF}. And, just like the UVLO for VDD, there is hystersis (V_{VCCI_HYS}) to ensure stable operation.

Table 1. VCCI UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	L	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	H	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	L	L	L

Copyright © 2017–2019, Texas Instruments Incorporated

Table 2. VDD UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VDD-VSS < V_{VDD_ON} during device start up	H	L	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	H	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	L	L	L

9.3.2 Input and Output Logic Table

Assume VCCI, VDDA, VDDB are powered up (see VDD, VCCI, and Under Voltage Lock Out (UVLO) for more information on UVLO operation modes), Table 3 shows the operation with INA, INB and DIS and the corresponding output state.

Table 3. INPUT/OUTPUT Logic Table(1)

INPUTS		DIS	OUTPUTS		NOTE
INA	INB		OUTA	OUTB	
L	L	L or Left Open	L	L	Disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting to a µC with distance.
L	H	L or Left Open	L	H	
H	L	L or Left Open	H	L	
H	H	L or Left Open	H	H	
Left Open	Left Open	L or Left Open	L	L	It is recommended to tie INA/INB to ground if not used to achieve better noise immunity.
X	X	H	L	L	-

(1) "X" means L, H or left open.

9.3.3 Input Stage

The input pins (INA, INB, and DIS) of UCC21220 and UCC21220A are based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V micro-controllers), since the UCC21220 and UCC21220A have a typical high threshold (V_{INAH}) of 1.8 V and a typical low threshold of 1 V, which vary little with temperature (see Figure 12 and Figure 16). A wide hysterisis (V_{INA_HYS}) of 0.8 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These resistors are typically 200 kΩ for INA/B and 50 kΩ for DIS (See Functional Block Diagram). However, it is still recommended to ground an input if it is not being used.

Since the input side of UCC21220 or UCC21220A are isolated from the output drivers, the input signal amplitude can be larger or smaller than VDD, provided that it doesn't exceed the recommended limit. This allows greater flexibility when integrating with control signal sources, and allows the user to choose the most efficient VDD for their MOSFET/IGBT gate. That said, the amplitude of any signal applied to INA or INB must *never* be at a voltage higher than VCCI.

Copyright © 2017–2019, Texas Instruments Incorporated

9.3.4 Output Stage

The UCC21220 and UCC21220A output stages feature a pull-up structure which delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *Pull-Up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET (R_{NMOS}) is approximately 1.47 Ω when activated.

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *Pull-Up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore the effective resistance of the UCC21220 and UCC21220A pull-up stage during this brief turn-on phase is much lower than what is represented by the R_{OH} parameter.

The pull-down structure of the UCC21220 and UCC21220A are composed of an N-channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. Both outputs of the UCC21220 and UCC21220A are capable of delivering 4-A peak source and 6-A peak sink current pulses. The output voltage swings between VDD and VSS provides rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out.

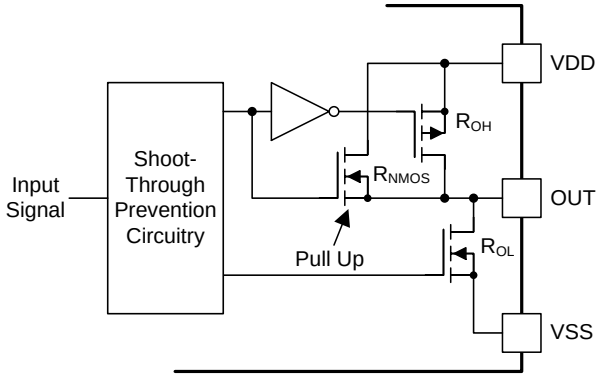


Figure 34. Output Stage

Copyright © 2017–2019, Texas Instruments Incorporated

9.3.5 Diode Structure in UCC21220 and UCC21220A

Figure 35 illustrates the multiple diodes involved in the ESD protection components. This provides a pictorial representation of the absolute maximum rating for the device.

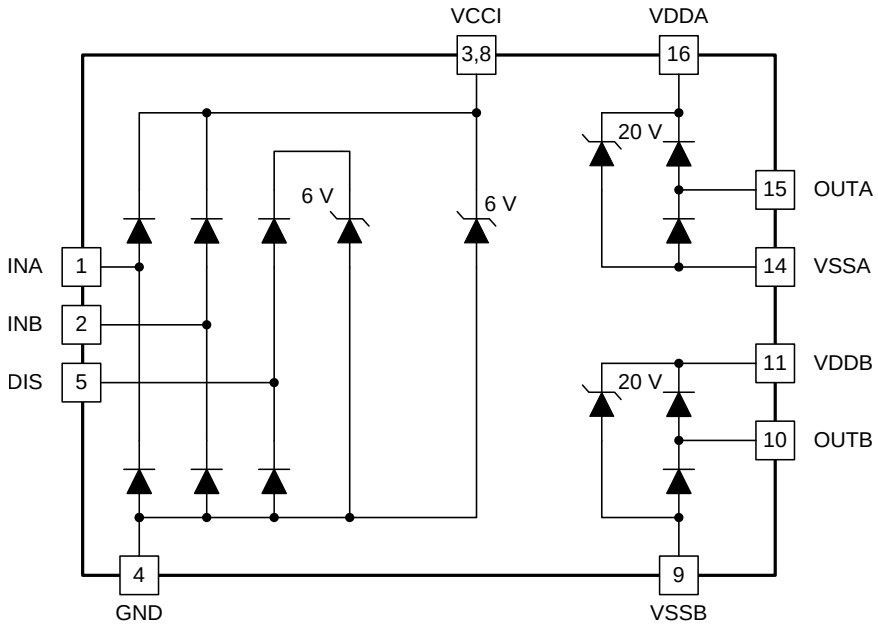


Figure 35. ESD Structure

9.4 Device Functional Modes

9.4.1 Disable Pin

Setting the DIS pin high shuts down both outputs simultaneously. Pull the DIS pin low (or left open) allows UCC21220 and UCC21220A to operate normally. The DIS pin is quite responsive, as far as propagation delay and other switching parameters are concerned (See Figure 22). The DIS pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to GND if the DIS pin is not used to achieve better noise immunity.

Copyright © 2017–2019, Texas Instruments Incorporated

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The UCC21220 and UCC21220A effectively combine both isolation and buffer-drive functions. The flexible, universal capability of the UCC21220 (with up to 5.5-V VCCI and 18-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or GaN transistor. With integrated components, advanced protection features (UVLO and disable) and optimized switching performance; the UCC21220 and UCC21220A enable designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

10.2 Typical Application

The circuit in Figure 36 shows a reference design with UCC21220 or UCC21220A driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications.

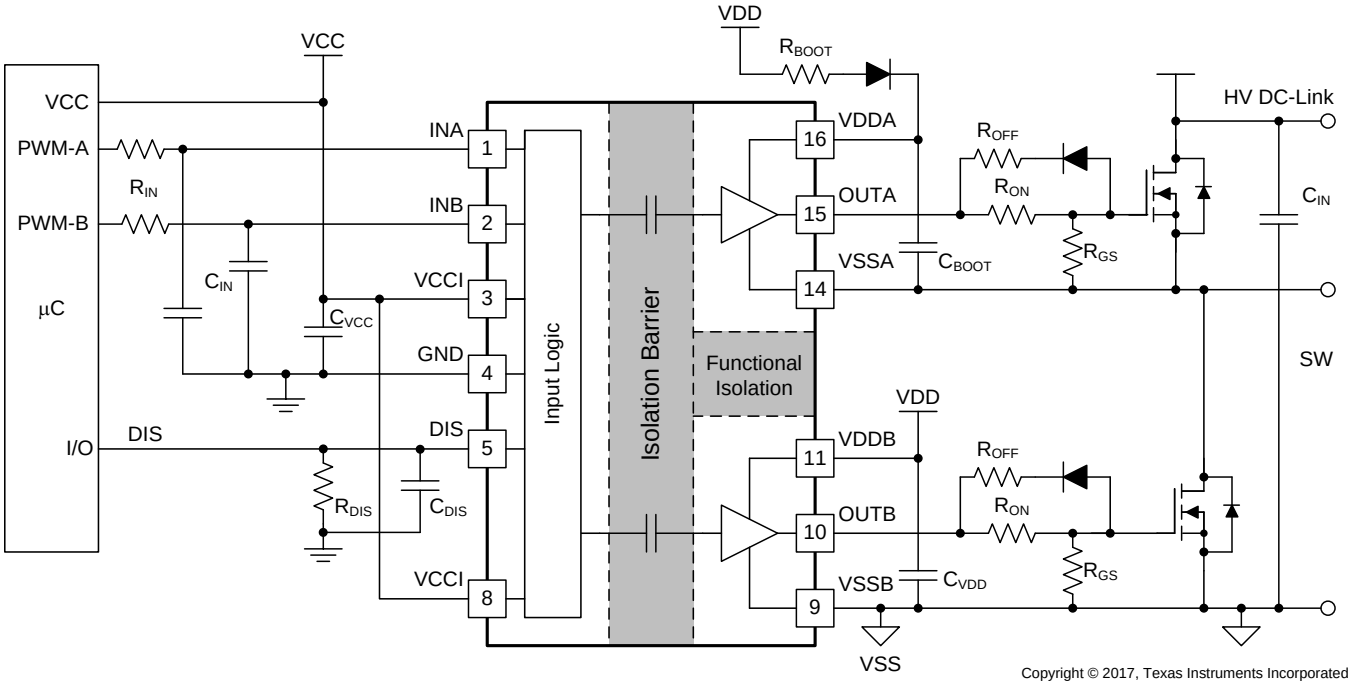


Figure 36. Typical Application Schematic

Copyright © 2017–2019, Texas Instruments Incorporated

Typical Application (continued)

10.2.1 Design Requirements

Table 4 lists reference design parameters for the example application: UCC21220 or UCC21220A driving 650-V MOSFETs in a high side-low side configuration.

Table 4. UCC21220 and UCC21220A Design Requirements

PARAMETER	VALUE	UNITS
Power transistor	IPP65R150CFD	-
VCC	5.0	V
VDD	12	V
Input signal amplitude	3.3	V
Switching frequency (f_s)	100	kHz
DC link voltage	400	V

10.2.2 Detailed Design Procedure

10.2.2.1 Designing INA/INB Input Filter

It is recommended that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input R_{IN}-C_{IN} filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an R_{IN} in the range of 0 Ω to100 Ω and a C_{IN} between 10 pF and 100 pF. In the example, an R_{IN} = 51 Ω and a C_{IN} = 33 pF are selected, with a corner frequency of approximately 100 MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

10.2.2.2 Select External Bootstrap Diode and its Series Resistor

The bootstrap capacitor is charged by VDD through an external bootstrap diode every cycle when the low side transistor turns on. Charging the capacitor involves high-peak currents, and therefore transient power dissipation in the bootstrap diode may be significant. Conduction loss also depends on the diode's forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

When selecting external bootstrap diodes, it is recommended that one chose high voltage, fast recovery diodes or SiC Schottky diodes with a low forward voltage drop and low junction capacitance in order to minimize the loss introduced by reverse recovery and related grounding noise bouncing. In the example, the DC-link voltage is 400 V_{DC}. The voltage rating of the bootstrap diode should be higher than the DC-link voltage with a good margin. Therefore, a 600-V ultrafast diode, MURA160T3G, is chosen in this example.

A bootstrap resistor, R_{BOOT}, is used to reduce the inrush current in D_{BOOT} and limit the ramp up slew rate of voltage of VDDA-VSSA during each switching cycle, especially when the VSSA(SW) pin has an excessive negative transient voltage. The recommended value for R_{BOOT} is between 1 Ω and 20 Ω depending on the diode used. In the example, a current limiting resistor of 2.2 Ω is selected to limit the inrush current of bootstrap diode. The estimated worst case peak current through D_{Boot} is,

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{BDF}}{R_{Boot}} = \frac{12V - 1.5V}{2.7\Omega} \approx 4A \quad (1)$$

where

- V_{BDF} is the estimated bootstrap diode forward voltage drop around 4 A.

10.2.2.3 Gate Driver Output Resistor

The external gate driver resistors, R_{ON}/R_{OFF}, are used to:

1. Limit ringing caused by parasitic inductances/capacitances.
2. Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength, i.e. peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI).

As mentioned in Output Stage, the UCC21220 and UCC21220A have a pull-up structure with a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The combined peak source current is 4 A. Therefore, the peak source current can be predicted with:

$$I_{OA+} = \min\left(4A, \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right) \quad (2)$$

$$I_{OB+} = \min\left(4A, \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right)$$

where

- R_{ON}: External turn-on resistance.
- R_{GFET_INT}: Power transistor internal gate resistance, found in the power transistor datasheet.
- I_{O+} = Peak source current – The minimum value between 4 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance. (3)

In this example:

$$I_{OA+} = \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{12V - 0.8V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 1.5\Omega} \approx 2.3A \quad (4)$$

$$I_{OB+} = \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{12V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 1.5\Omega} \approx 2.5A \quad (5)$$

Therefore, the high-side and low-side peak source current is 2.3 A and 2.5 A respectively. Similarly, the peak sink current can be calculated with:

$$I_{OA-} = \min\left(6A, \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}}\right) \quad (6)$$

$$I_{OB-} = \min\left(6A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}}\right)$$

where

- R_{OFF}: External turn-off resistance, R_{OFF}=0 in this example;
- V_{GDF}: The anti-parallel diode forward voltage drop which is in series with R_{OFF}. The diode in this example is an MSS1P4.
- I_{O-}: Peak sink current – the minimum value between 6 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance. (7)

Copyright © 2017–2019, Texas Instruments Incorporated

In this example,

$$I_{OA-} = \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{12V - 0.8V - 0.85V}{0.55\Omega + 0\Omega + 1.5\Omega} \approx 5.0A \quad (8)$$

$$I_{OB-} = \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{12V - 0.85V}{0.55\Omega + 0\Omega + 1.5\Omega} \approx 5.4A \quad (9)$$

Therefore, the high-side and low-side peak sink current is 5.0 A and 5.4A respectively.

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, it is strongly recommended that the gate driver loop should be minimized. On the other hand, the peak source/sink current is dominated by loop parasitics when the load capacitance (C_{ISS}) of the power transistor is very small (typically less than 1 nF), because the rising and falling time is too small and close to the parasitic ringing period.

10.2.2.4 Estimating Gate Driver Power Loss

The total loss, P_G, in the gate driver subsystem includes the power losses of the UCC21220 and UCC21220A (P_{GD}) and the power losses in the peripheral circuitry, such as the external gate drive resistor. Bootstrap diode loss is not included in P_G and not discussed in this section.

P_{GD} is the key power loss which determines the thermal safety-related limits of the UCC21220 and UCC21220A, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. P_{GDQ} is measured on the bench with no load connected to OUTA and OUTB at a given VCCI, VDDA/VDDB, switching frequency and ambient temperature. Figure 5 and Figure 8shows the operating current consumption vs. operating frequency with no load. In this example, V_{VCCI} = 5 V and V_{VDD} = 12 V. The current on each power supply, with INA/INB switching from 0 V to 3.3 V at 100 kHz is measured to be I_{VCCI} ≈ 2.5 mA, and I_{VDDA} = I_{VDDB} ≈ 1.5 mA. Therefore, the P_{GDQ} can be calculated with

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{DDA} + V_{VDDB} \times I_{DDB} = 50mW \quad (10)$$

The second component is switching operation loss, P_{GDO}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Total dynamic loss due to load switching, P_{GSW}, can be estimated with

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW}$$

where

- Q_G is the gate charge of the power transistor. (11)

If a split rail is used to turn on and turn off, then VDD is going to be equal to difference between the positive rail to the negative rail.

So, for this example application:

$$P_{GSW} = 2 \times 12V \times 100nC \times 100kHz = 240mW \quad (12)$$

Q_G represents the total gate charge of the power transistor switching 480 V at 14 A provided by the datasheet, and is subject to change with different testing conditions. The UCC21220 and UCC21220A gate driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} will be equal to P_{GSW} if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside the UCC21220 and UCC21220A. If there are external turn-on and turn-off resistances, the total loss will be distributed between the gate driver pull-up/down resistances and external gate resistances. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4 A/6 A, however, it will be non-linear if the source/sink current is saturated. Therefore, P_{GDO} is different in these two scenarios.

Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2} \times \left(\frac{R_{OH} \parallel R_{NMOS}}{R_{OH} \parallel R_{NMOS} + R_{ON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} \parallel R_{ON} + R_{GFET\_Int}} \right) \tag{13}$$

In this design example, all the predicted source/sink currents are less than 4 A/6 A, therefore, the UCC21220 and UCC21220A gate driver loss can be estimated with:

$$P_{GDO} = \frac{240\text{mW}}{2} \times \left(\frac{5\Omega \parallel 1.47\Omega}{5\Omega \parallel 1.47\Omega + 2.2\Omega + 1.5\Omega} + \frac{0.55\Omega}{0.55\Omega + 0\Omega + 1.5\Omega} \right) \approx 60\text{mW} \tag{14}$$

Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = 2 \times f_{SW} \times \left[4\text{A} \times \int_0^{T_{R\_Sys}} \left(V_{DD} - V_{OUTA/B}(t) \right) dt + 6\text{A} \times \int_0^{T_{F\_Sys}} V_{OUTA/B}(t)\, dt \right]$$

where

- $V_{OUTA/B}(t)$ is the gate driver OUTA and OUTB pin voltage during the turn on and off transient, and it can be simplified that a constant current source (4 A at turn-on and 6 A at turn-off) is charging/discharging a load capacitor. Then, the $V_{OUTA/B}(t)$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted. (15)

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the P_{GDO} will be a combination of Case 1 and Case 2, and the equations can be easily identified for the pull-up and pull-down based on the above discussion. Therefore, total gate driver loss dissipated in the gate driver UCC21220 and UCC21220A, P_{GD}, is:

$$P_{GD} = P_{GDQ} + P_{GDO} \tag{16}$$

which is equal to 127 mW in the design example.

10.2.2.5 Estimating Junction Temperature

The junction temperature (T_J) of the UCC21220 and UCC21220A can be estimated with:

$$T_J = T_C + \Psi_{JT} \times P_{GD}$$

where

- T_C is the UCC21220 and UCC21220A case-top temperature measured with a thermocouple or some other instrument, ψ_{JT} is the junction-to-top characterization parameter from the Thermal Information table. Importantly, ψ_{JT} is developed based on JEDEC standard PCB board and it is subject to change when the PCB board layout is different. For more information, please visit application report - semiconductor and IC package thermal metrics. (17)

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\Theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). $R_{\Theta JC}$ can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heatsink is applied to an IC package. In all other cases, use of $R_{\Theta JC}$ will inaccurately

Copyright © 2017–2019, Texas Instruments Incorporated

estimate the true junction temperature. Ψ_{JT} is experimentally derived by assuming that the amount of energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimates can be made accurately to within a few degrees Celsius. For more information, see the Layout Guidelines and Semiconductor and IC Package Thermal Metrics application report.

10.2.2.6 Selecting VCCI, VDDA/B Capacitor

Bypass capacitors for VCCI, VDDA, and VDDB are essential for achieving reliable performance. It is recommended that one choose low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15 V_{DC} is applied.

10.2.2.6.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 25-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1 µF, should be placed in parallel with the MLCC.

10.2.2.6.2 Selecting a VDDA (Bootstrap) Capacitor

A VDDA capacitor, also referred to as a *bootstrap capacitor* in bootstrap power supply configurations, allows for gate drive current transients up to 6 A, and needs to maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with

$$Q_{Total} = Q_G + \frac{I_{VDD}\,@100kHz\,(\text{No Load})}{f_{SW}} = 100nC + \frac{1.5mA}{100kHz} = 115nC \quad (18)$$

where

- Q_G: Gate charge of the power transistor.
- I_{VDD}: The channel self-current consumption with no load at 100kHz.
-

Therefore, the absolute minimum C_{Boot} requirement is:

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{VDDA}} = \frac{115nC}{0.5V} = 230nF \quad (19)$$

where

- ΔV_{VDDA} is the voltage ripple at VDDA, which is 0.5 V in this example.

In practice, the value of C_{Boot} is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients. Therefore, it is recommended to include a safety-related margin in the C_{Boot} value and place it as close to the VDD and VSS pins as possible. A 50-V 1-µF capacitor is chosen in this example.

$$C_{Boot}=1\mu F \quad (20)$$

To further lower the AC impedance for a wide frequency range, it is recommended to have bypass capacitor with a low capacitance value, in this example a 100 nF, in parallel with C_{Boot} to optimize the transient performance.

NOTE

Too large C_{BOOT} is not good. C_{BOOT} may not be charged within the first few cycles and V_{BOOT} could stay below UVLO. As a result, the high-side FET does not follow input signal command. Also during initial C_{BOOT} charging cycles, the bootstrap diode has highest reverse recovery current and losses.

Copyright © 2017–2019, Texas Instruments Incorporated

10.2.2.6.3 Select a VDDB Capacitor

Chanel B has the same current requirements as Channel A, Therefore, a VDDB capacitor (Shown as C_{VDD} in Figure 36) is needed. In this example with a bootstrap configuration, the VDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50-V, 10-µF MLCC and a 50-V, 220-nF MLCC are chosen for C_{VDD}. If the bias power supply output is a relatively long distance from the VDDB pin, a tantalum or electrolytic capacitor with a value over 10 µF, should be used in parallel with C_{VDD}.

10.2.2.7 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by non-ideal PCB layout and long package leads (e.g. TO-220 and TO-247 type packages), there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

Figure 37 shows the first example with negative bias turn-off on the channel-A driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply, V_A, is equal to 17 V, the turn-off voltage will be –5.1 V and turn-on voltage will be 17 V – 5.1 V ≈ 12 V. The channel-B driver circuit is the same as channel-A, therefore, this configuration needs two power supplies for a half-bridge configuration, and there will be steady state power consumption from R_Z.

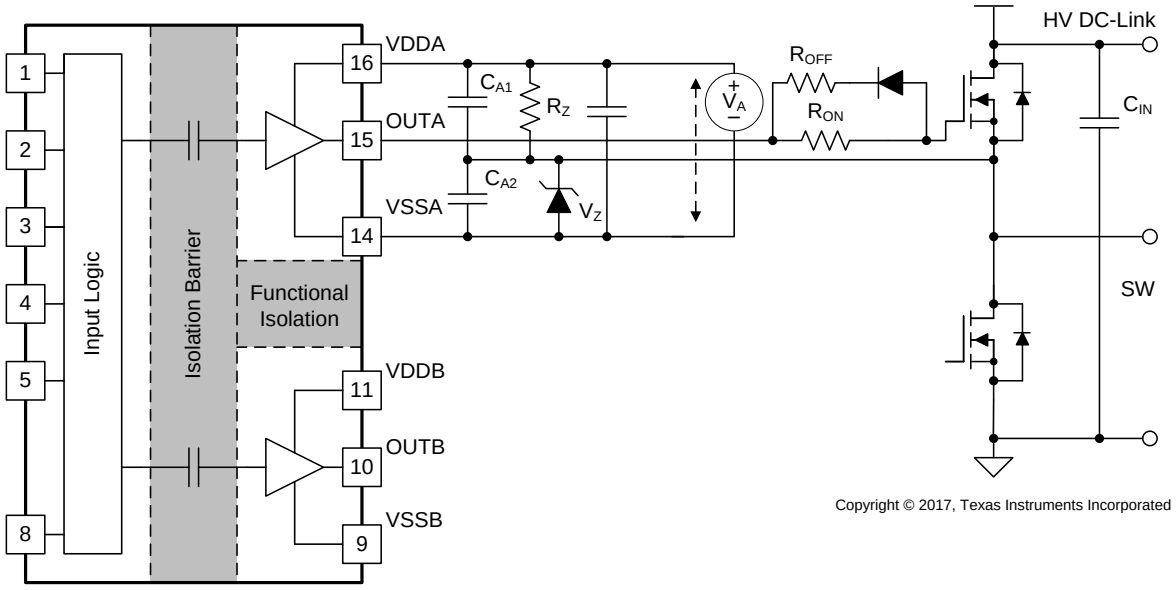


Figure 37. Negative Bias with Zener Diode on Iso-Bias Power Supply Output

Copyright © 2017–2019, Texas Instruments Incorporated

Figure 38 shows another example which uses two supplies (or single-input-double-output power supply). Power supply V_{A+} determines the positive drive output voltage and $V_{A–}$ determines the negative turn-off voltage. The configuration for channel B is the same as channel A. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

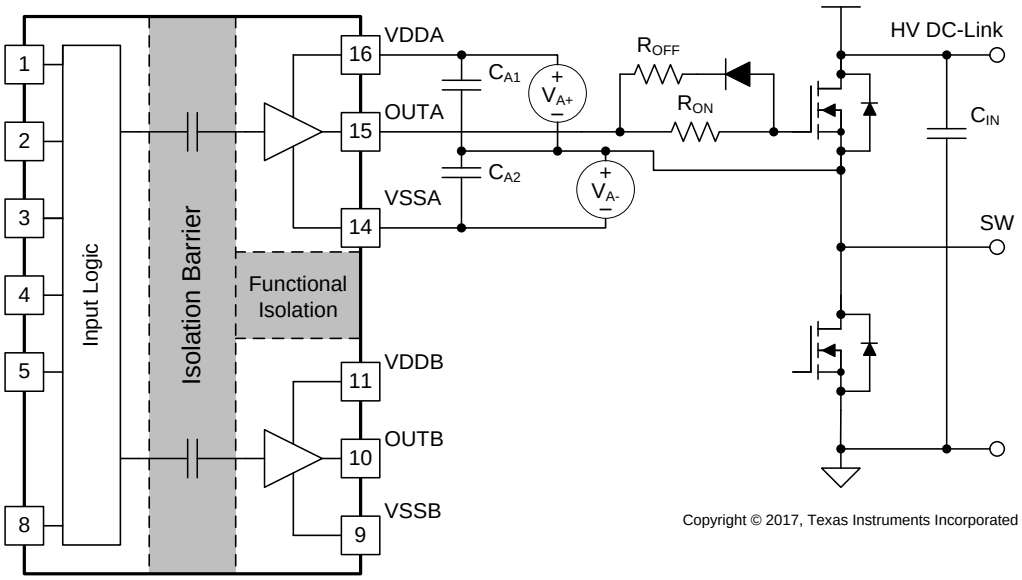


Figure 38. Negative Bias with Two Iso-Bias Power Supplies

The last example, shown in Figure 39, is a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, this solution has limitations:

1. The negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (~50%) such as variable frequency resonant convertors or phase shift convertors which favor this solution.
2. The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means the low side switch must turn-on or have free-wheeling current on the body (or anti-parallel) diode for a certain period during each switching cycle to refresh the bootstrap capacitor. Therefore, a 100% duty cycle for the high side is not possible unless there is a dedicated power supply for the high side, like in the other two example circuits.

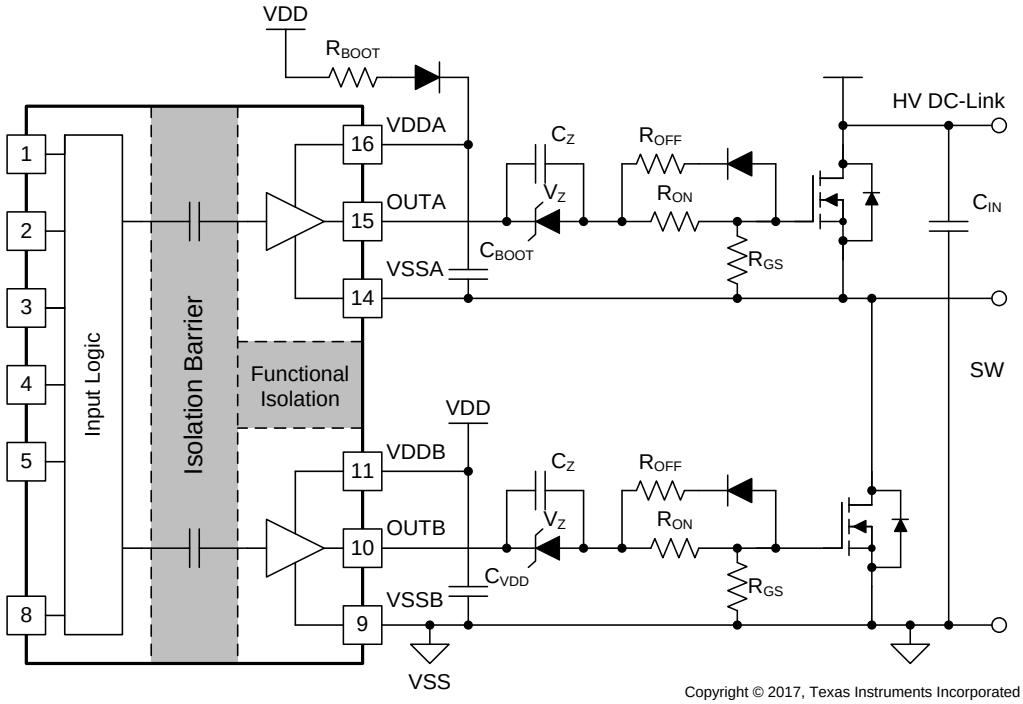


Figure 39. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path

Copyright © 2017–2019, Texas Instruments Incorporated

10.2.3 Application Curves

Figure 40 and Figure 41 shows the bench test waveforms for the design example shown in Figure 36 under these conditions: VCC = 5.0 V, VDD = 12 V, f_{SW} = 100 kHz, $V_{DC\text{-}Link}$ = 400 V.

Channel 1 (Yellow): INA pin signal.

Channel 2 (Blue): INB pin signal.

Channel 3 (Pink): Gate-source signal on the high side power transistor.

Channel 4 (Green): Gate-source signal on the low side power transistor.

In Figure 40, INA and INB are sent complimentary 3.3-V, 20%/80% duty-cycle signals with 200ns deadtime. The gate drive signals on the power transistor have a 200-ns dead time with 400V high voltage on the DC-Link, shown in the measurement section of Figure 40. Note that with high voltage present, lower bandwidth differential probes are required, which limits the achievable accuracy of the measurement.

Figure 41 shows a zoomed-in version of the waveform of Figure 40, with measurements for propagation delay and deadtime. Importantly, the output waveform is measured between the power transistors' gate and source pins, and is not measured directly from the driver's OUTA and OUTB pins.

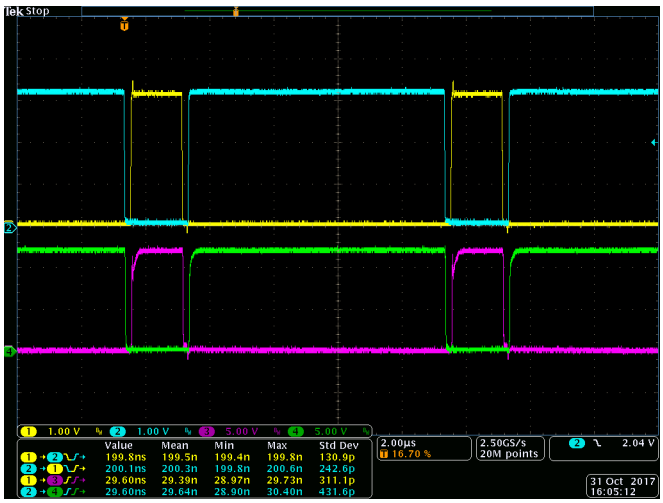


Figure 40. Bench Test Waveform for INA/B and OUTA/B

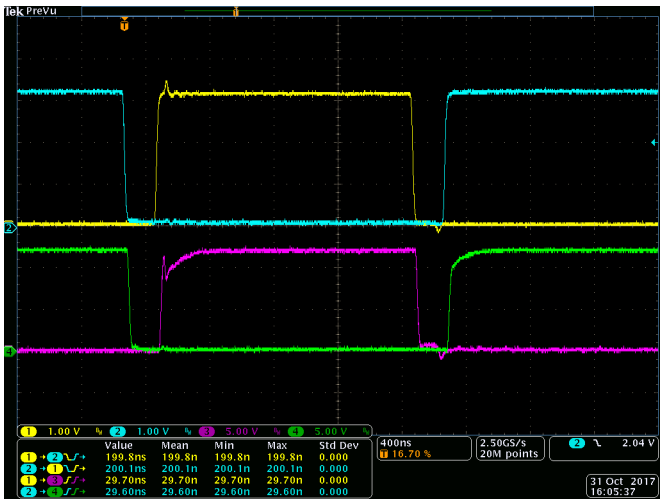


Figure 41. Zoomed-In bench-test waveform

11 Power Supply Recommendations

The recommended input supply voltage (VCCI) for UCC21220 and UCC21220A is between 3 V and 5.5 V. The output bias supply voltage (VDDA/VDDB) range from 9.2V to 18V. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of each device. One mustn't let VDD or VCCI fall below their respective UVLO thresholds (For more information on UVLO see VDD, VCCI, and Under Voltage Lock Out (UVLO)). The upper end of the VDDA/VDDB range depends on the maximum gate voltage of the power device being driven by UCC21220 and UCC21220A. The UCC21220 and UCC21220A have a recommended maximum VDDA/VDDB of 18 V.

A local bypass capacitor should be placed between the VDD and VSS pins. This capacitor should be positioned as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is further suggested that one place two such capacitors: one with a value of ≈10-µF for device biasing, and an additional ≤100-nF capacitor in parallel for high frequency filtering..

Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of UCC21220 and UCC21220A, this bypass capacitor has a minimum recommended value of 100 nF.

Copyright © 2017–2019, Texas Instruments Incorporated

12 Layout

12.1 Layout Guidelines

Consider these PCB layout guidelines for in order to achieve optimum performance for the UCC21220 and UCC21220A.

12.1.1 Component Placement Considerations

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSSA (HS) pin, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- It is recommended to bypass using a ≥1-nF low ESR/ESL capacitor, C_{DIS}, close to DIS pin when connecting to a μC with distance

12.1.2 Grounding Considerations

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

12.1.3 High-Voltage Considerations

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC21220 and UCC21220A isolation performance.
- For half-bridge, or high-side/low-side configurations, one should try to increase the clearance distance of the PCB layout between the high and low-side PCB traces.

12.1.4 Thermal Considerations

- A large amount of power may be dissipated by the UCC21220 and UCC21220A if the driving voltage is high, the load is heavy, or the switching frequency is high (Refer to Estimating Gate Driver Power Loss for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VDDA, VDDB, VSSA and VSSB pins is recommended, with priority on maximizing the connection to VSSA and VSSB (See Figure 43 and Figure 44). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. Ensure that no traces or coppers from different high-voltage planes overlap.

Copyright © 2017–2019, Texas Instruments Incorporated

12.2 Layout Example

Figure 42 shows a 2-layer PCB layout example with the signals and key components labeled.

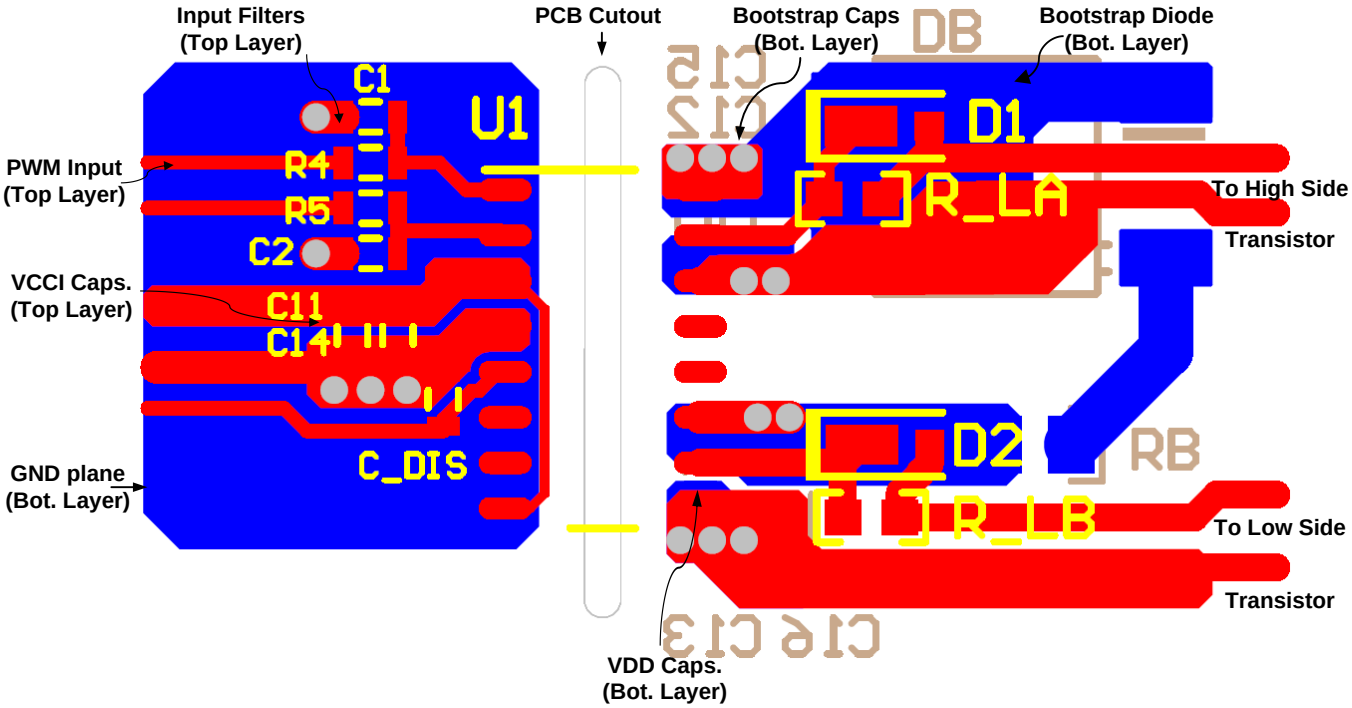


Figure 42. Layout Example

Figure 43 and Figure 44 shows top and bottom layer traces and copper.

NOTE

There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.

PCB traces between the high-side and low-side gate drivers in the output stage are increased to maximize the creepage distance for high-voltage operation, which will also minimize cross-talk between the switching node VSSA (SW), where high dv/dt may exist, and the low-side gate drive due to the parasitic capacitance coupling.

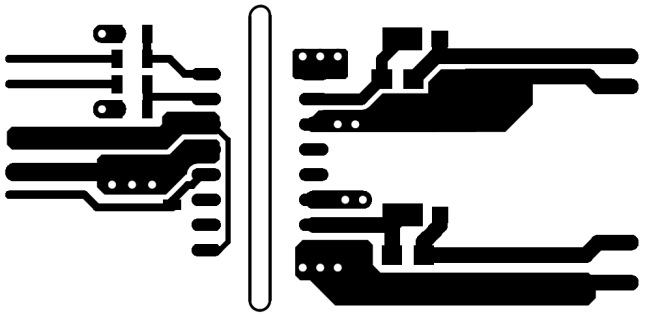


Figure 43. Top Layer Traces and Copper

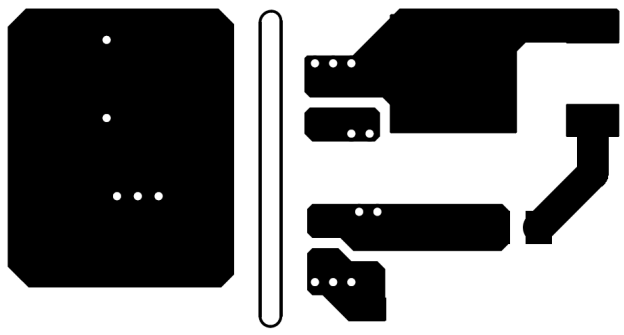


Figure 44. Bottom Layer Traces and Copper

Copyright © 2017–2019, Texas Instruments Incorporated

Layout Example (continued)

Figure 45 and Figure 46 are 3D layout pictures with top view and bottom views.

NOTE

The location of the PCB cutout between the primary side and secondary sides, which ensures isolation performance.

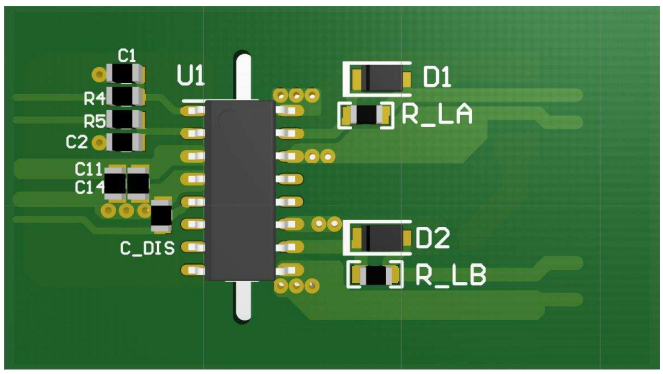


Figure 45. 3-D PCB Top View

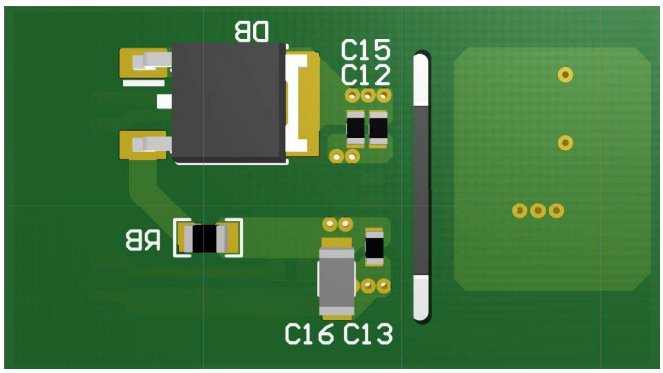


Figure 46. 3-D PCB Bottom View

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Isolation Glossary

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC21220	Click here	Click here	Click here	Click here	Click here
UCC21220A	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.

13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2017–2019, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC21220AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	21220A	Samples
UCC21220ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	21220A	Samples
UCC21220D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	21220	Samples
UCC21220DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	21220	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

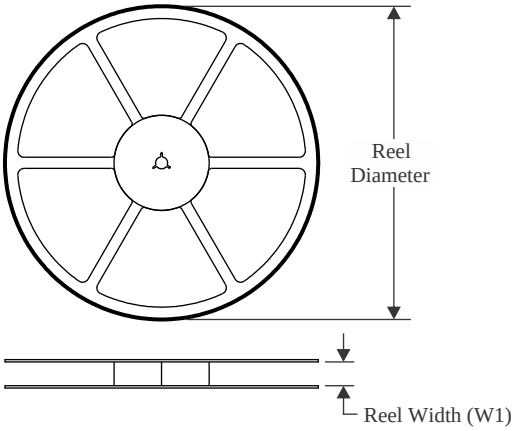
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

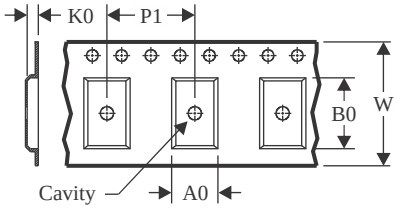
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

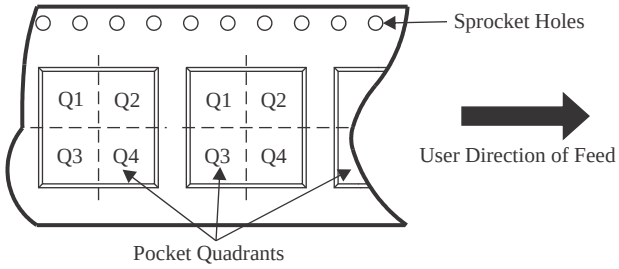


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

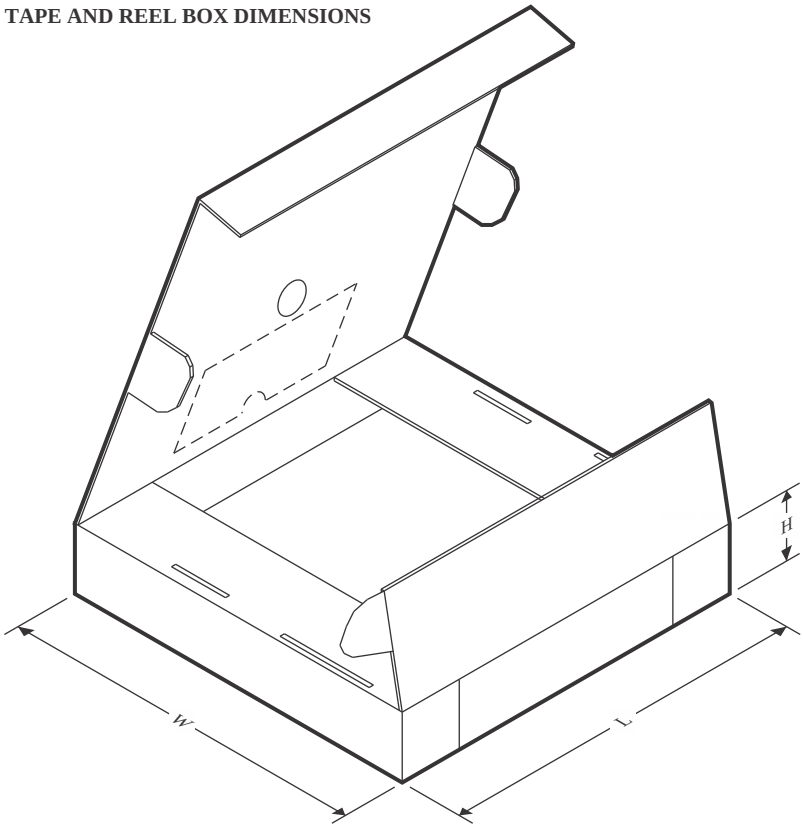
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC21220ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC21220ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC21220DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC21220DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

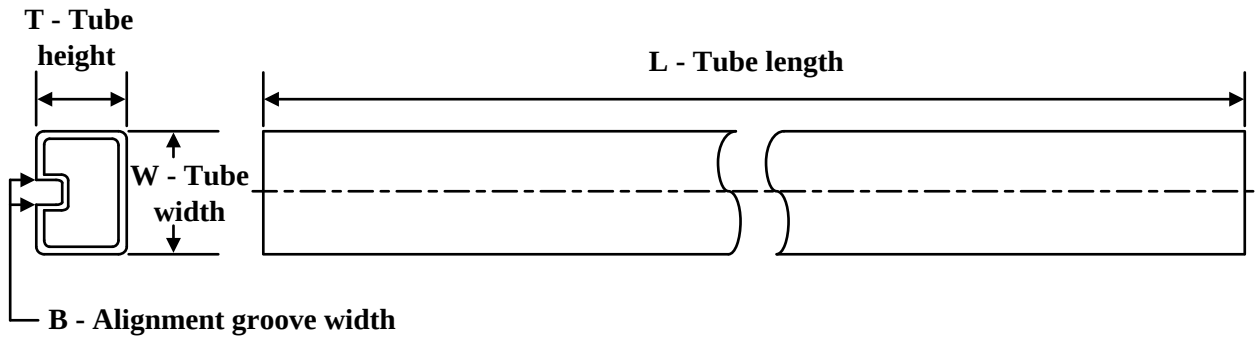
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC21220ADR	SOIC	D	16	2500	356.0	356.0	35.0
UCC21220ADR	SOIC	D	16	2500	350.0	350.0	43.0
UCC21220DR	SOIC	D	16	2500	350.0	350.0	43.0
UCC21220DR	SOIC	D	16	2500	356.0	356.0	35.0

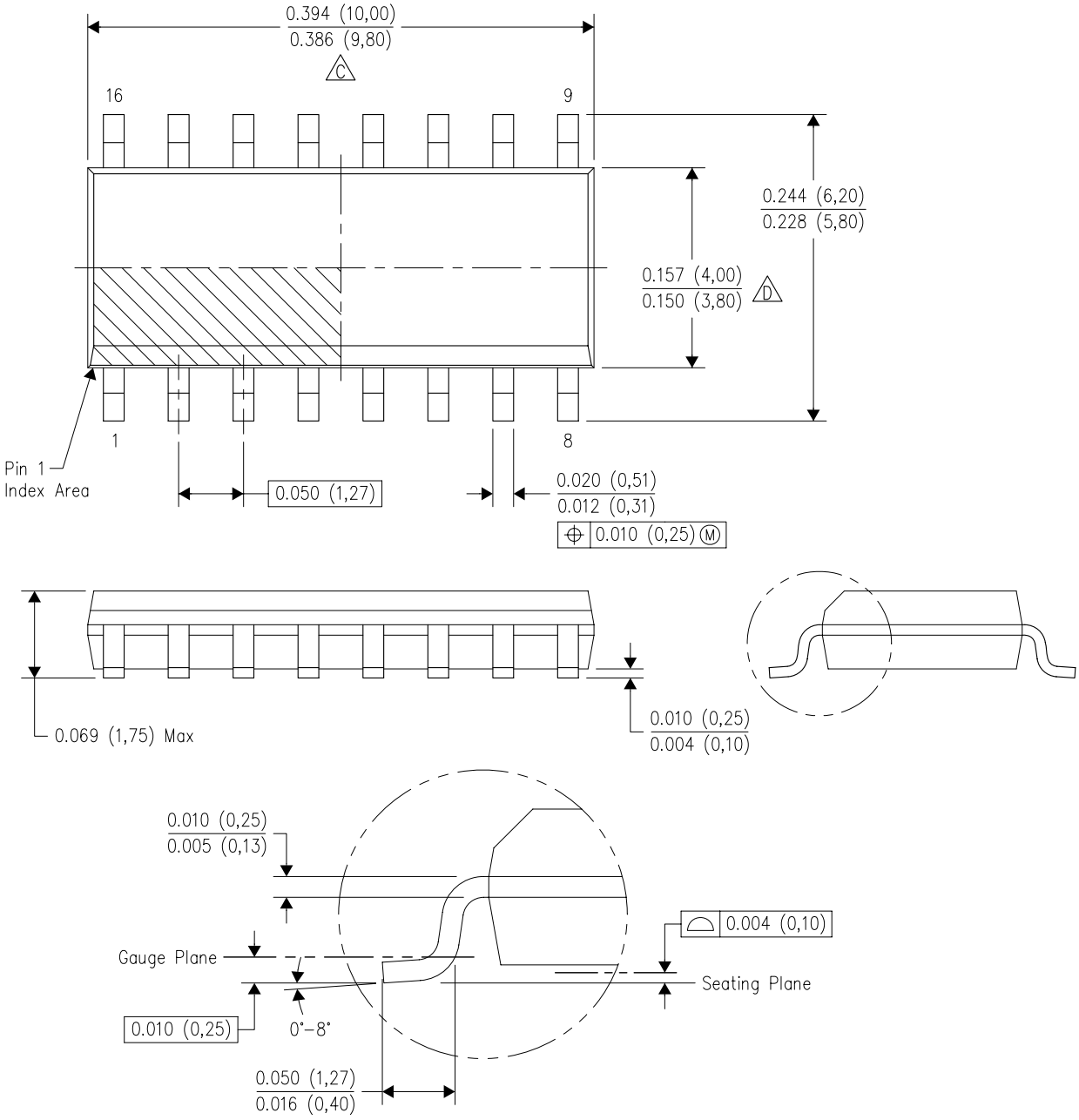
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC21220AD	D	SOIC	16	40	505.46	6.76	3810	4
UCC21220AD	D	SOIC	16	40	506.6	8	3940	4.32
UCC21220D	D	SOIC	16	40	505.46	6.76	3810	4
UCC21220D	D	SOIC	16	40	506.6	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated