# UCC27212 120-V Boot, 4-A Peak, High-Frequency Half-Bridge Driver

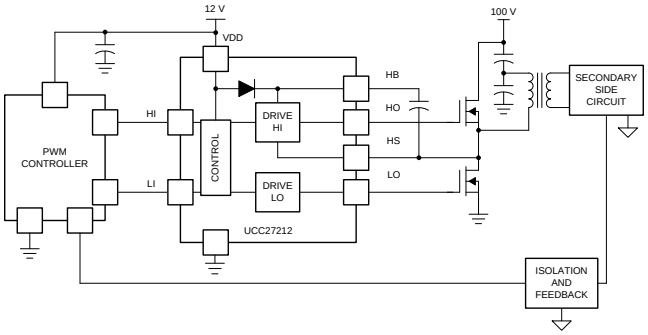
## 1 Features

- 4-A Sink, 4-A Source Output Currents
- Maximum Boot Voltage 120-V DC
- 7-V to 17-V VDD Operating Range
- 20-V ABS Maximum VDD Operating Range
- 5-V Turn-off Under Voltage Lockout (UVLO)
- Input Pins Can Tolerate –10 V to +20 V
- 7.2-ns Rise and 5.5-ns Fall Time (1000-pF Load)
- 20-ns Typical Propagation Delay
- 4-ns Typical Delay Matching
- Specified from –40°C to +140°C

## 2 Applications

- DC-DC Power Supplies
- Merchant Telecom Rectifiers
- Half-Bridge and Full-Bridge Converters
- Push-Pull and Active-Clamp Forward Converters

### Typical Application Diagram






## 3 Description

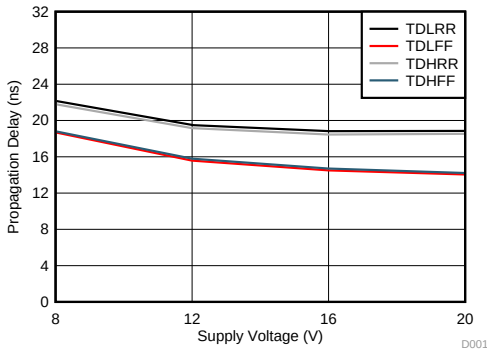
The UCC27212 device has a peak output current of 4-A source and 4-A sink, which allows for the ability to drive large power MOSFETs. The device features an on-chip 120-V rated bootstrap diode eliminating the need for external discrete diodes. The input structure can directly handle –10 V, which increases robustness and is also independent of supply voltage. The UCC27212 offers 5 V UVLO which helps lower power losses and increased input hysteresis that allows for interface to analog or digital PWM controllers with enhanced noise immunity. The switching node of the UCC27212 (HS pin) can handle –18-V maximum, which allows the high-side channel to be protected from inherent negative voltages.

### Device Information(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| UCC27212 | WSON (10) | 4.0 mm x 4.0 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Propagation Delays vs Supply Voltage T = 25°C



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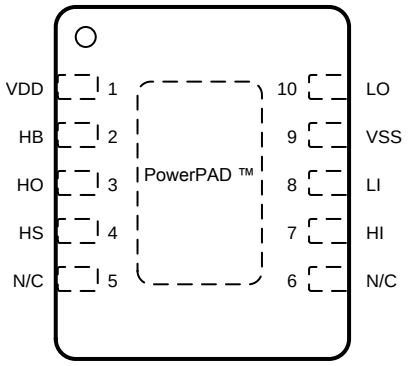
# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (June 2017) to Revision A | Page |
|---|---|
| • Changed " 5-V to 17-V VDD Operating Range, (20-V ABS Maximum)" to "7-V to 17-V VDD Operating Range, (20-V ABS Maximum)" | 1 |
| • Changed extended output pulse from 325-ns MAX to 325-ns TYP. | 8 |

# 5 Pin Configuration and Functions

**DPR Package**
**SON-10**
**Top View**




Not to scale

**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 2 | HB | P | High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 µF to 0.1 µF. |
| 7 | HI | I | High-side input.(1) |
| 3 | HO | O | High-side output. Connect to the gate of the high-side power MOSFET. |
| 4 | HS | P | High-side source connection. Connect to source of high-side power MOSFET. Connect the negative side of bootstrap capacitor to this pin. |
| 8 | LI | I | Low-side input.(1) |
| 10 | LO | O | Low-side output. Connect to the gate of the low-side power MOSFET. |
| 5 | N/C | — | No internal connection. |
| 6 | N/C | — | No internal connection. |
| Pad | PowerPAD ™ (2) | G | Used on the DDA, DRM and DPR packages only. Electrically referenced to VSS (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance. |
| 1 | VDD | P | Positive supply to the lower-gate driver. Decouple this pin to VSS (GND). Typical decoupling capacitor range is 0.22 µF to 4.7 µF.(3) |
| 9 | VSS | G | Negative supply terminal for the device which is generally grounded. |

(1) For cold temperature applications TI recommends the upper capacitance range. Follow the Layout Guidelines for PCB layout.
(2) The thermal pad is not directly connected to any leads of the package; however, it is electrically and thermally connected to the substrate which is the ground of the device.
(3) HI or LI input is assumed to connect to a low impedance source signal. The source output impedance is assumed less than 100 Ω. If the source impedance is greater than 100 Ω, add a bypassing capacitor, each, between HI and VSS and between LI and VSS. The added capacitor value depends on the noise levels presented on the pins, typically from 1 nF to 10 nF should be effective to eliminate the possible noise effect. When noise is present on two pins, HI or LI, the effect is to cause HO and LO malfunctions to have wrong logic outputs.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$(2), $V_{HB} – V_{HS}$ | Supply voltage range | | –0.3 | 20 | V |
| $V_{LI}$, $V_{HI}$ | Input voltages on LI and HI | | –10 | 20 | V |
| $V_{LO}$ | Output voltage on LO | DC | –0.3 | VDD + 0.3 | V |
| | | Repetitive pulse < 100 ns(3) | –2 | VDD + 0.3 | V |
| $V_{HO}$ | Output voltage on HO | DC | $V_{HS}$ – 0.3 | VHB + 0.3 | V |
| | | Repetitive pulse < 100 ns(3) | $V_{HS}$ – 2 | VHB + 0.3 | V |
| $V_{HS}$ | Voltage on HS | DC | –1 | 100 | V |
| | | Repetitive pulse < 100 ns(3) | –(24 V – VDD) | 115 | V |
| $V_{HB}$ | Voltage on HB | | –0.3 | 120 | V |
| $T_J$ | Operating virtual junction temperature range | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to VSS unless otherwise noted. Currents are positive into and negative out of the specified terminal.
(3) Verified at bench characterization. VDD is the value used in an application design.

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range, all voltages are with respect to VSS; currents are positive into and negative out of the specified terminal. –40°C < $T_J$ = $T_A$ < 140°C (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage range, $V_{HB}$ – $V_{HS}$ | 7 | 12 | 17 | V |
| $V_{HS}$ | Voltage on HS | –1 | | 100 | V |
| $V_{HS}$ | Voltage on HS (repetitive pulse < 100 ns) | –(20 V – VDD) | | 110 | V |
| $V_{HB}$ | Voltage on HB | $V_{HS}$ + 8 | | 115 | V |
| | Voltage slew rate on HS | | | 50 | V/ns |
| | Operating junction temperature | –40 | | 140 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | UCC27212 DPR (SON) 10 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 36.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 36.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 14.0 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 14.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range, $V_{HS}$ = $V_{SS}$ = 0 V, no load on LO or HO, $T_A$ = $T_J$ = –40°C to +140°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENTS, $V_{DD}$ = $V_{HB}$ = 12 V** | | | | | | |
| $I_{DD}$ | $V_{DD}$ quiescent current | $V_{(LI)}$ = $V_{(HI)}$ = 0 V | 0.05 | 0.085 | 0.17 | mA |
| $I_{DDO}$ | $V_{DD}$ operating current | f = 500 kHz, $C_{LOAD}$ = 0 | 2.1 | 2.5 | 6.5 | mA |
| $I_{HB}$ | Boot voltage quiescent current | $V_{(LI)}$ = $V_{(HI)}$ = 0 V | 0.015 | 0.065 | 0.1 | mA |
| $I_{HBO}$ | Boot voltage operating current | f = 500 kHz, $C_{LOAD}$ = 0 | 1.5 | 2.5 | 5.1 | mA |
| $I_{HBS}$ | HB to $V_{SS}$ quiescent current | $V_{(HS)}$ = $V_{(HB)}$ = 115 V | | 0.0005 | 1 | µA |
| $I_{HBSO}$ | HB to $V_{SS}$ operating current | f = 500 kHz, $C_{LOAD}$ = 0 | | 0.07 | 1.2 | mA |
| **SUPPLY CURRENTS, $V_{DD}$ = $V_{HB}$ = 6.8 V** | | | | | | |
| $I_{DD}$ | VDD quiescent current | $V_{(LI)}$ = $V_{(HI)}$ = 0 V | 0.02 | 0.065 | 0.14 | mA |
| $I_{DDO}$ | VDD operating current | f = 500 kHz, $C_{LOAD}$ = 0 | 2.1 | 2.5 | 6.5 | mA |
| $I_{HB}$ | Boot voltage quiescent current | $V_{(LI)}$ = $V_{(HI)}$ = 0 V | 0.01 | 0.04 | 0.08 | mA |
| $I_{HBO}$ | Boot voltage operating current | f = 500 kHz, $C_{LOAD}$ = 0 | 1.5 | 2.5 | 5.1 | mA |
| $I_{HBS}$ | HB to VSS quiescent current | $V_{(HS)}$ = $V_{(HB)}$ = 115 V | | 0.0005 | 1 | µA |
| $I_{HBSO}$ | HB to VSS operating current | f = 500 kHz, $C_{LOAD}$ = 0 | | 0.07 | 1.2 | mA |
| **INPUT, $V_{DD}$ = $V_{HB}$ = 12 V** | | | | | | |
| $V_{HIT}$ | Input voltage threshold | | 1.7 | 2.3 | 2.55 | V |
| $V_{LIT}$ | Input voltage threshold | | 1.2 | 1.6 | 1.9 | V |
| $V_{IHYS}$ | Input voltage hysteresis | | | 700 | | mV |
| $R_{IN}$ | Input pulldown resistance | | | 68 | | kΩ |
| **INPUT, $V_{DD}$ = $V_{HB}$ = 6.8 V** | | | | | | |
| $V_{HIT}$ | Input voltage threshold | | 1.6 | 2.0 | 2.6 | V |
| $V_{LIT}$ | Input voltage threshold | | 1.1 | 1.5 | 2.1 | V |

## Electrical Characteristics (continued)

over operating free-air temperature range, $V_{HS}$ = $V_{SS}$ = 0 V, no load on LO or HO, $T_A$ = $T_J$ = –40°C to +140°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IHYS}$ | Input voltage hysteresis | | | 500 | | mV |
| $R_{IN}$ | Input pulldown resistance | | | 68 | | kΩ |
| **UNDER-VOLTAGE LOCKOUT (UVLO), $V_{DD}$ = $V_{HB}$ = 12 V** | | | | | | |
| $V_{DDR}$ | $V_{DD}$ turnon threshold | | 4.9 | 5.7 | 6.4 | V |
| $V_{DDHYS}$ | Hysteresis | | | 0.4 | | V |
| $V_{HBR}$ | $V_{HB}$ turnon threshold | | 4.35 | 5.3 | 6.3 | V |
| $V_{HBHYS}$ | Hysteresis | | | 0.3 | | V |
| **BOOTSTRAP DIODE, $V_{DD}$ = $V_{HB}$ = 12 V** | | | | | | |
| $V_F$ | Low-current forward voltage | $I_{VDD-HB}$ = 100 µA | | 0.65 | 0.8 | V |
| $V_{FI}$ | High-current forward voltage | $I_{VDD-HB}$ = 100 mA | | 0.85 | 0.95 | V |
| $R_D$ | Dynamic resistance, ΔVF/ΔI | $I_{VDD-HB}$ = 100 mA and 80 mA | 0.3 | 0.5 | 0.85 | Ω |
| **BOOTSTRAP DIODE, $V_{DD}$ = $V_{HB}$ = 6.8 V** | | | | | | |
| $V_F$ | Low-current forward voltage | $I_{VDD-HB}$ = 100 µA | | 0.65 | 0.8 | V |
| $V_{FI}$ | High-current forward voltage | $I_{VDD-HB}$ = 100 mA | | 0.85 | 0.95 | V |
| $R_D$ | Dynamic resistance, ΔVF/ΔI | $I_{VDD-HB}$ = 100 mA and 80 mA | 0.3 | 0.5 | 0.85 | Ω |
| **LO GATE DRIVER, $V_{DD}$ = $V_{HB}$ = 12 V** | | | | | | |
| $V_{LOL}$ | Low-level output voltage | | 0.05 | 0.1 | 0.19 | V |
| $V_{LOH}$ | High level output voltage | | 0.1 | 0.16 | 0.29 | V |
| | Peak pullup current(1) | | | 3.7 | | A |
| | Peak pulldown current (1) | | | 4.5 | | A |
| **LO GATE DRIVER, $V_{DD}$ = $V_{HB}$ = 6.8 V** | | | | | | |
| $V_{LOL}$ | Low-level output voltage | $I_{LO}$ = 100 mA | 0.04 | 0.13 | 0.35 | V |
| $V_{LOH}$ | High level output voltage | $I_{LO}$ = –100 mA, $V_{LOH}$ = $V_{DD}$ – $V_{LO}$ | 0.12 | 0.23 | 0.42 | V |
| | Peak pullup current | $V_{LO}$ = 0 V | | 1.3 | | A |
| | Peak pulldown current | $V_{LO}$ = 12 V for VDD = 6.8V | | 1.7 | | A |
| **HO GATE DRIVER, $V_{DD}$ = $V_{HB}$ = 12 V** | | | | | | |
| $V_{HOL}$ | Low-level output voltage | | 0.05 | 0.1 | 0.19 | V |
| $V_{HOH}$ | High-level output voltage | | 0.1 | 0.16 | 0.29 | V |
| | Peak pullup current (1) | | | 3.7 | | A |
| | Peak pulldown current (1) | | | 4.5 | | A |
| **HO GATE DRIVER, $V_{DD}$ = $V_{HB}$ = 6.8 V** | | | | | | |
| $V_{LOL}$ | Low-level output voltage | $I_{HO}$ = 100 mA | 0.04 | 0.13 | 0.35 | V |
| $V_{LOH}$ | High level output voltage | $I_{HO}$ = –100 mA, $V_{HOH}$ = $V_{HB}$ – $V_{HO}$ | 0.12 | 0.23 | 0.42 | V |
| | Peak pullup current | $V_{HO}$ = 0 V | | 1.3 | | A |
| | Peak pulldown current | $V_{HO}$ = 12 V for VDD = 6.8V | | 1.7 | | A |

(1) Ensured by design.

## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PROPAGATION DELAYS, $V_{DD}$ = $V_{HB}$ = 12 V** | | | | | | |
| $T_{DLFF}$ | $V_{LI}$ falling to $V_{LO}$ falling | $C_{LOAD}$ = 0 | 10 | 16 | 30 | ns |
| $T_{DHFF}$ | $V_{HI}$ falling to $V_{HO}$ falling | $C_{LOAD}$ = 0 | 10 | 16 | 30 | ns |
| $T_{DLRR}$ | $V_{LI}$ rising to $V_{LO}$ rising | $C_{LOAD}$ = 0 | 10 | 20 | 42 | ns |
| $T_{DHRR}$ | $V_{HI}$ rising to $V_{HO}$ rising | $C_{LOAD}$ = 0 | 10 | 20 | 42 | ns |

## Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PROPAGATION DELAYS, $V_{DD}$ = $V_{HB}$ = 6.8 V** | | | | | | |
| $T_{DLFF}$ | $V_{LI}$ falling to $V_{LO}$ falling | $C_{LOAD}$ = 0 | 10 | 24 | 50 | ns |
| $T_{DHFF}$ | $V_{HI}$ falling to $V_{HO}$ falling | $C_{LOAD}$ = 0 | 10 | 24 | 50 | ns |
| $T_{DLRR}$ | $V_{LI}$ rising to $V_{LO}$ rising | $C_{LOAD}$ = 0 | 13 | 28 | 57 | ns |
| $T_{DHRR}$ | $V_{HI}$ rising to $V_{HO}$ rising | $C_{LOAD}$ = 0 | 13 | 28 | 57 | ns |
| **DELAY MATCHING, $V_{DD}$ = $V_{HB}$ = 12 V** | | | | | | |
| $T_{MON}$ | From HO OFF to LO ON | $T_J$ = 25°C | | 4 | 9.5 | ns |
| | | $T_J$ = –40°C to +140°C | | 4 | 17 | ns |
| $T_{MOFF}$ | From LO OFF to HO ON | $T_J$ = 25°C | | 4 | 9.5 | ns |
| | | $T_J$ = –40°C to +140°C | | 4 | 17 | ns |
| **DELAY MATCHING, $V_{DD}$ = $V_{HB}$ = 6.8 V** | | | | | | |
| $T_{MON}$ | From HO OFF to LO ON | $T_J$ = 25°C | | 8 | | ns |
| | | $T_J$ = –40°C to +140°C | | 8 | 18 | ns |
| $T_{MOFF}$ | From LO OFF to HO ON | $T_J$ = 25°C | | 6 | | ns |
| | | $T_J$ = –40°C to +140°C | | 6 | 18 | ns |
| **OUTPUT RISE AND FALL TIME, $V_{DD}$ = $V_{HB}$ = 12 V** | | | | | | |
| $t_R$ | LO rise time | $C_{LOAD}$ = 1000 pF, from 10% to 90% | | 7.8 | | ns |
| $t_R$ | HO rise time | $C_{LOAD}$ = 1000 pF, from 10% to 90% | | 7.8 | | ns |
| $t_F$ | LO fall time | $C_{LOAD}$ = 1000 pF, from 90% to 10% | | 6.0 | | ns |
| $t_F$ | HO fall time | $C_{LOAD}$ = 1000 pF, from 90% to 10% | | 6.0 | | ns |
| $t_R$ | LO, HO | $C_{LOAD}$ = 0.1 µF, (3 V to 9 V) | | 0.36 | 0.6 | µs |
| $t_F$ | LO, HO | $C_{LOAD}$ = 0.1 µF, (9 V to 3 V) | | 0.20 | 0.4 | µs |
| **OUTPUT RISE AND FALL TIME, $V_{DD}$ = $V_{HB}$ = 6.8 V** | | | | | | |
| $t_R$ | LO rise time | $C_{LOAD}$ = 1000 pF, from 10% to 90% | | 9.5 | | ns |
| $t_R$ | HO rise time | $C_{LOAD}$ = 1000 pF, from 10% to 90% | | 13.0 | | ns |
| $t_F$ | LO fall time | $C_{LOAD}$ = 1000 pF, from 90% to 10% | | 9.5 | | ns |
| $t_F$ | HO fall time | $C_{LOAD}$ = 1000 pF, from 90% to 10% | | 13.0 | | ns |
| $t_R$ | LO, HO | $C_{LOAD}$ = 0.1 µF, (30% to 70%) | | 0.45 | 0.7 | µs |
| $t_F$ | LO, HO | $C_{LOAD}$ = 0.1 µF, (70% to 30%) | | 0.2 | 0.5 | µs |
| **MISCELLANEOUS** | | | | | | |
| Minimum input pulse width that changes the output | | | | | 100 | ns |
| Bootstrap diode turnoff time (1)(2) | | IF = 20 mA, $I_{REV}$ = 0.5 A (3) | | 20 | | ns |
| Extended output pulse | | when VDD = VHB = 6.8 V, VHS = 100 V, and input pulse width is 100 ns | | 325 | | ns |

(1) Ensured by design.
(2) $I_F$: Forward current applied to bootstrap diode, IREV: Reverse current applied to bootstrap diode.
(3) Typical values for $T_A$ = 25°C.

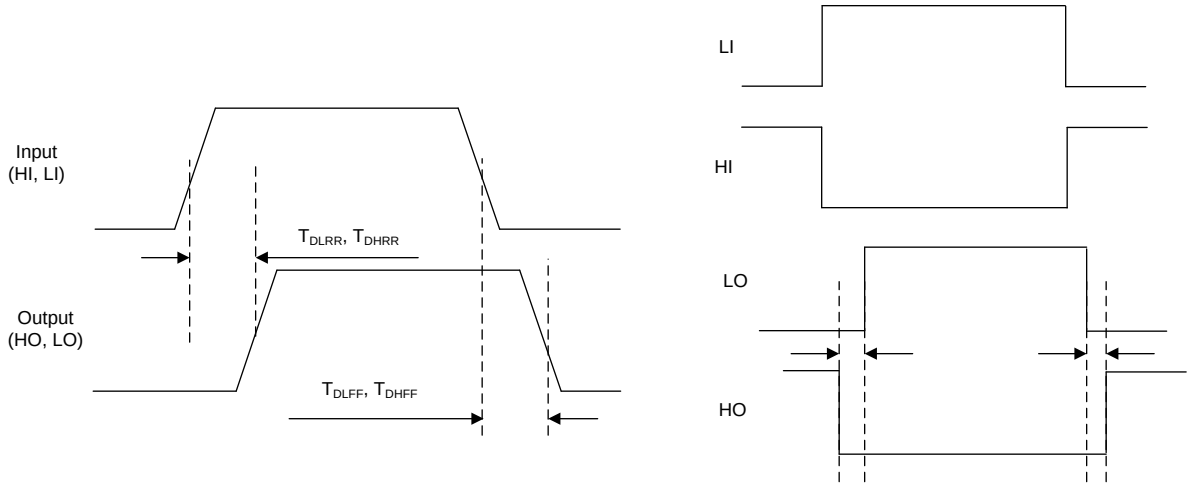



**Figure 1. Timing Diagram**

## 6.7 Typical Characteristics

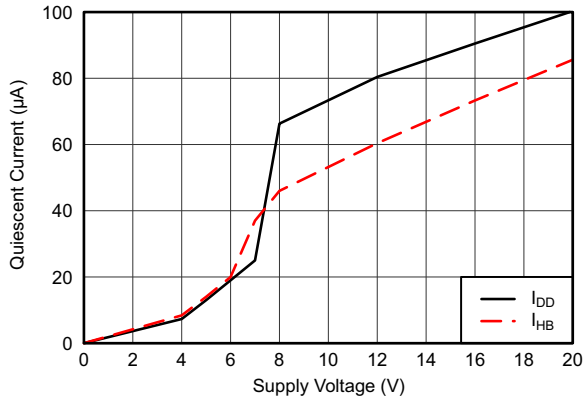



**Figure 2. Quiescent Current vs Supply Voltage**

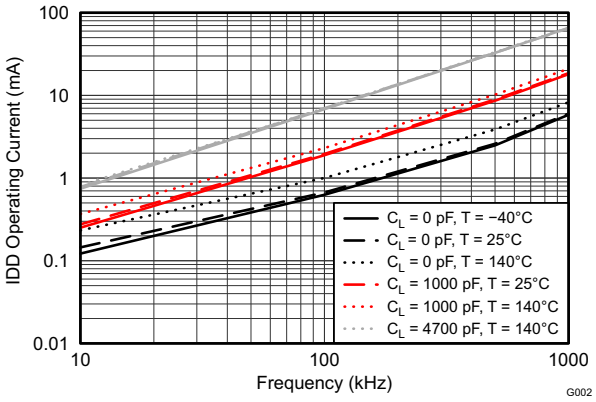



**Figure 3. IDD Operating Current vs Frequency**

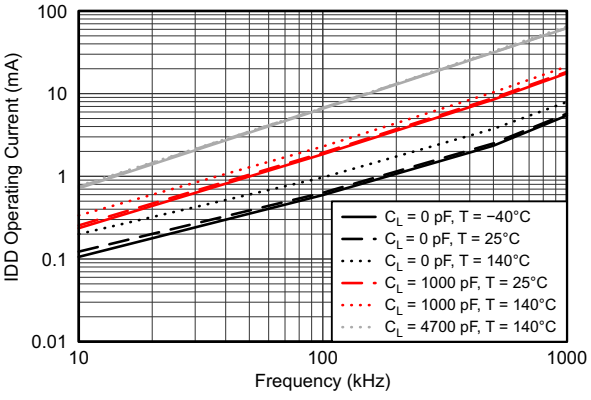



**Figure 4. IDD Operating Current vs Frequency**

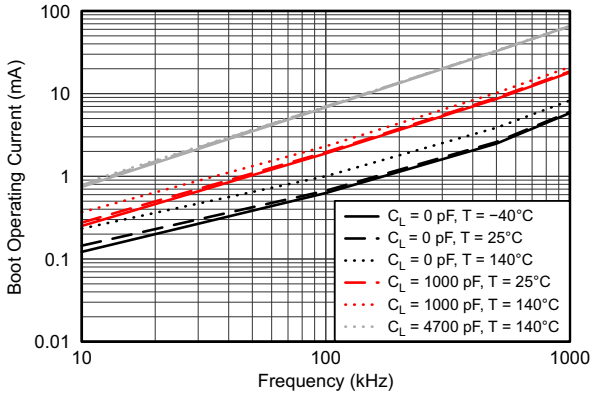



**Figure 5. Boot Voltage Operating Current vs Frequency (HB To HS)**

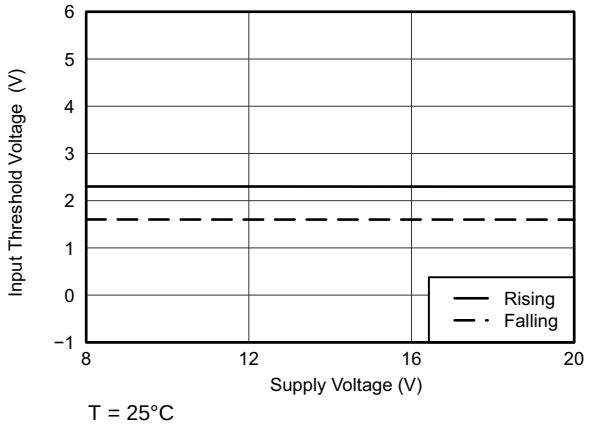



**Figure 6. Input Threshold vs Supply Voltage**

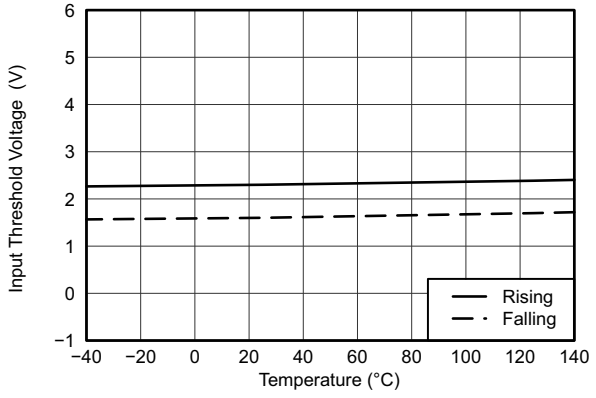
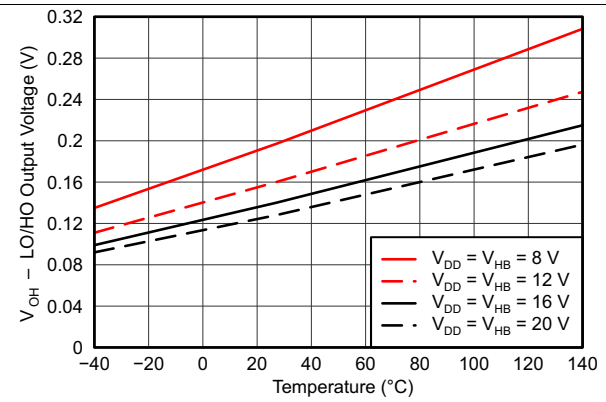


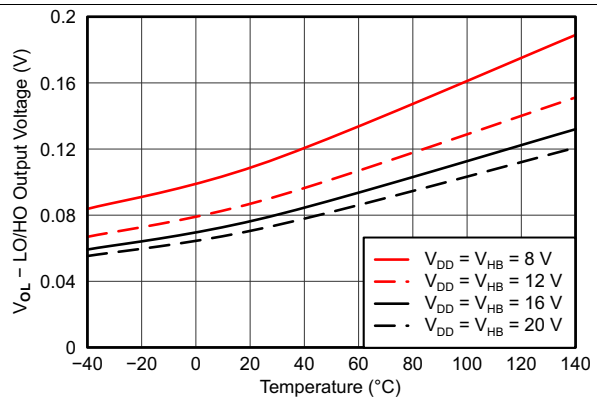

**Figure 7. Input Thresholds vs Temperature**

## Typical Characteristics (continued)




$I_{HO}$ = $I_{LO}$ = 100 mA

**Figure 8. LO and HO High-Level Output Voltage vs Temperature**




$I_{HO}$ = $I_{LO}$ = 100 mA

**Figure 9. LO and HO Low-Level Output Voltage vs Temperature**

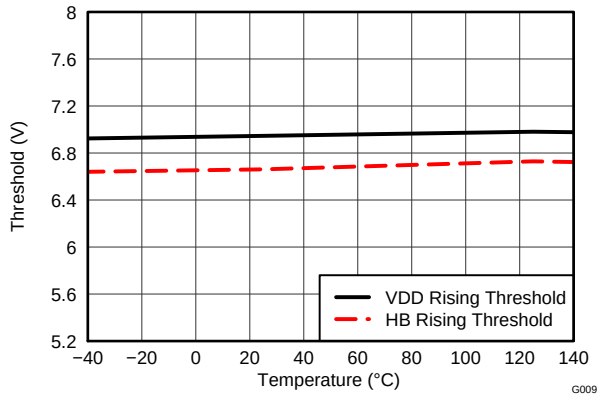



**Figure 10. Undervoltage Lockout Threshold vs Temperature**

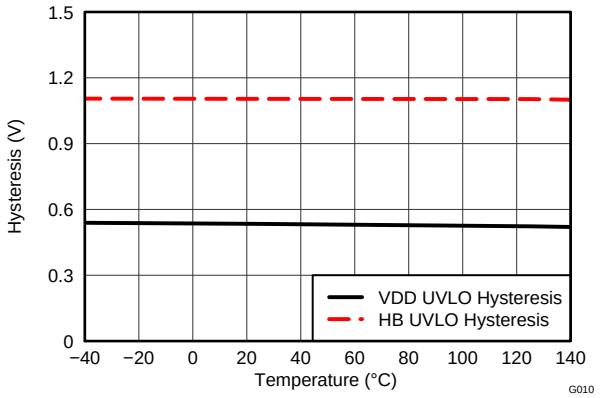
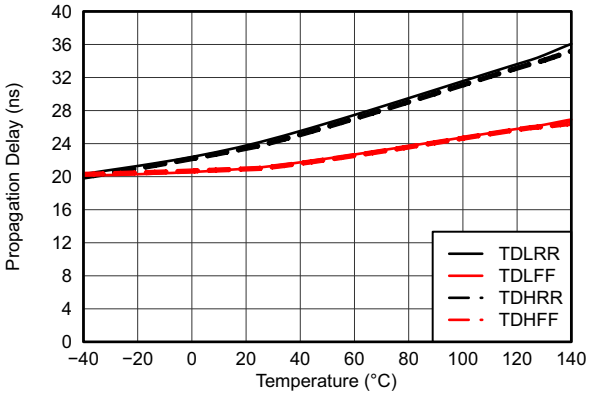
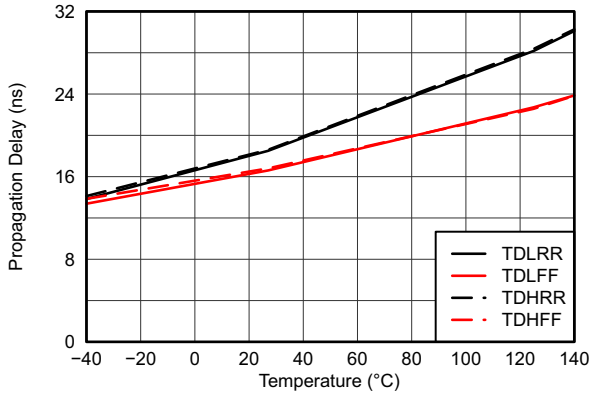



**Figure 11. Undervoltage Lockout Threshold Hysteresis vs Temperature**




$V_{DD}$ = $V_{HB}$ = 12 V

**Figure 12. Propagation Delays vs Temperature**




$V_{DD}$ = $V_{HB}$ = 12 V

**Figure 13. Propagation Delays vs Temperature**

## Typical Characteristics (continued)

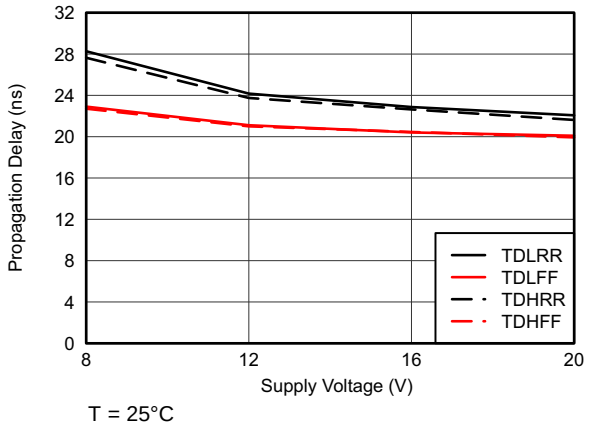



**Figure 14. Propagation Delays vs Supply Voltage ($V_{DD}$ = $V_{HB}$)**

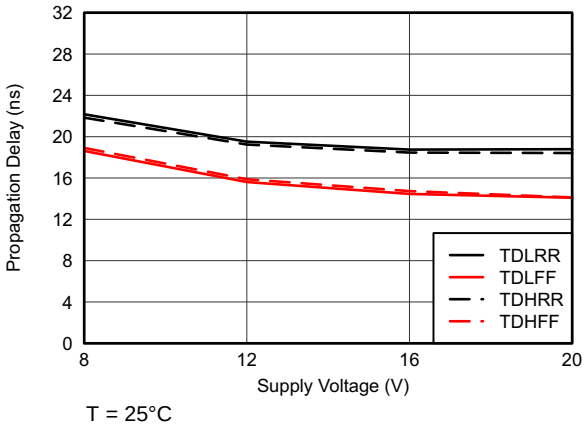



**Figure 15. Propagation Delays vs Supply Voltage ($V_{DD}$ = $V_{HB}$)**

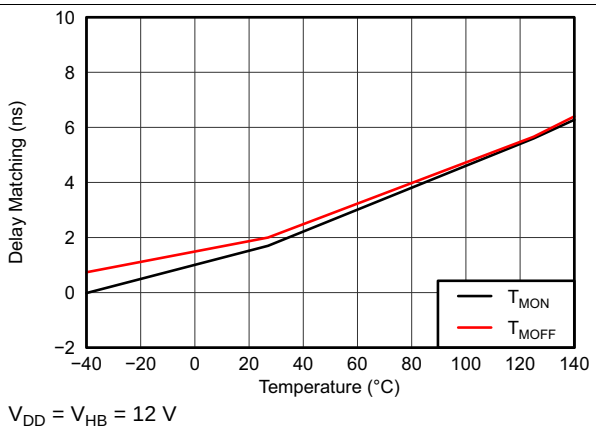



**Figure 16. Delay Matching vs Temperature**

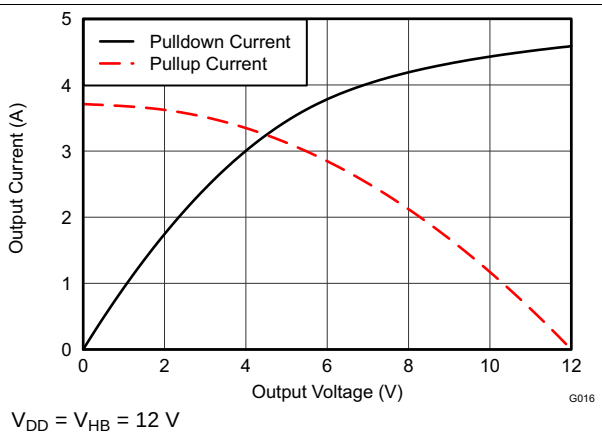



**Figure 17. Output Current vs Output Voltage**

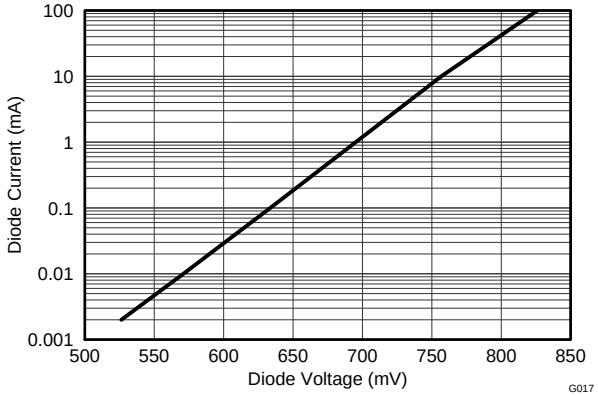



**Figure 18. Diode Current vs Diode Voltage**

# 7 Detailed Description

## 7.1 Overview

The UCC27212 device represents Texas Instruments' latest generation of high-voltage gate drivers, which are designed to drive both the high-side and low-side of N-Channel MOSFETs in a half- and full-bridge or synchronous-buck configuration. The floating high-side driver can operate with supply voltages of up to 120 V, which allows for N-Channel MOSFET control in half-bridge, full-bridge, push-pull, two-switch forward, and active clamp forward converters.

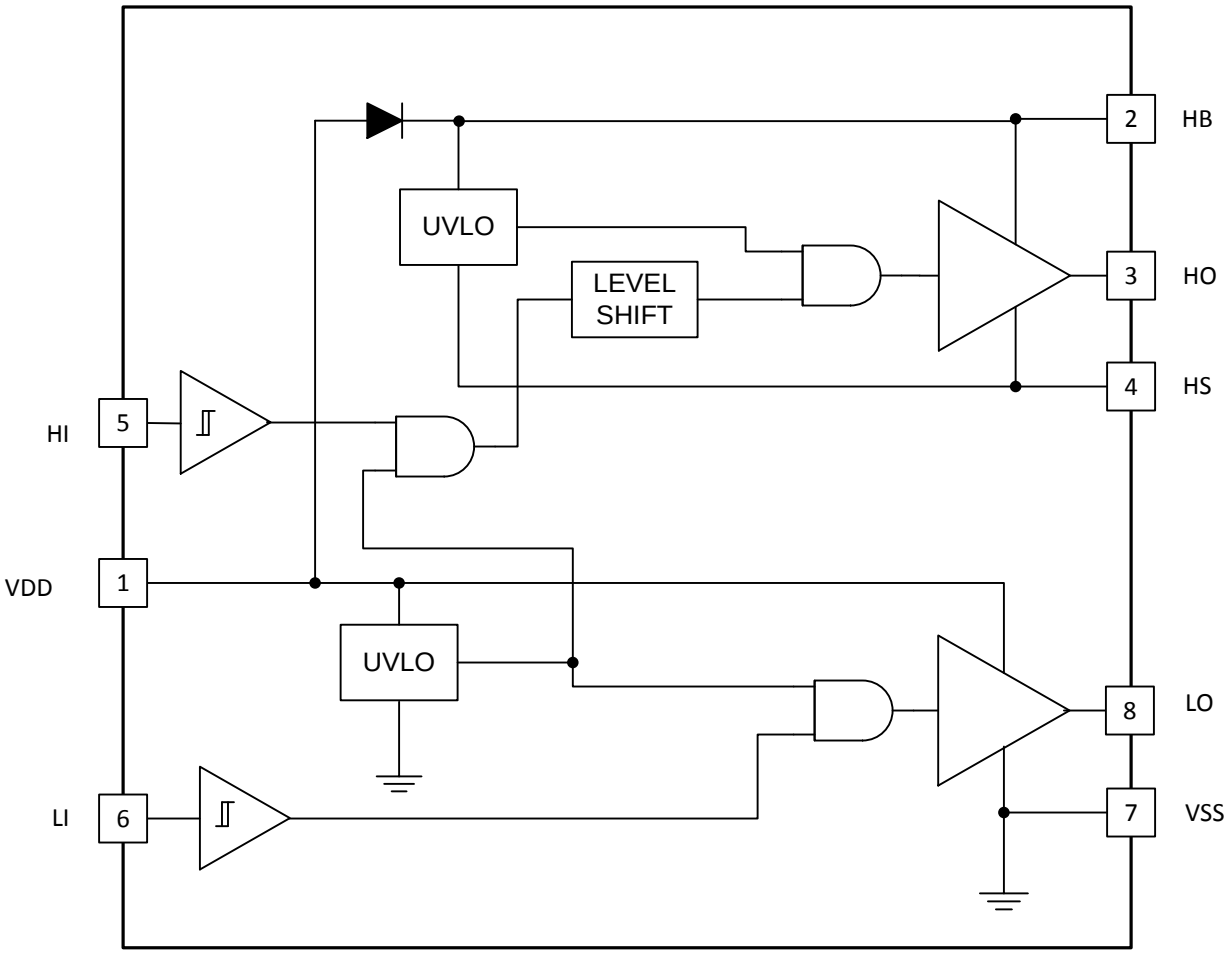
The UCC27212 device feature 4-A source and sink capability, industry best-in-class switching characteristics and a host of other features listed in Table 1. These features combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

**Table 1. UCC27212 Highlights**

| FEATURE | BENEFIT |
|---|---|
| 4-A source and sink current with 0.9-Ω output resistance | High peak current ideal for driving large power MOSFETs with minimal power loss (fast-drive capability at Miller plateau) |
| Input pins (HI and LI) can directly handle –10 VDC up to 20 VDC | Increased robustness and ability to handle undershoot and overshoot can interface directly to gate-drive transformers without having to use rectification diodes. |
| 120-V internal boot diode | Provides voltage margin to meet telecom 100-V surge requirements |
| Switch node (HS pin) able to handle –18 V maximum for 100 ns | Allows the high-side channel to have extra protection from inherent negative voltages caused by parasitic inductance and stray capacitance |
| Robust ESD circuitry to handle voltage spikes | Excellent immunity to large dV/dT conditions |
| 18-ns propagation delay with 7.2-ns rise time and 5.5-ns fall time | Best-in-class switching characteristics and extremely low-pulse transmission distortion |
| 2-ns (typical) delay matching between channels | Avoids transformer volt-second offset in bridge |
| Symmetrical UVLO circuit | Ensures high-side and low-side shut down at the same time |
| TTL optimized thresholds with increased hysteresis | Complementary to analog or digital PWM controllers; increased hysteresis offers added noise immunity |

In the UCC27212 device, the high side and low side each have independent inputs that allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27212. The UCC27212 is the TTL or logic compatible version. The high-side driver is referenced to the switch node (HS), which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to $V_{SS}$, which is typically ground. The UCC27212 functions are divided into the input stages, UVLO protection, level shift, boot diode, and output driver stages.

## 7.2 Functional Block Diagram






## 7.3 Feature Description

### 7.3.1 Input Stages

The input stages provide the interface to the PWM output signals. The input stages of the UCC27212 device have impedance of 70-kΩ nominal and input capacitance is approximately 2 pF. Pulldown resistance to $V_{SS}$ (ground) is 70 kΩ. The logic level compatible input provides a rising threshold of 2.3 V and a falling threshold of 1.6 V. There is enough input hysteresis to avoid noise related jitter issues on the input.

### 7.3.2 Undervoltage Lockout (UVLO)

The bias supplies for the high-side and low-side drivers have UVLO protection. $V_{DD}$ as well as $V_{HB}$ to $V_{HS}$ differential voltages are monitored. The $V_{DD}$ UVLO disables both drivers when $V_{DD}$ is below the specified threshold. The rising $V_{DD}$ threshold is 5.7 V with 0.4-V hysteresis. The VHB UVLO disables only the high-side driver when the $V_{HB}$ to $V_{HS}$ differential voltage is below the specified threshold. The $V_{HB}$ UVLO rising threshold is 5.3 V with 0.4 V hysteresis.

## Feature Description (continued)

### 7.3.3 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

### 7.3.4 Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC27212 family of drivers. The diode anode is connected to $V_{DD}$ and cathode connected to $V_{HB}$. With the $V_{HB}$ capacitor connected to HB and the HS pins, the $V_{HB}$ capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

### 7.3.5 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from $V_{DD}$ to $V_{SS}$ and the high side is referenced from $V_{HB}$ to $V_{HS}$.

## 7.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See the *Undervoltage Lockout (UVLO)* section for information on UVLO operation mode. In the normal mode the output state is dependent on states of the HI and LI pins. Table 2 lists the output states for different input pin combinations.

**Table 2. Device Logic Table**

| HI PIN | LI PIN | HO(1) | LO(2) |
|---|---|---|---|
| L | L | L | L |
| L | H | L | H |
| H | L | H | L |
| H | H | H | H |

(1) HO is measured with respect to HS.
(2) LO is measured with respect to VSS.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

To affect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers, and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

Finally, emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. Gate-driver devices are extremely important components in switching power, and they combine the benefits of high-performance, low-cost component count and board-space reduction as well as simplified system design.

## 8.2 Typical Application

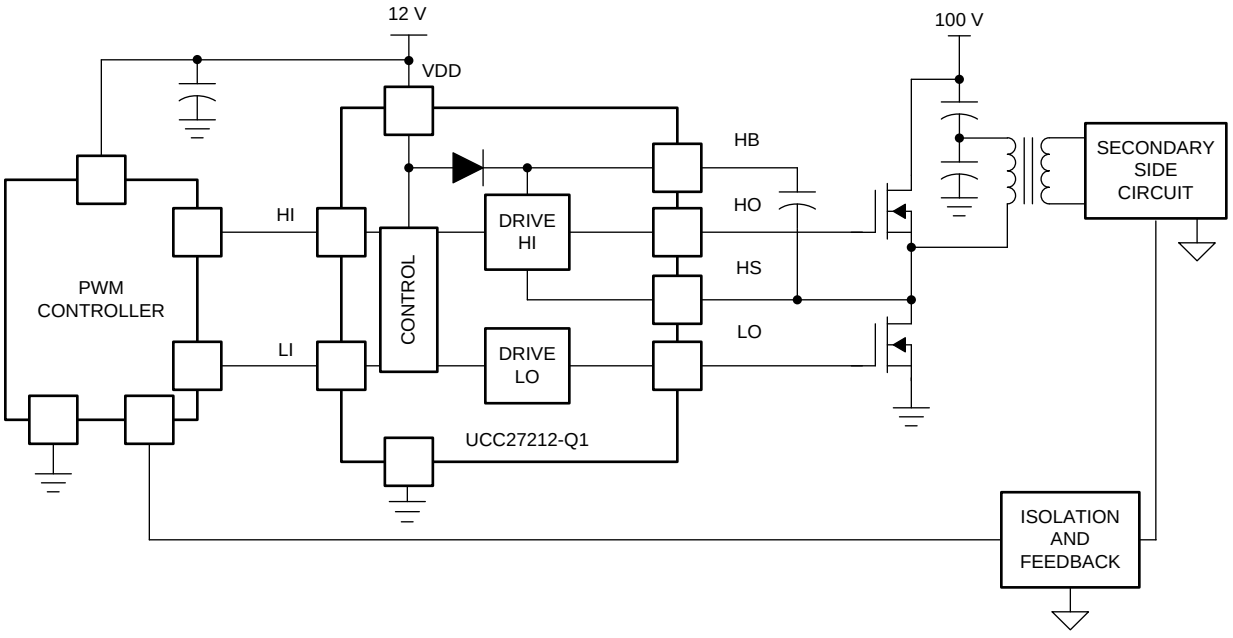





**Figure 19. UCC27212 Typical Application**

## Typical Application (continued)

### 8.2.1 Design Requirements

For this design example, use the parameters listed in Table 3.

**Table 3. Design Specifications**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Supply voltage, VDD | 12 V |
| Voltage on HS, VHS | 0 V to 100 V |
| Voltage on HB, VHB | 12 V to 112 V |
| Output current rating, IO | –4 A to 4 A |
| Operating frequency | 500 kHz |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Power Dissipation*

Power dissipation of the gate driver has two portions as shown in Equation 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

Use Equation 2 to calculate the DC portion of the power dissipation (PDC).

$$PDC = I_Q \times V_{DD}$$

where

- $I_Q$ is the quiescent current for the driver. (2)

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and so forth). The UCC27212 features very low quiescent currents (less than 0.17 mA, refer to the table and contain internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the PDC on the total power dissipation within the gate driver can be safely assumed to be negligible. The power dissipated in the gate-driver package during switching (PSW) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage VG, which is very close to input bias supply voltage VDD)
- Switching frequency
- Use of external gate resistors. When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 3.

$$EG = ½C_{LOAD} \times V_{DD}^2$$

where

- $C_{LOAD}$ is load capacitor
- $V_{DD}$ is bias voltage feeding the driver (3)

There is an equal amount of energy dissipated when the capacitor is charged and when it is discharged. This leads to a total power loss given by Equation 4.

$$PG = C_{LOAD} \times V_{DD}^2 \times f_{SW}$$

where

- $f_{SW}$ is the switching frequency (4)

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when switching a capacitor which is calculated using the equation $Q_G = C_{LOAD} \times V_{DD}$ to provide Equation 5 for power.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} = Q_G \times V_{DD} \times f_{SW} \quad (5)$$

This power $P_G$ is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on and off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor.

### 8.2.3 Application Curves

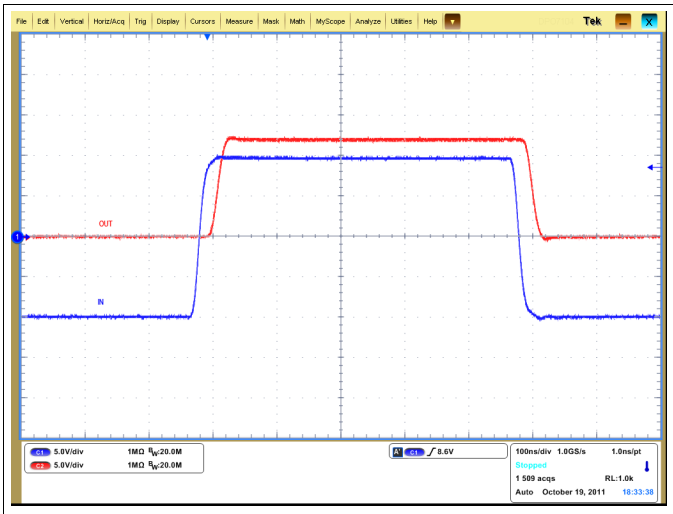



**Figure 20. Negative 10-V Input**

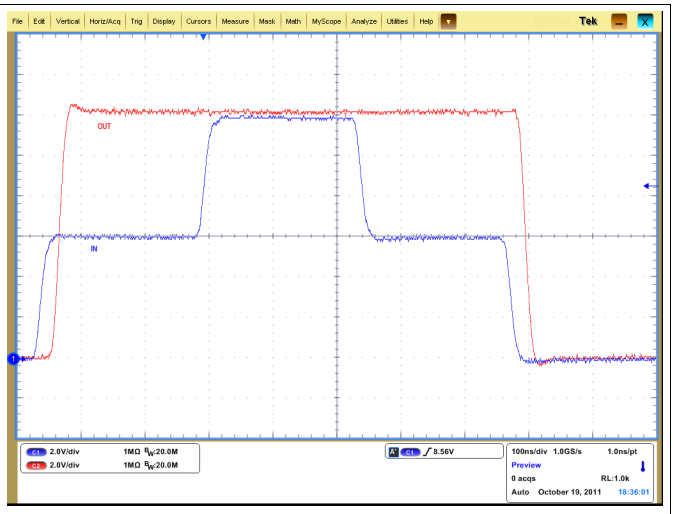



**Figure 21. Step Input**

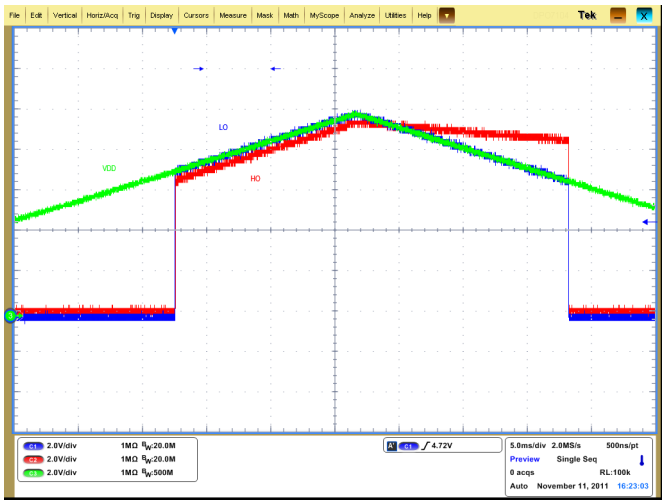



**Figure 22. Symmetrical UVLO**

# 9 Power Supply Recommendations

The bias supply voltage range for which the UCC27212 device is recommended to operate is from 7 V to 17 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the $V_{DD}$ pin supply circuit blocks. Whenever the driver is in UVLO condition when the $V_{DD}$ pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the $V_{DD}$ pin of the device (which is a stress rating). Keeping a 3-V margin to allow for transient voltage spikes, the maximum recommended voltage for the $V_{DD}$ pin is 17 V. The UVLO protection feature also involves a hysteresis function, which means that when the $V_{DD}$ pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(hys)}$. Therefore, ensuring that, while operating at or near the 7 V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the $V_{DD}$ pin voltage has dropped below the $V_{(OFF)}$ threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up the device does not begin operation until the $V_{DD}$ pin voltage has exceeded the $V_{(ON)}$ threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the $V_{DD}$ pin. Although this fact is well known, it is important to recognize that the charge for source current pulses delivered by the HO pin is also supplied through the same $V_{DD}$ pin. As a result, every time a current is sourced out of the HO pin, a corresponding current pulse is delivered into the device through the $V_{DD}$ pin. Thus, ensure that a local bypass capacitor is provided between the $V_{DD}$ and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is required. TI recommends using a capacitor in the range 0.22 µF to 4.7 µF between $V_{DD}$ and GND. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore a 0.022-µF to 0.1-µF local decoupling capacitor is recommended between the HB and HS pins.

# 10 Layout

## 10.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the $V_{DD}$ – $V_{SS}$ and $V_{HB}$-$V_{HS}$ (bootstrap) capacitors as close as possible to the device (see ).
- Pay close attention to the GND trace. Use the thermal pad of the package as GND by connecting it to the VSS pin (GND). The GND trace from the driver goes directly to the source of the MOSFET, but must not be in the high current path of the MOSFET drain or source current.
- Use similar rules for the HS node as for GND for the high-side driver.
- For systems using multiple UCC27212 devices, TI recommends that dedicated decoupling capacitors be located at $V_{DD}$–$V_{SS}$ for each device.
- Care must be taken to avoid placing VDD traces close to LO, HS, and HO signals.
- Use wide traces for LO and HO closely following the associated GND or HS traces. A width of 60 to 100 mils is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node must be routed from one layer to another. For GND, the number of vias must be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid LI and HI (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.

A poor layout can cause a significant drop in efficiency or system malfunction, and it can even lead to decreased reliability of the whole system.

## 10.2 Layout Example

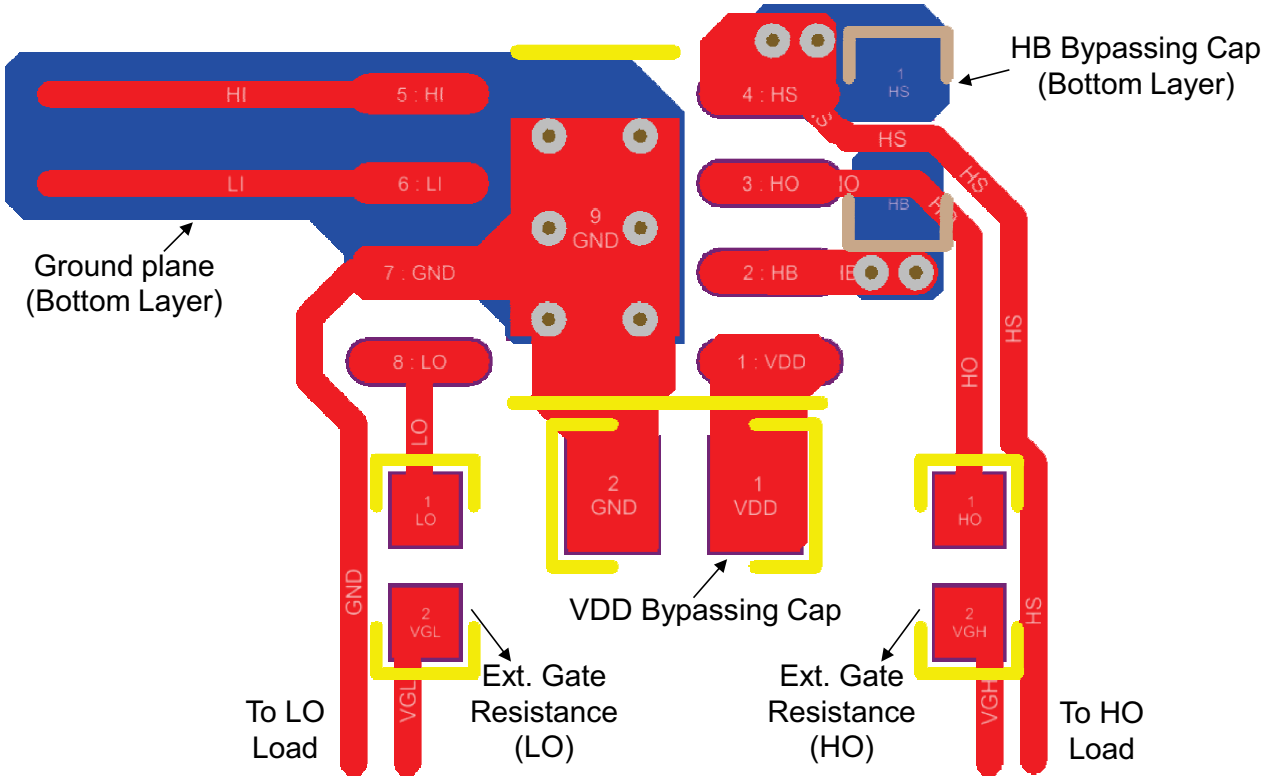



**Figure 23. UCC27212 Layout Example**

### 10.2.1 Thermal Considerations

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. For a gate driver to be useful over a particular temperature range, the package must allow for efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package are listed in . For detailed information regarding the table, refer to the Application Note from Texas Instruments entitled *Semiconductor and IC Package Thermal Metrics* (SPRA953). The UCC27212 device is offered in SOIC (8) and VSON (8). The section lists the thermal performance metrics related to the SOT-23 package.

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation see the following:

- PowerPAD™ Thermally Enhanced Package, Application Report
- PowerPAD™ Made Easy, Application Report

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

E2E is a trademark of Texas Instruments.

## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC27212DPRR | ACTIVE | WSON | DPR | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | UCC 27212 | Samples |
| UCC27212DPRT | ACTIVE | WSON | DPR | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | UCC 27212 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

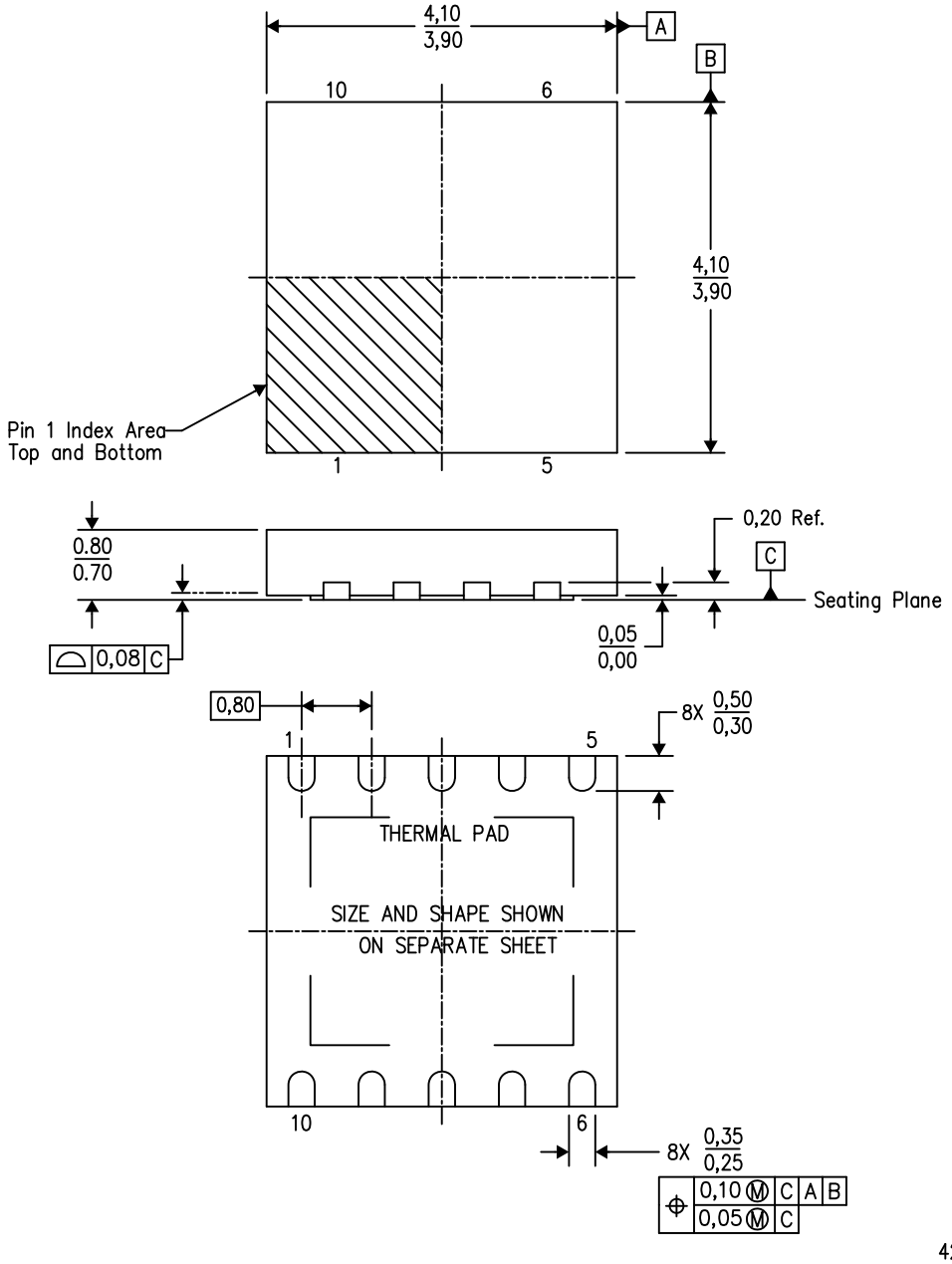
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

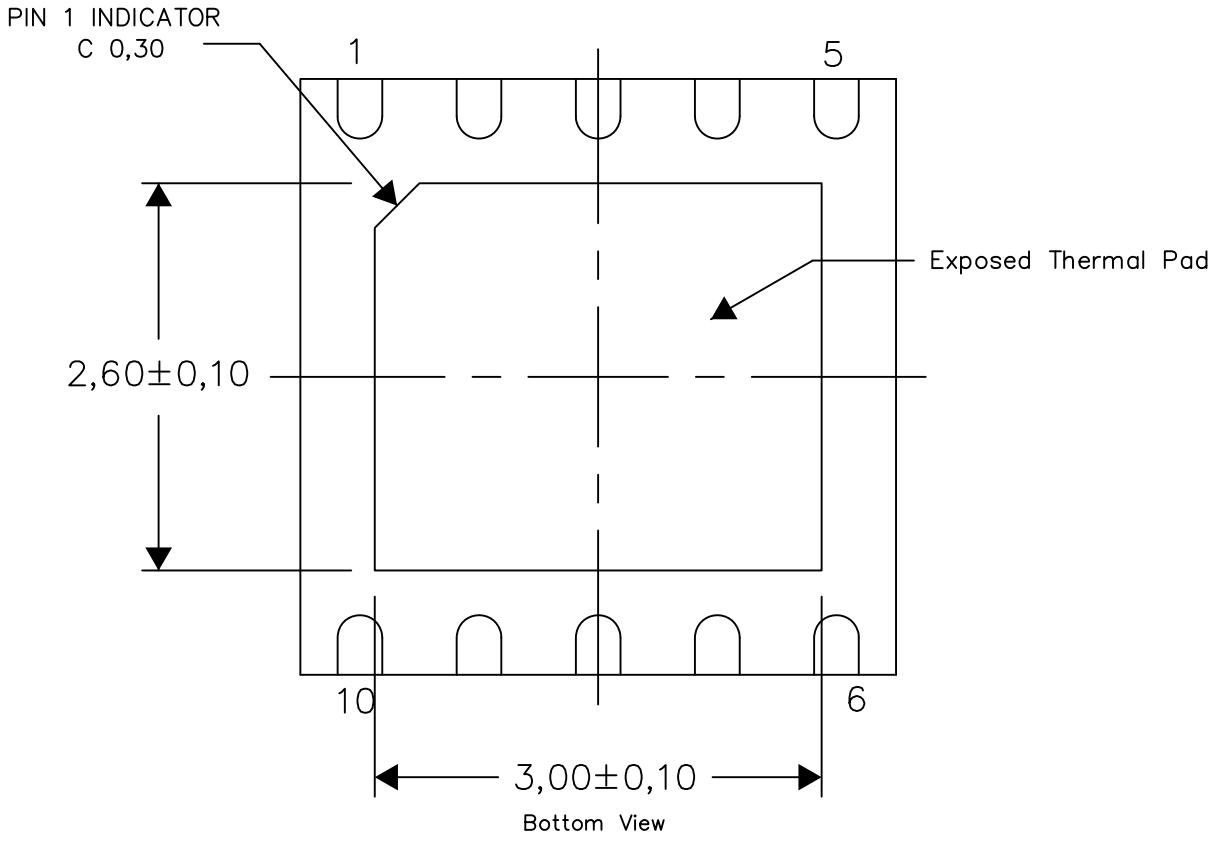
DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

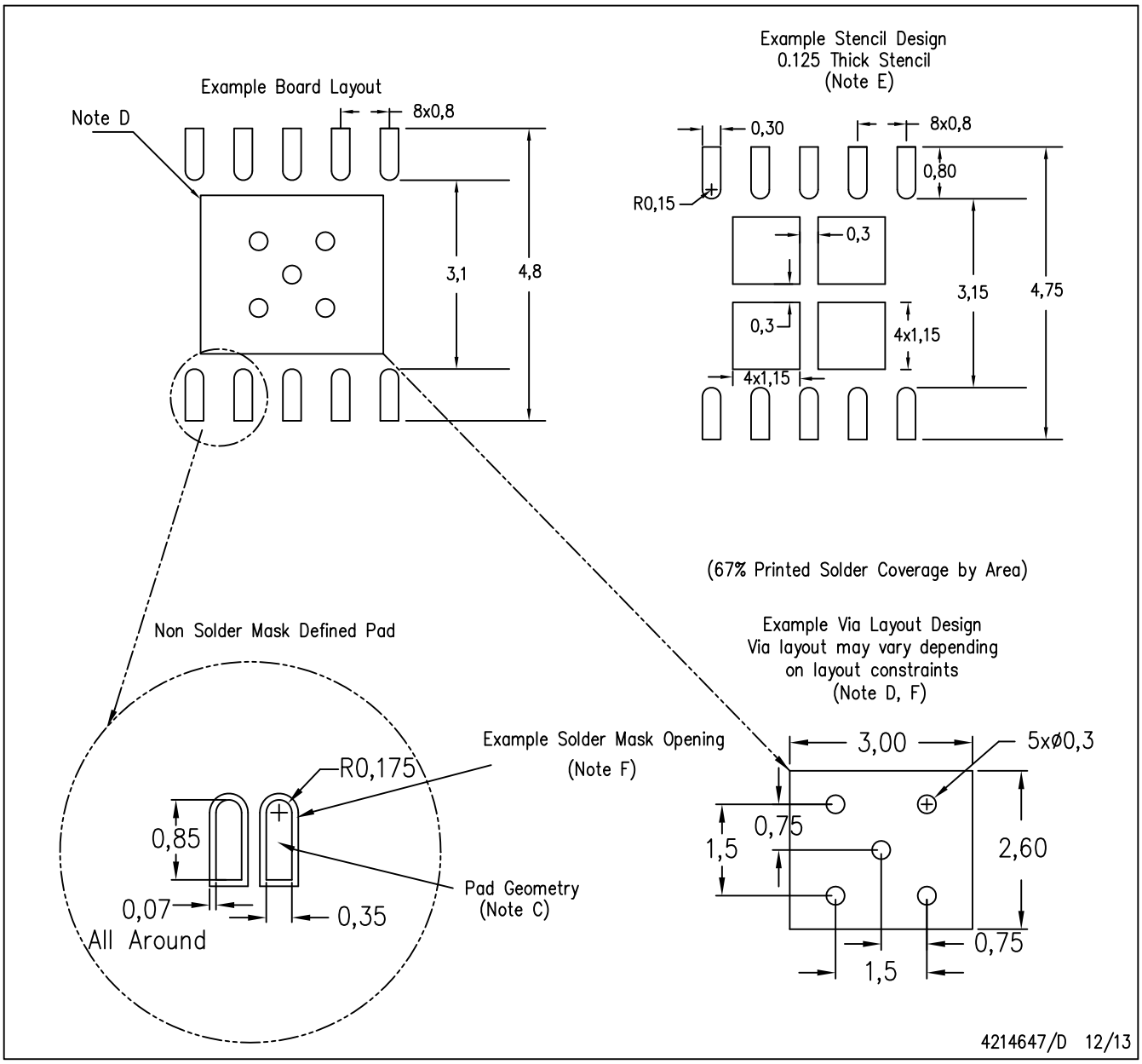



Exposed Thermal Pad Dimensions

4211551/C 12/13

NOTES: All linear dimensions are in millimeters

# DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265