# Digital Control Compatible Synchronous-Buck Gate Driver With Current Sense and Fault Protection

**Check for Samples: UCD7232**

## FEATURES

- **Dual High Current Drivers.**
- **Full Compatibility with TI Fusion Digital Power Supply Controllers, such as UCD91xx and UCD92xx Families**
- **Operational to 2 MHz Switching Frequency**
- **High-Side FET and Output Current Limit Protection with Independently Adjustable Thresholds**
- **Fast High-Side Overcurrent Sense Circuit with Fault Flag Output – Prevents Catastrophic Current Levels on a Cycle-by-Cycle Basis**
- **Differential High-Gain Current Sense Amplifier**
- **Voltage Proportional to Load Current Monitor Output**
- **Wide Input Voltage Range: 4.7 V to 15 V Operation to 2.2 V Input Supported with an External 4.5-6.5 V Bias Supply**
- **Onboard Regulated Supplies for Gate Drive and Internal Circuits**
- **Integrated Thermal Shutdown**
- **Selectable Operation Modes:**
  - **PWM plus Synchronous Rectifier Enable (SRE) with Automatic Dead-Time Control**
  - **Direct High-Gate and Low-Gate Inputs for Direct FET Control**
- **3-State PWM Input for Power Stage Shutdown**
- **UVLO Housekeeping Circuit**
- **Rated from –40°C to +125°C Junction Temperature**

## APPLICATIONS

- **Digitally-Controlled Synchronous-Buck Power Stages for Single- and Multi-Phase Applications**
- **Digitally-Controlled Power Modules**

## DESCRIPTION

The UCD7232 high current driver is specifically designed for digitally-controlled, point-of-load, synchronous buck switching power supplies. Two driver circuits provide high charge and discharge current for the high-side NMOS switch and the low-side NMOS synchronous rectifier in a synchronous buck circuit. The MOSFET gates are driven by an internally regulated $V_{GG}$ supply. The internal $V_{GG}$ regulator can be disabled to permit the user to supply their own gate drive voltage. This flexibility allows a wide power conversion input voltage range of 2.2 to 15 V. Internal under voltage lockout (UVLO) logic insures $V_{GG}$ is good before allowing chip operation.

A drive logic block allows operation in one of two modes selected by the SRE Mode pin. In Synchronous Mode, the logic block uses the PWM signal to control both the high-side and low-side gate drive signals. Dead time is automatically adjusted to prevent cross conduction. The Synchronous Rectifier Enable (SRE) pin controls whether or not the low-side FET is turned on when the PWM signal is low. In Independent Mode, the PWM and SRE pins control the high-side and low-side gates directly. No anti-cross-conduction logic is used in this mode.

On-board comparators monitor the voltage across the high side switch and the voltage across an external current sense element to safeguard the power stage from sudden high current loads. Blanking delay is set for the high side comparator by a single resistor in order to avoid false reports coincident with switching edge noise. In the event of a high-side fault or an over-current fault, the high-side FET turned off and the Fault Flag (FLT) is asserted to alert the digital controller. The fault thresholds are independently set by the HS Sense and ILIM pins.

Output current is measured and monitored by a precision, high gain, switched capacitor differential amplifier that processes the voltage present across an external current sense element. The amplified signal is available for use by the digital controller on the $I_{MON}$ pin. The current sense amplifier has output offset of 0.5 V so that both positive (sourcing) and negative (sinking) current can be sensed.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

An on-chip temperature sense monitors the die temperature. If it exceeds approximately 165°C, the temperature sensor will initiate a thermal shutdown that halts output switching and sets the FLT flag. The temperature fault automatically clears when the die temperatures falls by approximately 20°.

## FUNCTIONAL BLOCK DIAGRAM

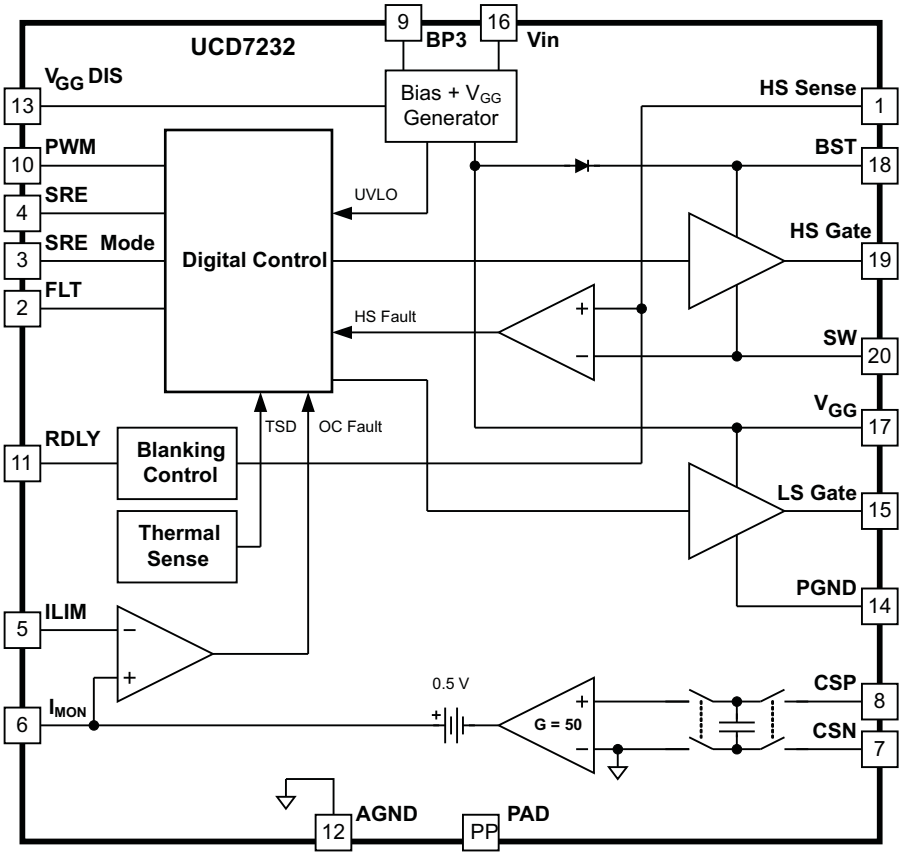



**Figure 1. UCD7232 Block Diagram**

## SIMPLIFIED APPLICATION DIAGRAM

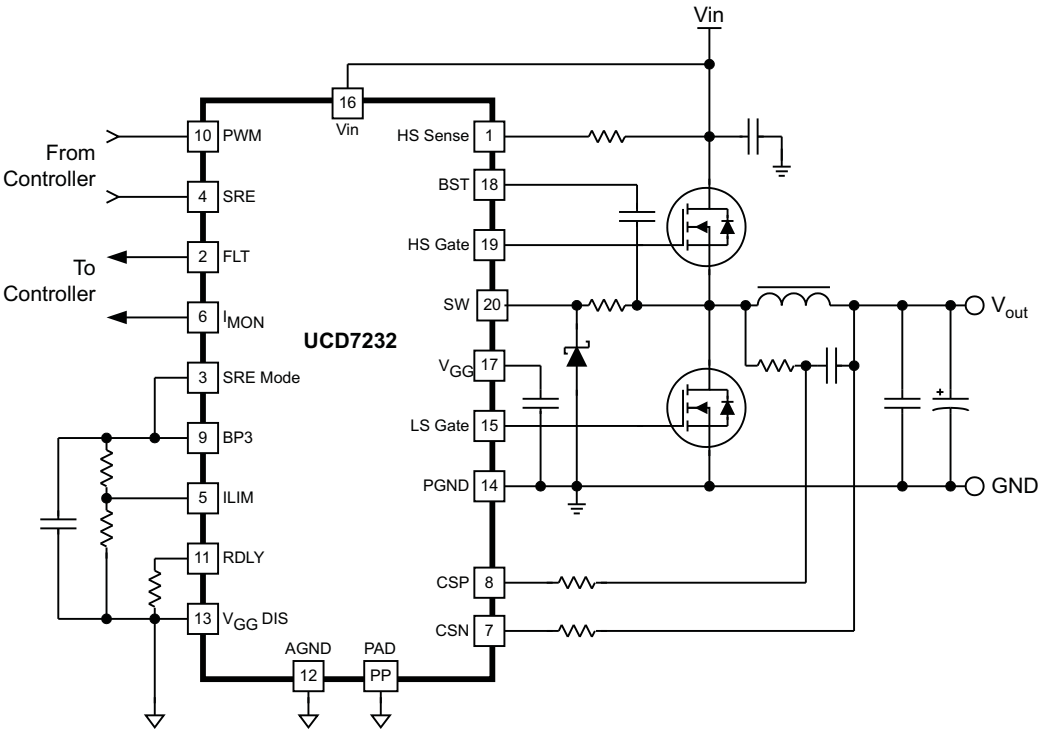
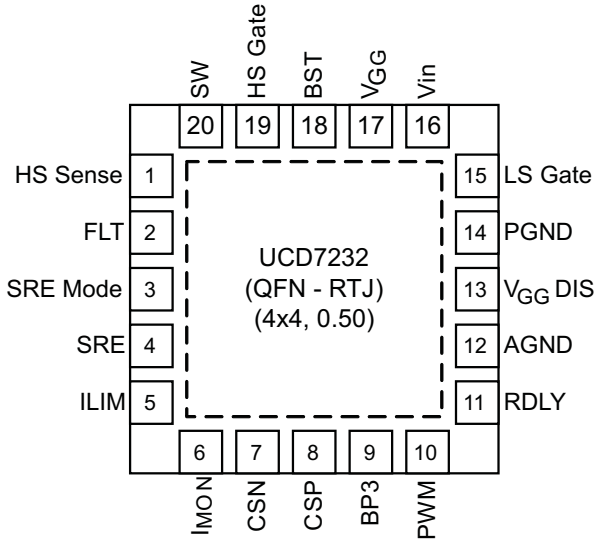



**Figure 2. Typical Synchronous Buck Power Stage**

## CONNECTION DIAGRAM




### ORDERING INFORMATION

| TEMPERATURE RANGE | PACKAGE | TAPE AND REEL QTY | PART NUMBER |
|---|---|---|---|
| –40°C to +125°C | Plastic QFN-20 (RTJ) | 250 | UCD7232RTJT |
| | | 2500 | UCD7232RTJR |

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Supply voltage, $V_{IN}$ | | –0.3 | 16 | V |
| Bootstrap voltage | $V_{BST}$ DC | –0.3 | 23 | V |
| | $V_{BST}$ Pulse ($V_{SW}$at 20V < 400ns) | –0.3 | 27 | |
| | $V_{BST}$ Pulse ($V_{SW}$at 22V < 64ns) | –0.3 | 29 | |
| | $V_{BST}$ Pulse ($V_{SW}$at 30V < 16ns) | –0.3 | 37 | |
| Gate drive supply voltage | $V_{GG}$ (Externally supplied) | –0.3 | 7 | V |
| Output gate drive voltage | HS Gate – SW | –0.3 | 7 | V |
| | LS Gate | PGND – 0.3 | $V_{GG}$+0.3 | |
| Switch node voltage | $V_{SW}$ DC | –1 | 16 | V |
| | $V_{SW}$ Pulse < 400 ns, E = 20 µJ | –2 | 20 | |
| | $V_{SW}$ Pulse < 64 ns | –5 | 22 | |
| | $V_{SW}$ Pulse < 16 ns | –10 | 30 | |
| Analog inputs | CSP, CSN, RDLY | –0.3 | 5.6 | V |
| | ILIM | –0.3 | 3.6 | |
| | HS Sense | –0.3 | 16 | |
| Digital inputs | PWM, SRE, SRE Mode | –0.3 | 5.6 | V |
| | $V_{GG}$ DIS | –0.3 | 3.6 | |
| Analog outputs | $I_{MON}$ | –0.3 | 3.6 | V |
| Digital outputs | FLT | –0.3 | 3.6 | V |
| ESD Rating | Human body model | | 2000 | V |
| | Charged device model | | 500 | |
| Operating ambient temperature, $T_A$ | | –40 | 125 | °C |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{STG}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to AGND. Currents are positive into, negative out of the specified terminal. Consult company packaging information for thermal limitations and considerations of packages.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | UCD7232 | UNITS |
|---|---|---|---|
| | | RTJ (20 PINS) | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 38.2 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 34.4 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 15.7 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 15.7 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 5.9 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Power Input Voltage (Internally generated $V_{GG}$) | 4.7 | 12 | 15 | V |
| $V_{IN}$ | Power Input Voltage (Externally supplied $V_{GG}$) | 2.2 | – | 15 | V |
| $V_{GG}$ | Externally supplied gate drive voltage | 4.6 | 6 | 6.5 | V |
| $T_J$ | Operating junction temperature range | –40 | – | 125 | °C |

## ELECTRICAL CHARACTERISTICS

$V_{IN}$ = 12V, 4.7 µF from $V_{GG}$ to PGND, 1 µF from BP3 to AGND, 0.22 µF from BST to SW, $T_A = T_J$ = –40°C to 125°C, RDLY = 8.06kΩ, SRE Mode = 3.3V, $V_{GG}$ DIS tied to AGND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY SECTION** | | | | | | |
| | Supply current | Outputs not switching, $V_{IN}$ = 5 V, PWM = LOW | | 8 | 10 | mA |
| | Supply current | Outputs not switching, $V_{IN}$ = 15 V, PWM = LOW | | 8 | 10 | mA |
| **GATE DRIVE UNDER-VOLTAGE LOCKOUT** | | | | | | |
| $V_{GG}$ | UVLO OFF | $V_{GG}$ rising | | 4.4 | 4.6 | V |
| $V_{GG}$ | UVLO ON | $V_{GG}$ falling | 4.1 | 4.3 | | V |
| $V_{GG}$ | UVLO hysteresis | | | 80 | | mV |
| **$V_{GG}$ SUPPLY GENERATOR** | | | | | | |
| $V_{GG}$ | | $V_{IN}$ ≥ 7 V, I_$V_{GG}$ ≤ 100 mA | 5 | | | V |
| | | $V_{IN}$ = 12 V, I_$V_{GG}$ ≤ 80 mA | 5.6 | 6.2 | 6.8 | V |
| | Dropout | $V_{IN}$ = 4.75 V, I_$V_{GG}$ ≤ 100 mA | | | 350 | mV |
| **DIGITAL INPUT SIGNALS (PWM, SRE)** | | | | | | |
| $V_{IH\_PWM}$ | Positive-going input threshold voltage | | | 1.8 | 2 | V |
| $V_{IL\_PWM}$ | Negative-going input threshold voltage | | 0.80 | 0.90 | | V |
| PWM | Input voltage hysteresis, ($V_{IH} – V_{IL}$) | | | 0.90 | | V |
| $V_{IH\_SRE}$ | Positive-going input threshold voltage | | | 1.5 | 1.7 | V |
| $V_{IL\_SRE}$ | Negative-going input threshold voltage | | 0.9 | 1.00 | | V |
| SRE | Input voltage hysteresis, ($V_{IH} – V_{IL}$) | | | 0.45 | | V |
| $I_{PWM}$ | Input current | $V_{PWM}$ = 5 V | | 140 | | µA |
| | | $V_{PWM}$ = 3.3 V | | 70 | | |
| | | $V_{PWM}$ = 0 V | | –63 | | |
| $I_{SRE}$ | Input current | $V_{SRE}$ = 5 V | | 190 | | µA |
| | | $V_{SRE}$ = 3.3 V | | 12 | | |
| | | $V_{SRE}$ = 0 V | | –330 | | |
| $t_{HLD\_R}$ | 3-state hold-off time (1) | $V_{PWM}$ transition from 0 V to 1.65 V, Time until $V_{LS\ Gate}$ falls to 0 V | 450 | 600 | 750 | ns |
| $t_{HLD\_R}$ | 3-state recovery time (1) | $V_{PWM}$ transition from 1.65 V to 0 V, Time until $V_{LS\ Gate}$ rises to $V_{GG}$ | 150 | 330 | 500 | ns |
| $t_{min}$ | PWM minimum pulse to force HS gate pulse (1) | $C_L$ = 3 nF at HS gate, VPWM = 3.3 V | 50 | | | ns |
| | PWM frequency (1) | $Qg_{HS}$ + $Qg_{LS}$ < 46 nC, $V_{GG}$ = 6.4 V | | | 2 | MHz |
| **OUTPUT CURRENT LIMIT (ILIM)** | | | | | | |
| | ILIM Input impedance (1) | | | 250 | | kΩ |
| | ILIM set point range (1) | | 0.5 | | 3 | V |
| | FLT output high level | $I_{LOAD}$ = –2 mA | 2.7 | 3.3 | | V |
| | FLT output low level (1) | $I_{LOAD}$ = 2 mA | | 0.1 | 0.6 | V |
| $t_{FAULT\_HS}$ | Fault detection time. Delay until HS Gate falling. (1) | $V_{(ILIM)}$ = 1.50 V, (CSP – CSN) = 20 mV, CSN = 1.80 V | | 100 | 150 | ns |
| $t_{FAULT\_LS}$ | Fault detection time. Delay until LS Gate rising. (1) | $V_{(ILIM)}$ = 1.50 V, (CSP – CSN) = 20 mV, CSN = 1.80 V | | 150 | 200 | ns |

(1) As designed and characterized. Not 100% tested in production.

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN}$ = 12V, 4.7 µF from $V_{GG}$ to PGND, 1 µF from BP3 to AGND, 0.22 µF from BST to SW, $T_A = T_J$ = –40°C to 125°C, RDLY = 8.06kΩ, SRE Mode = 3.3V, $V_{GG}$ DIS tied to AGND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{FAULT\_FLT}$ | Fault detection time. Delay until FLT asserted(2) | $V_{(ILIM)}$ = 1.50 V, (CSP – CSN) = 20 mV, CSN = 1.80 V | | 85 | 170 | ns |
| | Propagation delay from PWM to reset FLT(2) | PWM falling to FLT falling after a current limit event is cleared. PWM pulse width ≥100 ns. | | 85 | 200 | ns |
| **CURRENT SENSE BLANKING (RDLY, HS Sense)** | | | | | | |
| $I_{RDLY}$ | RDLY source current | 8.06 kΩ resistor from RDLY to AGND | 80 | 90 | 100 | µA |
| | RDLY resistance range(2) | | 7.5 | 8.06 | 10 | kΩ |
| $t_{BLANK}$ | HS blanking time | RDLY = 8.06 kΩ. From SW rising to HS fault comparator enabled | 110 | 125 | 140 | ns |
| $I_{HS\ Sense}$ | HS Sense sink current | $R_{HS\ Sense}$ = 2. kΩ to $V_{IN}$, $V_{IN}$ = 12 V | | 100 | | µA |
| $t_{HSFAULT\_HS}$ | HS fault detection time. Delay after $t_{BLANK}$ until HS Gate falling(2) | RDLY = 8.06 kΩ, $R_{HS\ Sense}$ = 2 kΩ to $V_{IN}$, $V_{IN}$ = 12 V, $V_{IN} – V_{SW}$ = 220 mV | | 20 | | ns |
| $t_{HSFAULT\_LS}$ | HS fault detection time. Delay after $t_{BLANK}$ until LS Gate falling(2) | RDLY = 8.06 kΩ, $R_{HS\ Sense}$ = 2 kΩ to $V_{IN}$, $V_{IN}$ = 12 V, $V_{IN} – V_{SW}$ = 220 mV | | 30 | | ns |
| **CURRENT SENSE AMPLIFER ($I_{MON}$, CSP, CSN)** | | | | | | |
| | $V(I_{MON})$ at no load | CSP = CSN = 1.8 V | 460 | 500 | 540 | mV |
| | Closed loop DC gain | CSP – CSN = 10 mV; 0.5 V ≤ CSN ≤ 3.3 V | 48 | 50.2 | 52.4 | V/V |
| | | Gain with 2.49k resistors in series with CSP, CSN | 45.6 | 47.8 | 49.9 | V/V |
| | Input impedance(2) | Differential, CSP – CSN | | 100 | | kΩ |
| $V_{CM}$ | Input common mode voltage range(2) | $V_{CM}$(max) is limited to ($V_{GG}$ – 1.2 V) | –0.3 | | 5.6 | V |
| $V(I_{MON})_{MIN}$ | | CSP = 1.2 V; CSN = 1.3 V; $I(I_{MON})$ = –250 µA | | 0.1 | 0.15 | V |
| $V(I_{MON})_{MAX}$ | | CSP = 1.3 V; CSN = 1.2 V; $I(I_{MON})$ = 500 µA | 3 | 3.2 | 3.3 | V |
| | Sampling Rate(2) | | | 5 | | Msps |
| **LOW-SIDE OUTPUT DRIVER (LS Gate)** | | | | | | |
| | Peak Source Current(2) | $V_{GG}$ = 6.2 V, PWM = Low, LS Gate = 3 V | | 6 | | A |
| | Peak Sink Current (2) | $V_{GG}$ = 6.2 V, PWM = High, LS Gate = 3 V | | 6 | | A |
| $t_{RL}$ | Rise Time(2) | $C_L$ = 6 nF, $V_{IN}$ = 12 V, $V_{GG}$ = 6.2 V | | 30 | | ns |
| $t_{FL}$ | Fall Time(2) | $C_L$ = 6 nF, $V_{IN}$ = 12 V, $V_{GG}$ = 6.2 V | | 20 | | ns |
| | Output with $V_{GG}$ <UVLO (2) | $V_{GG}$ = 1 V, Isink = 10 mA | | 0 | 0.5 | V |
| | Propagation Delay from PWM to LS Gate(2) | $C_L$ = 3 nF, PWM falling SW = 0 V, $V_{GG}$ = 6.2 V | | 46 | | ns |
| **HIGH-SIDE OUTPUT DRIVER (HS Gate)** | | | | | | |
| | Source current(2) | $V_{IN}$ = 12 V, BST = 6.2 V, PWM = High, HS Gate = 3 V | | 4 | | A |
| | Sink current(2) | $V_{IN}$ = 12 V, BST = 6.2 V, PWM = Low, HS Gate = 3 V | | 4 | | A |
| $t_{RH}$ | Rise time(2) | $C_L$ = 3 nF HS Gate to SW, $V_{GG}$ = 6.2 V | | 27 | | ns |
| $t_{FH}$ | Fall time(2) | $C_L$ = 3 nF HS Gate to SW, $V_{GG}$ = 6.2 V | | 21 | | ns |
| | Propagation delay from PWM to HS Gate(2) | $C_L$ = 3 nF HS Gate to SW, PWM rising, SW = 0 V, $V_{GG}$ = 6.2 V | | 50 | | ns |
| **SWITCHING TIME** | | | | | | |
| $t_{DLH}$ | HS gate turn-off propagation delay(2) | $C_L$ = 3 nF | | 16 | | ns |
| $t_{DLL}$ | LS gate turn-off propagation delay(2) | $C_L$ = 3 nF | | 15 | | ns |
| $t_{DTH}$ | Dead time LS; Gate off to HS; Gate on(2) | $C_L$ = 3 nF | | 12 | | ns |
| $t_{DTL}$ | Dead time HS; Gate off to LS; Gate on(2) | $C_L$ = 3 nF | | 15 | | ns |
| **BOOTSTRAP DIODE** | | | | | | |
| $V_F$ | Forward voltage(2) | Forward bias current 100 mA | | 0.4 | | V |
| **THERMAL SHUTDOWN** | | | | | | |
| | Rising threshold(2) | | 155 | 165 | 175 | °C |
| | Falling threshold(2) | | 135 | 145 | 155 | °C |
| | Hysteresis(2) | | | 20 | | °C |

(2) As designed and characterized. Not 100% tested in production.

## PIN FUNCTIONS

| PIN | | I/O | FUNCTION |
|---|---|---|---|
| QFN-20 | NAME | | |
| 1 | HS Sense | I | High-side current fault threshold set pin. A resistor is connected from this pin directly to the drain of the high-side FET. The voltage drop across this resistor sets the maximum voltage drop allowed across the high-side FET after the blanking time set by RDLY. Exceeding this threshold will assert FLT and truncate the HS Gate pulse. This pin sinks a constant 100µA of current. |
| 2 | FLT | O | Fault Flag. The FLT signal is a 3.3v digital output which is asserted high when an over-current, over-temperature, or UVLO fault is detected. After an over-current event is detected, the flag is reset low on the falling edge of the next PWM pin, provided the over-current condition is no longer detected during the on-time of the PWM signal. For UVLO and over-temperature faults, the flag is reset when the fault condition is no longer present. |
| 3 | SRE Mode | I | Synchronous Rectifier Enable Mode select pin. When high, the high-side and low-side gate drive timing is controlled by the PWM pin. Anti-cross-conduction logic prevents simultaneous application of high-side and low-side gate drive. When low, independent operation of the high-side and low-side gate is selected. The high-side gate is directly controlled by the PWM signal. The low-side gate is directly controlled by the SRE signal. No anti-cross-conduction circuitry is active in this mode. This pin should not be left floating. |
| 4 | SRE | I | Synchronous Rectifier Enable or Low-Side Input. This pin is a digital input capable of accepting 3.3V or 5V logic level signals. A Schmitt trigger input comparator desensitizes this pin from external noise. When SRE Mode is high, this signal, when low, disables the synchronous rectifier FET. The LS Gate signal is held off. When SRE Mode is high, this signal, when high, allows the LS Gate signal to function according to the state of the PWM pin. When SRE Mode is low, this pin is a direct input to the LS Gate driver. |
| 5 | ILIM | I | Output current limit threshold set pin. The voltage on this pin sets the fault threshold voltage on the $I_{MON}$ pin. The nominal threshold voltage range is 0.5 V to 3.0 V. When $V(I_{MON})$ exceeds $V_{(ILIM)}$, the FLT pin is asserted and the HS Gate pulse is truncated. |
| 6 | $I_{MON}$ | O | Current Sense Linear Amplifier Output. The output voltage level on this pin represents the average output current. $V(I_{MON}) = 0.5\ V + 50.2\ (V(CSP) – V_{(CSN)})$. |
| 7 | CSN | I | Inverting input of the output current sense amplifier and current limit comparator. |
| 8 | CSP | I | Non-inverting input of the output current sense amplifier and current limit comparator. |
| 9 | BP3 | O | Bypass capacitor for internal 3.3V supply. Connect a 1µF (minimum) ceramic capacitor from this pin to AGND. |
| 10 | PWM | I | PWM input. This pin is a digital input capable of accepting 3.3 V or 5 V logic level signals. A Schmitt trigger input comparator desensitizes this pin from external noise. When SRE Mode is high, this pin controls both gate drivers. When SRE Mode is low, this pin only controls the high-side driver. This pin can detect when the input drive signal has switched to a high impedance (3-state) mode. When the high impedance mode is detected, both the HS Gate and LS Gate signals are held low. |
| 11 | RDLY | I | Requires a resistor to AGND for setting the Current Sense blanking time for the high-side current sense comparator and output current limit circuitry. |
| 12 | AGND | – | Analog ground return for all circuits except the LS Gate driver. |
| 13 | $V_{GG}$ DIS | I | $V_{GG}$ Disable pin. When pulled high, the on-chip $V_{GG}$ linear regulator is disabled. When disabled, an externally supplied gate voltage must be connected to the $V_{GG}$ pin. Connect this pin to AGND to use the on-chip regulator. |
| 14 | PGND | – | Power Ground pin. This pin provides a return path for the low-side gate driver. |
| 15 | LS Gate | O | The Low-Side high-current driver output. Drives the gate of the low-side synchronous MOSFET between $V_{GG}$ and PGND. |
| 16 | Vin | I | Input Voltage to the buck power stage and driver circuitry |
| 17 | $V_{GG}$ | I/O | Gate Drive voltage supply. When $V_{GG}$ DIS is low, $V_{GG}$ is generated by an on-chip linear regulator. Nominal output voltage is 6.2 V. When $V_{GG}$ DIS is high, an externally supplied gate voltage can be applied to this pin. Connect a 4.7 µF capacitor from this pin to PGND. |
| 18 | BST | I/O | Floating bootstrap supply for high side driver. Connect the bootstrap capacitor between this pin and the SW node. The bootstrap capacitor provides the charge to turn on the high-side MOSFET. |
| 19 | HS Gate | O | The High-Side high-current driver output. Drives the gate of the high side buck MOSFET between BST and SW. |
| 20 | SW | I/O | Switching node connection to buck inductor. This pin provides a return path for the high-side gate driver. |
| PP | PAD | – | Power Pad. Connect directly to AGND for better thermal performance and EMI reduction. |

# DETAILED DESCRIPTION

## GENERAL

The UCD7232 is designed primarily to be a synchronous buck driver with current measurement and fault detection capabilities that make it an ideal partner with digital power controllers. This device incorporates two high-current gate drive stages and sophisticated current measurement circuitry that allows for the monitoring and reporting of output load current. Two separate fault detection blocks protect the power stage from excessive load current or short circuits. On-chip thermal shutdown protects the device in case of severe over-temperature conditions. Detected faults immediately truncate the power conversion cycle in progress, without controller intervention, and assert a digital fault flag (FLT). Gate drive voltage is supplied by an on-chip linear regulator. If desired, this regulator can be disabled and an external gate drive voltage can be supplied. Mode selection pins allow the device to be used in synchronous mode or independent mode. In synchronous mode, the high-side and low-side gate timing is controlled by a single PWM input. Anti-cross-conduction dead-time intervals are applied automatically to the gate drives. In independent mode, the high-side and low-side gate drive signals are controlled directly by the PWM and SRE pins. The automatic dead-time logic is disabled in this mode. When operating in synchronous mode, the use of the low-side FET can be disabled under the control of the SRE pin. This feature facilitates start-up into a pre-bias voltage and is also used in some applications to reduce power consumption at light loads.

## PWM INPUT

The PWM input pin accepts the digital signal from the controller that represents the desired high-side FET on-time duration. This input is designed to accept 3.3V logic levels, but is also tolerant of 5V input levels. The SRE Mode pin sets the behavior of the PWM pin. When the SRE Mode pin is asserted high, the device is placed in synchronous mode. In this mode, the timing duration of the high-side gate drive and the low-side gate drive are both controlled PWM input signal. When PWM is high, the high-side gate drive (HS Gate) is on and the low-side gate drive (LS Gate) is off. When PWM is low, the high-side gate drive is off and the low-side gate drive is on. Automatic anti-cross-conduction logic monitors the gate to source voltage of the FETs to verify that the proper FET is turned off before the other FET is turned on. When the SRE Mode pin is asserted low, the device is placed in independent mode. In this mode the PWM input only controls the high-side gate drive. When PWM is high, the high-side gate drive is on. The low side FET in independent mode is directly controlled by the SRE pin. No anti-cross-conduction logic is active in independent mode. The user must insure that the PWM and SRE signals do not overlap.

The PWM input supports a 3-state detection feature. It can detect if the PWM input signal has entered a 3-state mode. When 3-state mode is detected, both the high-side and low-side gate drive signals are held off. To support this mode, the PMW input pin has an internal pull-up resistor of approximately 50kΩ to 3.3V. It also has a 50kΩ pull-down resistor to ground. During normal operation, the PWM input signal swings below 0.8V and above 2.5V. If the source driving the PWM pin enters a 3-state or high impedance state, the internal pull-up/pull-down resistors will tend to pull the voltage on the PWM pin to 1.65V. If the voltage on the PWM pin remains within the 0.8V to 2.5V 3-state detection band for longer than the $t_{HLD\_R}$ 3-state detection hold-off time, then the device enters 3-state mode and turns both gate drives off. This behavior occurs regardless of the state of the SRE Mode and SRE pins. When exiting 3-state mode, PWM should first be asserted low. This will insure that the bootstrap capacitor is recharged before attempting to turn on the high-side FET.

The logic threshold of this pin typically exhibits 900mV of hysteresis to provide noise immunity and insure glitch-free operation of the gate drivers.

## SRE INPUT

The SRE (Synchronous Rectifier Enable) pin is a digital input with an internal 10kΩ pull-up resistor to 3.3V. It is designed to accept 3.3V logic levels, but is also tolerant of 5V levels. The SRE Mode pin sets the behavior of the SRE pin. When the SRE Mode pin is asserted high, the device is placed in synchronous mode. In this mode, the input, when asserted high, enables the operation of the low-side synchronous rectifier FET. The state of the low-side gate drive signal is governed by the PWM input. When SRE is asserted low while in synchronous mode, the low-side FET gate drive is continuously held low, keeping the FET off. While held off, current flow in the low-side FET is restricted to its intrinsic body diode. When the SRE Mode pin is asserted low, the device is placed in independent mode. In this mode, the state of the low-side gate drive signal follows the state of the SRE signal. It is completely independent of the state of the PWM signal. No anti-cross-conduction logic is active in independent mode. The user must insure that the PWM and SRE signals do not overlap.

The logic threshold of this pin typically exhibits 450mV of hysteresis to provide noise immunity and insure glitch-free operation of the low-side gate driver.

## SRE MODE

The SRE Mode pin is a digital input designed to accept 3.3V logic levels, but is also tolerant of levels up to 5V. This pin sets the operational mode on the device. When asserted high, the device will be placed in synchronous mode. In this mode the behavior of both the high-side and low-side gate drive signals are under the control of the PWM input. When asserted low, this pin configures the device for independent mode. In this mode the high-side FET is under the control of the PWM pin. The low-side FET is under the control of the SRE pin. The SRE Mode pin is designed to be permanently tied high or low depending on the power architecture being implemented. It is not intended to be switched dynamically while the device is in operation. This pin can be tied to the BP3 pin to always select synchronous mode.

### $V_{IN}$

$V_{IN}$ supplies power to the internal circuits of the device. The input power is conditioned by an internal linear regulator that provides the $V_{GG}$ gate drive voltage. A second regulator that operates off of the $V_{GG}$ rail produces an internal 3.3V supply that powers the internal analog and digital functional blocks. The BP3 pin provides access for a high frequency bypass capacitor on this internal rail. The $V_{GG}$ regulator produces a nominal output of 6.2V. The output of the $V_{GG}$ regulator is monitored by the Under-Voltage Lock-Out (UVLO) circuitry. The device will not attempt to produce gate drive pulses until the $V_{GG}$ voltage is above the UVLO threshold. This insures that there is sufficient voltage available to drive the power FETs into saturation when switching activity begins. To use the internal $V_{GG}$ regulator, the voltage on Vin should be at least 4.7V.

When performing power conversion with less than 4.7V on the $V_{IN}$ pin, the gate drive voltage must be supplied externally. (See $V_{GG}$ and $V_{GG}$ DIS sections for details.)

### $V_{GG}$

The $V_{GG}$ pin is the gate drive voltage for the high current gate drivers stages. The voltage on this pin can be supplied internally by the on-chip regulator, or it can be externally supplied by the user. When using the internal regulator, the $V_{GG}$ DIS pin should be tied low. When an external source of $V_{GG}$ is to be used, the $V_{GG}$ DIS pin must be tied high. Current is drawn from the $V_{GG}$ supply in fast, high-current pulses. A 4.7µF ceramic capacitor should be connected from the $V_{GG}$ pin to the PGND pin as close as possible to the package.

Whether internally or externally supplied, the voltage on the $V_{GG}$ pin is monitored by the UVLO circuitry. The voltage must be higher than the UVLO threshold before power conversion can occur. Note that the FLT pin is asserted high when $V_{GG}$ is below the UVLO threshold.

The average current drawn from the $V_{GG}$ supply is dependant on the switching frequency and the total gate charge of the power FETs connected to the driver. This current can be significant and is a major contributor to the overall power dissipation of the driver. The total gate charge (Qg) is a function of the value of $V_{GG}$ and the power FET construction. A value for Qg can be obtained from the FET manufacturer's data sheet. A graph of Qg vs $V_{GS}$ is usually supplied. Use the value of $V_{GG}$ as the $V_{GS}$ value and read the corresponding value of Qg. A value of Qg should be obtained for both the high-side and low-side FETs.

To keep the current draw from the $V_{GG}$ supply within its capability, the switching frequency of the power stage should be limited to the following:

$$F_{sw(max)} = \frac{92000}{Qg_{HS} + Qg_{LS}} \quad (1)$$

Where $F_{sw(max)}$ is the maximum switching frequency in kHz, $Qg_{HS}$ is the gate charge of the high-side FET measured at $V_{GS}$ = 6.2V, and $Qg_{LS}$ is the total gate charge of the low-side FET(s) measured at $V_{GS}$ = 6.2V, both specified in nanocoulombs (nC). Selecting FETs with lower gate charge will permit higher operating frequencies. The formula above allows for a maximum of 92mA of total gate drive current. An additional 8mA is consumed by the remaining circuitry within the device.

The average gate drive current, in mA, can be calculated from the following equation (with switching frequency in kHz and charge in nC):

$$I_{GATE\_AVE} = (Qg_{HS} + Qg_{LS}) \times Fsw \times 1000 \quad (2)$$

Assuming $V_{GG}$ = 6.2V and Fsw = 500kHz, a typical Qg for a low-side FET is 50nC. A typical high-side FET Qg is 13nC. This combination creates an $I_{GATE\_AVE}$ of 31.5mA. If the switching frequency was doubled, the current draw would double to 63mA. If $V_{IN}$ = 12V and the internal $V_{GG}$ linear regulator is being used, the power dissipation in the $V_{GG}$ regulator, for this case, at 500kHz operation, is 183mW. At 1MHz, it increases to 365mW. Keep in mind that this is not the total power dissipation of the driver, only the portion dissipated in the $V_{GG}$ regulator. Good thermal layout techniques are required for this device.

### $V_{GG}$ DIS

This pin, when asserted high, disables the on-chip $V_{GG}$ linear regulator. When tied low, the $V_{GG}$ linear regulator is used to derive $V_{GG}$ from $V_{IN}$. This pin is designed to be permanently tied high or low depending on the power architecture being implemented. It is not intended to be switched dynamically while the device is in operation.

### SW

The SW pin connects to the switching node of the power conversion stage. It acts as the return path for the high-side gate driver. When configured as a synchronous buck stage, the voltage swing on SW normally traverses from below ground to well above $V_{IN}$. A power Schottky diode should be connected from this pin to PGND to clamp the negative voltage swing on this pin to less than 1V. A series 1Ω resistor connects this pin to the actual switching node. It acts as a current limiting resistor when the Schottky diode is clamping negative voltage swings. The diode should be rated for at least 0.5A of current and exhibit a breakdown voltage of at least 30V. Small-signal Schottky diodes should not be used.

Parasitic inductance in the high-side FET and the output capacitance (Coss) of both power FETs form a resonant circuit that can produce high frequency (>100MHz) ringing on this node. The voltage peak of this ringing, if not controlled, can exceed twice $V_{IN}$. Care must be taken to not allow the peak ringing amplitude to exceed twice the value of the input voltage, even if that voltage amplitude is within the Absolute Maximum rating limit for the pin. In many cases, a series resistor and capacitor snubber network connected from the switching node to PGND can be helpful in damping the ringing and decreasing the peak amplitude. It is recommended that provisions for snubber network components be provided during the layout of the printed circuit board. If testing reveals that the ringing amplitude at the SW pin exceeds twice $V_{IN}$, then the snubber components need to be populated.

### BST

The BST pin provides the drive voltage for the high-side FET. A bootstrap capacitor is connected from this pin to the SW node. Internally, a diode connects the BST pin to the $V_{GG}$ supply. In normal operation, when the high-side FET is off and the low-side FET is on, the SW node is pulled to ground and, thus, holds one side of the bootstrap capacitor at ground potential. The other side of the bootstrap capacitor is clamped by the internal diode to $V_{GG}$. The voltage across the bootstrap capacitor at this point is the magnitude of the gate drive voltage available to switch-on the high-side FET. The bootstrap capacitor should be a low ESR ceramic type, with a recommended minimum value of 0.22µF. A minimum voltage rating of 16V or higher is recommended.

### HS GATE

The HS Gate signal directly drives the gate of the high-side power FET. It provides high current drive to charge the gate capacitance of the FET rapidly to insure that it makes the transition from off to on as quickly as possible to minimize switching losses. When commanded on, the HS Gate is driven to the BST pin potential. As the FET begins to turn on, the SW will quickly rise to the $V_{IN}$ potential. This voltage swing is coupled by the bootstrap capacitor to the BST pin. The net result is that the BST pin voltage, and thus the HS Gate voltage, is always equal to $V_{SW}$ + $V_{GG}$. As the FET gate charges, the current return path for the driver is provided by the SW pin. When the HS Gate is commanded off, the driver pulls the pin to the SW potential. As the FET turns off, the SW pin will swing quickly to slightly below ground. Once again, this voltage swing is coupled to the BST pin by the bootstrap cap. The HS Gate circuitry is referenced to the SW pin and floats with the SW signal swing. The circuitry loop from the HS Gate pin to the gate of the FET and from the source of the high-side FET to the SW pin should kept as small and tight as possible to limit stray inductance. Likewise, the loop from the BST pin to the bootstrap capacitor and back to the SW pin should be kept small and tight.

## LS GATE

The LS Gate signal directly drives the gate of the low-side power FET. It provides high current drive to quickly charge the gate capacitance of the FET, which is often considerably larger than the high-side FET. When commanded on, the LS Gate is driven to the $V_{GG}$ pin potential. The current return path for the driver is provided by the PGND pin. When commanded off, the LS Gate pin is driven to the PGND potential. The traces from the LS Gate and the PGND pins to the low-side FET gate and source pins should be short and wide to minimize parasitic inductance and resistance.

## CSP, CSN

These pins are the input to the differential current sense amplifier. The Current Sense Positive (CSP) pin connects to the non-inverting input, the Current Sense Negative (CSN) connects to the inverting input. This amplifier provides the means to monitor and measure the output current of the power stage. The circuitry can be used with a discrete, low value, series current sense resistor, or can make use of the popular inductor DCR sense method.

The DCR method is illustrated in Figure 3. A series resistor and capacitor network is added across the buck stage power inductor. It can be shown that when the value of L/DCR is equal to RC, then the *voltage* developed across the capacitor, C, is a replica of the voltage waveform the *ideal current* would induce in the dc resistance (DCR) of the inductor. This method does *not* detect changes in current due to changes in inductance value caused by saturation effects. The value used for C should be in the 0.1µF to 2.2µF range. This keeps the impedance of the sense network low, which reduces its susceptibility to noise pickup from the switching node. The trace lengths of the CSP and CSN signals should be kept short and parallel. To aid in rejection of high frequency common-mode noise, a series 2.49k resistor should be added to both the CSP and CSN signal paths, with the resistors being placed close to the pins at the package. This small amount of additional resistance slightly lowers the current sense gain.

Power inductors are selected for the lowest possible DCR to minimize losses. Typical DCR values range from 0.5mΩ to 5mΩ. With a load current of 20A, the voltage presented across the CSP and CSN pins is only in the range of 10mV to 100mV. Keep in mind that this small differential signal is riding on a large common mode signal that is the dc output voltage. This makes the current sense signal challenging to process.

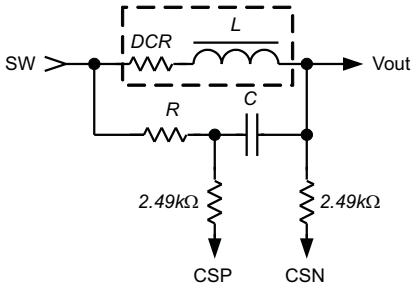



**Figure 3. DCR Current Sense**

The UCD7232 uses switched capacitor technology to perform the differential to single-ended conversion of the sensed current signal. This technique offers excellent common mode rejection. The differential CSP-CSN signal is amplified by a factor of 97.8 and then a fixed 500mV pedestal voltage is added to the result. This signal is presented to the $I_{MON}$ pin.

When using inductors with DCR values of 2mΩ or higher, it may be necessary to attenuate the input signal to prevent saturation of the current sense amplifier. This is easily accomplished through the addition of resistor R2 as shown in Figure 4.

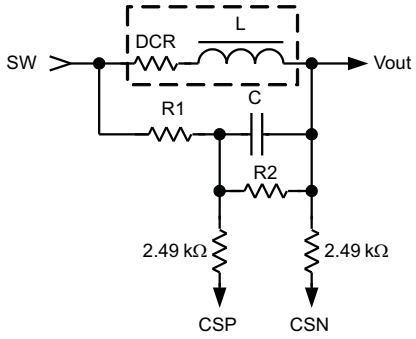



**Figure 4. Attenuating the DCR Sense Signal**

The amount of attenuation is equal to R2/(R1 + R2). The equivalent resistance value to use in the L/DCR = RC formula is the parallel combination of R1 and R2. Thus, when using the circuit of Figure 4,

$$L/DCR = C \times R1 \times R2/(R1 + R2) \quad (3)$$

### $I_{MON}$

The $I_{MON}$ signal is a voltage proportional to the output current delivered by the power stage. The voltage magnitude obeys the following equation when using the circuit of Figure 3. This equation takes into account the gain reduction caused by the series 2.49k resistors.

$$V(I_{OUT}) = 0.5 + 47.8 \times DCR \times I_{LOAD} \quad (4)$$

If the calculated value of $V(I_{MON})$ exceeds the range of the analog-to-digital converter (ADC) or, if used, the maximum fault comparator threshold limit of a controller monitoring this voltage, then the circuit of Figure 4 should be used. When using the circuit of Figure 4, the voltage on $I_{MON}$ obeys this modified equation:

$$V(I_{OUT}) = 0.5 + 47.8 \times DCR \times I_{LOAD} \times \left(\frac{R2}{R1 + R2}\right) \quad (5)$$

In either case, the output voltage is 500mV at no load. Current that is sourced to the load causes the $I_{MON}$ voltage to rise above 500mV. Current that is forced into the power stage (sinking current) is considered "negative" current and will cause the $I_{MON}$ voltage to fall below 500mV. The usable dynamic range of the $I_{MON}$ signal is approximately 100mV to 3.1V. Keep in mind that this signal swing could exceed not just the maximum range of an analog to digital converter (ADC) that may be used to read or monitor the $I_{MON}$ signal, but also the maximum programmable limit for the fault OC threshold. For example, the UCD92xx family of digital controllers has maximum limit of 2.5V for the ADC converter and 2.0V for the fault OC threshold, even though the input pin can tolerate voltages up to 3.3V.

The $I_{MON}$ voltage is internally fed to the non-inverting input of the output over-current fault comparator. Good practice dictates that the over-current threshold should be set at approximately 150% of the rated power stage output current plus one half of the peak-to-peak inductor ripple current. This mandates that the $I_{MON}$ signal should remain within its linear dynamic range at this threshold load current level. This requirement may force the use of the attenuation circuit of Figure 4. Note that the $I_{MON}$ voltage (that goes to the output over-current fault comparator) is held during the blanking interval set by the resistor on the RDLY pin. This means that the $I_{MON}$ pin will not reflect output current changes during the blanking interval, and that a fault will not be flagged until the blanking interval terminates.

### ILIM

The ILIM pin feeds the inverting input of the output over-current fault comparator. The voltage applied to this pin sets the over-current fault threshold. When the voltage on the $I_{MON}$ pin exceeds the voltage on this pin, a fault is flagged. The voltage on this pin can be set by a voltage divider, a DAC, or by a filtered PWM output. The usable voltage range of the ILIM pin is approximately 0.6V to 3.1V. This represents the linear range of the $I_{MON}$ signal for sourced output current. When using a voltage divider to set the threshold, a (0.01µF) capacitor to BP3 can be added to improve noise immunity.

## RDLY

The RDLY pin sets the blanking time of the high-side fault detection comparator. A resistor to AGND sets the blanking time according to the following formula, where $t_{BLANK}$ is in nanoseconds and RDLY is in kΩ. Values of RDLY of greater than 25kΩ should not be used.

$$RDLY = \frac{t_{BLANK} - 33}{11.413} \quad (6)$$

To calculate the nominal blanking time for a given value of resistance, use the formula below.

$$t_{BLANK} = 11.413 \times RDLY + 33 \quad (7)$$

The blanking interval begins on the rising edge of SW. During the blanking time the high-side fault comparator is held off. A high-side fault is flagged when the voltage drop across the high-side FET exceeds the threshold set by the HS Sense pin. Blanking is required because the high amplitude ringing that occurs on the rising edge of SW would otherwise cause false triggering of the fault comparator. The required amount of blanking time is a function of the high-side FET, the PCB layout, and whether or not a snubber network is being used. A value of 125ns is a typical starting point. An RDLY of 8.06kΩ will provide 125ns of blanking. The blanking interval should be kept as short as possible, consistent with reliable fault detection. The blanking interval sets the minimum duty cycle pulse width where high-side fault detection is possible. When the duty cycle of the PWM pulses are narrower than the blanking time, the high-side fault detection comparator is held off for the entire on-time and is, therefore, blind to any high-side faults.

Internally, the RDLY pin is fed by a 90µA current source. When using the default value of 8.06kΩ, the voltage observed on the RDLY pin will be approximately 725mV.

## HS SENSE

A resistor from the HS Sense pin to the drain of the high-side FET sets the high-side fault detection threshold. When the high-side FET is on, the current flow in the FET produces a voltage drop across the device. The magnitude of this voltage is equal to the $R_{DS(ON)}$ times the current through the FET. An absolute maximum current level can be set during the design stage and the resultant voltage drop across the FET can be calculated. This maximum voltage drop, $\Delta V_{MAX}$, sets the high-side fault threshold.

Internally, a high speed comparator monitors the voltage between the SW pin and the HS Sense pin when the high-side FET is on. Whenever the voltage on the SW pin is lower than the voltage on the HS Sense pin, a fault is flagged. To prevent false tripping during the ringing that accompanies the rising edge of SW, the output of the comparator is held off (blanked) for a time interval set by the RDLY pin. The voltage on the HS Sense pin is set by a resistor connected from the pin to the high-side FET drain. The HS Sense resistor value is calculated from the following formula, where $\Delta V_{MAX}$ is in mV, and $R_{HS\ Sense}$ is in kilohms.

$$R_{HS\ Sense} = \Delta V_{MAX} / 100 \quad (8)$$

For example, if $\Delta V_{MAX}$ is 100mV, then $R_{HS\ Sense}$ is 1kΩ.

The equation can be restated as follows, with $R_{HS\ Sense}$ in kilohms, $R_{DS(ON)}$ in milliohms, and $I_{MAX}$ in amps:

$$R_{HS\ Sense} = R_{DS(ON)HOT} \times I_{MAX}) / 100 \quad (9)$$

The value of $I_{MAX}$ should be set to approximately 150% of the expected maximum steady-state current. This allows some headroom to avoid nuisance fault events due to transient load currents and the inductor ripple current. Also, keep in mind that the $R_{DS(ON)}$ of a FET has a large positive temperature coefficient of approximately 4000ppm/°C. The junction temperature of the FET will be elevated when operating at currents near the $I_{MAX}$ threshold. In the equation above, use a value of $R_{DS(ON)HOT}$ that is approximately 140% of its typical room temperature value. When using the internal $V_{GG}$ gate drive supply, the FET, when turned on, is driven to a $V_{GS}$ enhancement voltage of approximately 6V. Most FET data sheets provide $R_{DS(ON)}$ values for $V_{GS}$ values of 4.5V and 10V. Do not use the $V_{GS}$ = 10V value for the room temperature $R_{DS(ON)}$ value. Some manufacturers provide a graph of $R_{DS(ON)}$ vs $V_{GS}$. If provided, use the $V_{GS}$ = 6V value for the room temperature $R_{DS(ON)}$ value.

A 100µA current sink pulls current through $R_{HS\ Sense}$. This sets up a reference voltage drop equal to $\Delta V_{MAX}$. It is important to connect the far end of the $R_{HS\ Sense}$ resistor directly to the drain of the high-side FET. This should be made with a separate, non-current-carrying trace. This insures that only the $R_{DS(ON)}$ of the FET influences the fault threshold and not the resistance of the pc board traces.

## FLT

The Fault Flag (FLT) is a digital output pin that is asserted when a significant fault is detected. It is meant to alert the host controller to an event that has interrupted power conversion. The FLT pin is held low in normal operation. When a fault is detected it is asserted high (3.3V). There are four events that can trigger the FLT signal: output over-current, high-side over-current, UVLO and thermal shutdown. The operation of the device during fault conditions is described in the Fault Behavior section. When asserted in response to an over-current fault, the FLT signal is reset low upon the falling edge of a subsequent PWM pulse, provided no faults are detected during the on-time of the pulse. If the fault is still present, the flag will remain asserted. When asserted in response to an UVLO or thermal shutdown event, the FLT pin will automatically de-assert itself when the UVLO or thermal event has passed. If the on-time of the PWM pulse is less than 100ns, then more than one pulse may be required to reset the flag.

## BP3

The BP3 pin provides a connection point for a bypass capacitor that quiets the internal 3.3V voltage rail. Connect a 1µF (or greater) ceramic capacitor from this pin to analog ground. Do not draw current from this pin. It is not intended to be a significant source of 3.3V. It can, however, be used to as a source of 3.3V for an ILIM voltage divider and a tie point for the SRE Mode pin. Current draw should be limited to 100µA or less.

## FAULT BEHAVIOR

When faults are detected, the device reacts immediately to minimize power dissipation in the FETs and protect the system. The type of fault influences the behavior of the gate drive signals.

When a thermal shutdown fault occurs, both HS Gate and LS Gate are immediately forced low. They will stay low, regardless of the state of PWM and SRE, for the duration of the thermal shutdown.

A UVLO fault occurs when the voltage on the $V_{GG}$ pin is less than the UVLO threshold. During this time both the HS Gate and LS Gate are driven low, regardless of the state of PWM and SRE. The fault is automatically cleared when the $V_{GG}$ voltage rises above the UVLO threshold.

When either a high-side fault or an output over-current fault is detected, the FLT pin is asserted high, and both gate signals are immediately pulled low. During a high-side fault, a high-side gate pulse will be issued with each incoming PWM pulse. If the fault is still present, the HS Gate signal will again be truncated. This behavior repeats on a cycle-by-cycle basis until the fault is gone or the PWM input is held low. This behavior is illustrated in Figure 5.

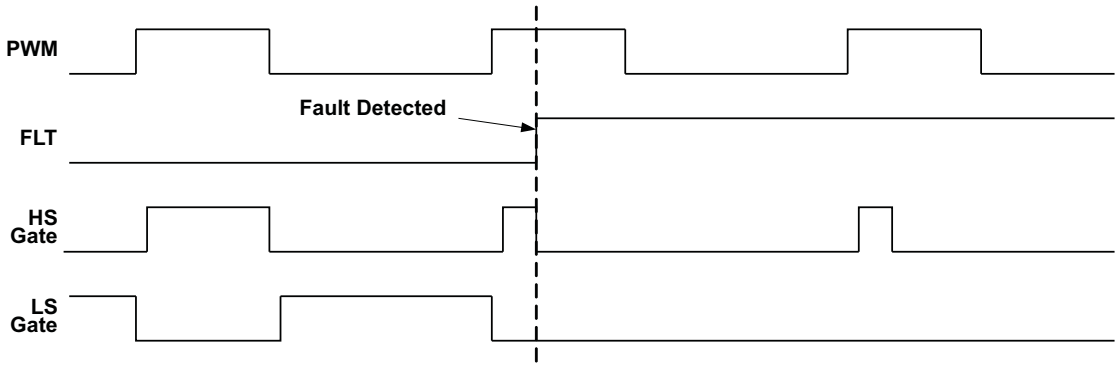



**Figure 5. High-Side Over-Current Fault Response**

When a high-side fault and output over-current fault are detected concurrently, then both FET drives are immediately turned off and held off. If the output over-current fault is still present at the next PWM rising edge, then no HS Gate pulse will be issued and both gates will continue to be held off. Unlike the high-side fault detection circuitry, the output over-current fault circuitry is not reset on a cycle-by-cycle basis. The output current must fall below the over-current threshold before switching will resume.

## FLT RESET

With the exception of a UVLO fault or a thermal shutdown fault, the FLT flag, once asserted, is cleared by subsequent PWM pulses. The FLT flag will be cleared on the falling edge of the next PWM pulse, provided a fault condition is not asserted during the entire on-time of the PWM pulse. If a fault is present or detected during the on-time interval, the FLT pin will remain asserted. This behavior is illustrated in Figure 6.

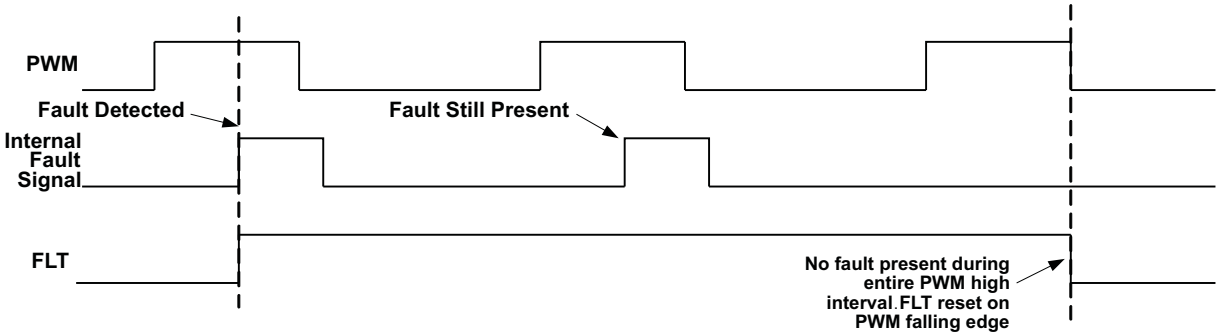



**Figure 6. FLT Reset Sequence**

Whenever the voltage on the $V_{GG}$ pin is below the UVLO falling threshold, as at the time of initial power-up, for example, the FLT pin will be asserted. When the voltage on the $V_{GG}$ pin rises above the UVLO rising threshold, the FLT pin will be cleared automatically. This permits the FLT pin to be used as a “Power Not Good” signal at initial power-up to signify that there is insufficient gate drive voltage available to permit proper power conversion. When FLT goes low, it is an indication of “Gate Drive Power Good” and power conversion can commence. After initial power-up, the assertion of the FLT flag should be interpreted that power conversion has stopped or has been limited by a fault condition.

## THERMAL SHUTDOWN

If the junction temperature exceeds approximately 165°C, the device will enter thermal shutdown. This will assert the FLT pin and both gate drivers will be turned off. When the junction temperature cools by approximately 20°C, the device will exit thermal shutdown. The FLT flag is reset upon exiting thermal shutdown.

Gate driver temperature will be strongly influenced by the switching frequency being used, the value of $V_{IN}$ and $V_{GG}$, and the total capacitive load on the HS Gate and LS Gate pins. The driver junction temperature is not normally strongly affected by load current. However, a rise in the PCB substrate temperature due to load current induced power dissipation in nearby components will raise the junction temperature and contribute to a possible thermal shutdown event.

## APPLICATION INFORMATION

### EXAMPLE 20A POWER STAGE

A partial schematic of a 20A power conversion stage designed for 500kHz operation is shown in Figure 7.

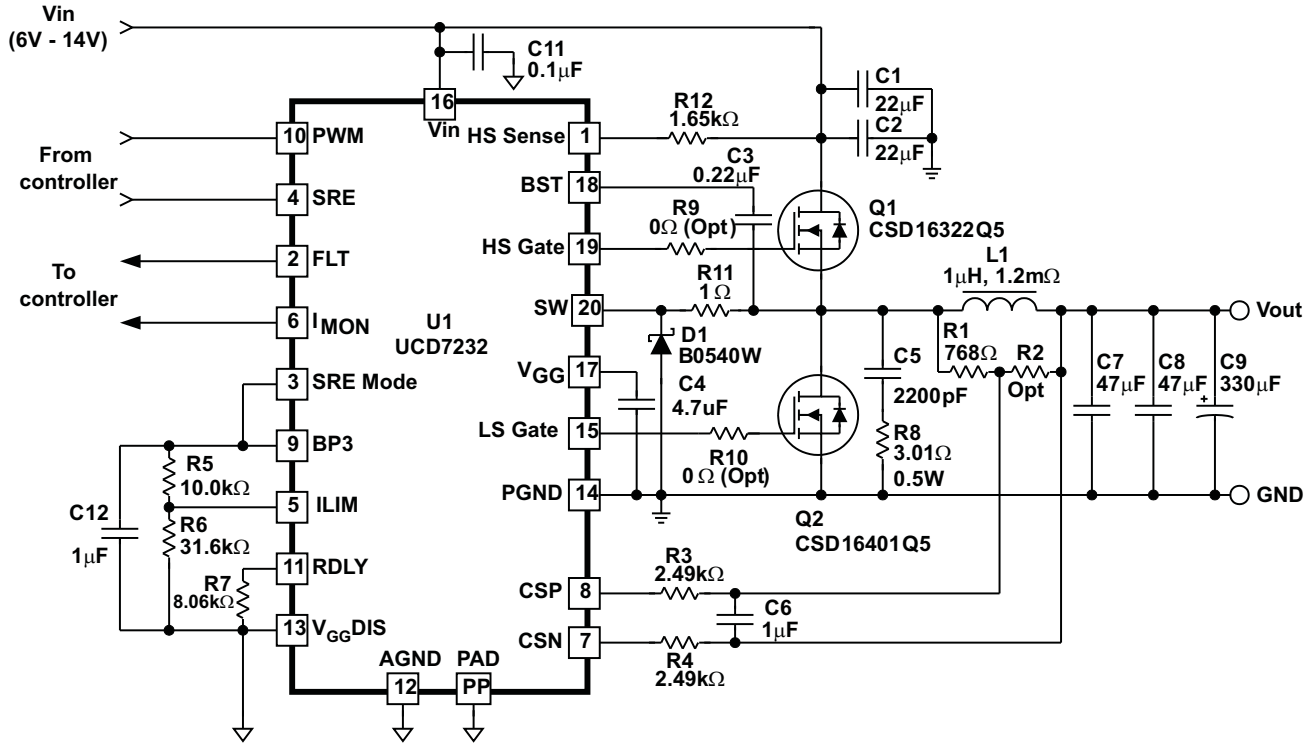



**Figure 7. Example 20A Power Stage**

This power stage has been designed to operate with a nominal input voltage of 12V. It will perform well with input voltages from 6V to 14V. The output voltage range is assumed to be 3.3V or lower. It has been configured to use the internal $V_{GG}$ supply and operate strictly in synchronous mode. The controller and voltage feedback components are not shown. This design works well with any of the UCD92xx family of Digital Power Controllers.

The first step in designing the power stage is selecting a nominal operating frequency. Lower switching frequencies will reduce FET switching losses and driver gate currents, but will require higher inductor values to keep inductor ripple current within reasonable values. Higher switching frequencies allow for smaller inductor values, which likely reduces their physical size and DCR, but higher FET switching losses and gate drive power may offset the efficiency gains achieved from reduced inductor DCR. 500kHz is a good starting point for power stages in the 15A to 25A range.

### INDUCTOR SELECTION

Once a switching frequency has been selected, an appropriate inductance value can now be selected. Ripple current and saturation current are the two key parameters that drive inductor value selection. Ripple current is the ac variation of the current through the inductor. It is superimposed on the average dc (load) current flowing through the inductor. High values of ripple current cause increased core losses in the inductor, and require more low ESR capacitance to keep the output ripple voltage to acceptable levels. Limit the inductor ripple current to approximately 30% of the rated dc load current. The peak-to-peak ripple current in an inductor determined by the voltage across the inductor, the time duration of that applied voltage, and the value of the inductor.

$$\Delta I_{PP} = V_L \times \Delta t / L \quad (10)$$

In a switching regulator, this equation can be rewritten to use the duty-cycle and switching frequency of the high-side FET to calculate the ripple current.

$$\Delta I_{PP} = [(V_{IN} - V_{OUT}) \times V_{OUT}] / (V_{IN} \times F_{SW} \times L) \quad (11)$$

For a synchronous buck regulator, the ripple current is highest at 50% duty cycle, or when Vout is one half of Vin. At higher or lower duty cycles, the ripple current decreases.

For this design, the maximum output current is targeted to be 20A. If the 30% ripple current rule is applied, the maximum allowable ripple current is $6A_{PP}$. The previous equation can be rearranged to use this value to compute a minimum inductance value that will meet our criteria.

$$L_{MIN} = [(V_{IN} – V_{OUT}) \times V_{OUT}] / (V_{IN} \times F_{SW} \times \Delta I_{MAX}) \quad (12)$$

For this design, the maximum ripple occurs when Vin = 14V and Vout is at the highest targeted output voltage of 3.3V. This produces a value for $L_{MIN}$ of 0.84µH. This value is rounded up to 1µH, which is a popular value that is available from inductor vendors.

Now that the inductance value has been determined, the current handling capacity of the inductor drives the next step in the selection process. The inductor saturation limit and DCR heating limit are two key parameters. At full load, the peak current in the inductor is equal to the load current plus one half of the $\Delta I_{PP}$ value. For this design, the peak inductor current is approximately 23A. The inductor must have a saturation current rating, $I_{SAT}$, of at least 23A. The inductor saturation rating is the current level at which the inductance value falls by 20 or 30% (depending on the vendor) from its no-load value. As current increases above this value, the inductance value may fall sharply, depending on the core material and construction of the inductor. Operating an inductor in its saturated region causes the current through it to increase rapidly, causing potentially damaging levels of current to flow in the high-side FET. Good engineering practice dictates that there be should be 15% or more headroom in the inductor saturation limit to allow for transient currents and surges that will be encountered in normal operation. For this design, an $I_{SAT}$ rating of at least 1.15 × 23A = 26.5A would be required.

For highest efficiency, an inductor with the lowest DCR will always have the lowest $I^2R$ losses. However, low resistance requires wire with a large cross section. This forces the inductor to be physically larger than a higher DCR device. The DCR of the inductor will limit its current handling capacity due to the heating it will cause when current flows through it. Inductor manufacturers typically give a maximum current rating for an inductor based on the current that produces a 40°C rise in the device temperature. Keep in mind that in an 85°C ambient environment, a 40°C rise will result in a device temperature of 125°C. Every inductor has two maximum current ratings: one is the 40°C rise rating, the other is the $I_{SAT}$ rating. The maximum usable current rating for the inductor is the lower of the two values. In a well designed inductor, the 40°C rise rating and $I_{SAT}$ are approximately equal. The 40°C rise rating should be at least equal to the maximum steady state load current of the power stage. Headroom above the steady state 40°C rise rating is not required. Momentary surge currents above the rating value will not cause a significant temperature rise due to the thermal mass of the part.

The last key inductor consideration is the choice of core material. Core material affects cost, power dissipation due to core loss, and saturation characteristics. There are three popular core materials used in power inductors: powdered iron, ferrite, and powdered alloy. Powder iron is inexpensive and has a desirable soft saturation characteristic that makes it tolerant of surge and transient currents. However, at high values of ripple current and higher switching frequencies (500kHz and up), core losses become quite large. The heating due to core loss is in addition to the $I^2R$ heating due to the winding DCR. Excessive core loss can cause the core temperature to rise dramatically. In some cases, this can lead to permanent degradation of the core. Powdered iron cores are best used at switching frequencies at or below 350kHz. Ferrite has the lowest core losses, making it ideal for higher switching frequencies. Ferrite saturates easily, so ferrite based inductors are produced with some form of air gap that lowers their effective permeability and extends their saturation limit. However, once the core reaches saturation, the falloff in inductance is quite steep. This dictates the selection of a device that has some extra $I_{SAT}$ headroom to allow for transient current surges. Ferrite is also the most costly core material. Powdered alloy cores are an improved version of powdered iron cores. By using more exotic metal mixtures in the core, alloy cores exhibit lower core loss at high frequencies and ripple currents compared to powered iron. In some cases, they approach the performance of ferrite. The powdered alloy cores retain the desirable soft saturation characteristic of powdered iron cores. Cost wise, powdered alloy usually falls between powdered iron and ferrite.

Now that the key inductor requirements are known, a device can be selected. In this design, a BI Technologies HM00-08822LFTR device, for example, meets the requirements. This is a 0.95µH device, with 1.2mΩ DCR. It uses a ferrite core with an $I_{SAT}$ rating of 29A.

## CALCULATING THE DCR CURRENT SENSE COMPONENTS

With an inductor selected, the next step is to calculate the value of the DCR current sensing components. While the inductor has a nominal room temperature resistance of 1.2mΩ, when in use, the winding temperature will be elevated. Copper has a positive temperature coefficient of 3800ppm/°C. If we assume a typical temperature rise of 20°, then the winding resistance will increase by 7.6% to approximately 1.3mΩ. This DCR value will be used in the following calculations.

With 20A of load current through the inductor, the voltage drop due to the DCR will be 1.3 × 20 = 26mV. This will be amplified by a factor of 48 by the current sense amplifier within the UCD7232. This will boost the signal to 1.25V. The internal circuitry then adds a 0.5V pedestal to the amplified signal which results in 1.75V at the $I_{MON}$ pin. This voltage is within the 2.0V dynamic range of the current measurement and fault detection circuitry of the controller, so the design can make use of the current sense network shown in Figure 3. No attenuation of the signal is necessary. R2 in Figure 7 is not required and does not have to be loaded. (If a higher DCR inductor were selected, attenuation of the current sense signal might be required, and, in that case, R2 would be populated.)

The values for the current sense RC network (R1 and C6) around the inductor can now be calculated. The requirement is L/DCR = RC. Let C = 1µF. Using 1µH for L and the warm DCR value of 1.3mΩ for DCR, the calculated value for R is 769Ω. The nearest standard 1% value is 768Ω. Thus, C6 = 1µF and R1 = 768Ω.

The CSP and CSN pins are sensitive to noise pickup. Signal traces to these pins should be kept short and away from the switching node and the gate drive traces. They should be shielded by ground planes and adjacent ground fingers if possible. Series 2.49kΩ resistors R3 and R4 are added close to the CSP and CSN pins to help attenuate noise. Further reduction in noise can be achieved by placing the current sense capacitor, C6, close to R3 and R4.

## FET SELECTION

At a minimum, the FETs used in the power stage must have a $V_{DS}$ breakdown rating of at least 1.5 times the maximum input voltage. This headroom is required since the peak voltage on the switching node is always higher than the input voltage due to ringing caused by energy storage in the parasitic inductance of the FETs and the PCB traces. With good layout practices and the use of a snubber network, the peak voltage on the FETs can be limited to 1.5 times Vin. In this example, a minimum $V_{DS}$ rating of 21V is required to accommodate a 14V input voltage.

The high-side FET should be selected to handle current pulses equal to twice the steady state current rating of the power stage. This allows headroom for ripple current, load transients, and brief over-current events. Note that this is a pulsed current requirement, not a continuous current requirement. The average current in the high-side FET is roughly equal to the load current times the duty cycle. For this example, an $I_D$ peak current rating of 40A or higher is the target. The average current in the FET will be highest at full load, at the lowest input voltage and highest output voltage. In this example, $V_{IN}$(min) is 6V and Vout(max) is 3.3V. At full load, the average FET current will be 11A. Adding a 20% safety margin to this value produces a 13.2A steady state drain current requirement.

When converting power from input voltages of approximately 8V and higher, switching losses begin to dominate over conduction losses in the high-side FET. That means $R_{DS(ON)}$ is not the primary specification that drives high-side FET selection. Low gate charge (Qg), low gate-to-drain charge (Qgd), and low gate resistance (Rg) become more important parameters. One of the most useful figures of merit is the product of on-resistance and gate charge (Qg × $R_{DS(ON)}$). The lower the number, the better the FET.

FETs are characterized at several standard gate enhancement voltages. The most popular are $V_{GS}$ voltages are 4.5V and 10V. Since our design is using approximately 6V of gate drive, the datasheet values of $R_{DS(ON)}$ at 4.5$V_{GS}$ will be of greatest interest. Be cautious of FETs that are characterized at 2.5$V_{GS}$. These are low-threshold FETs that are useful when converting power at input voltages below 6V. However, due to subtle, but serious, side effects of the low threshold voltage, they are best avoided when converting power at voltages above 6V.

For this design the TI CSD16322Q5 is an excellent choice for the high-side FET (Q1). It has low charge, an impressive figure of merit, and low Qgd. It exhibits low switching losses. It is produced in an industry standard, thermally enhanced, 5 × 6mm package. It has more than enough current handling capability for this 20A design.

Low-side FET selection is driven primarily by $R_{DS(ON)}$. The lower the value, the higher the efficiency. Lower $R_{DS(ON)}$ requires a larger die size, which increases total gate charge and device cost. For a given $R_{DS(ON)}$ value, the part with the lowest Qg is likely to be the best choice. At higher input voltages and narrower duty cycles, the low-side FET is conducting current for the majority of switching cycle. A thermally enhanced package is a must. The continuous current rating of the FET should at least be equal to the current rating of the power stage.

The TI CSD16401Q5 is used as the low-side FET (Q2) in this design. It has an $R_{DS(ON)}$ of 1.5mΩ, with only 21nC of Qg at 4.5V. It has more than enough current handling capacity. Its 25V minimum $BV_{DSS}$ rating beats our minimum voltage criteria. It comes in the same 5 × 6mm package as Q1.

In rare instances, the addition of a series gate resistor can be of some benefit when dealing with high amplitude ringing. Usually, however, the addition of series gate resistance increases switching losses and increases the risk of cross-conduction between the high-side and low-side FETs. A tight, low stray inductance PCB layout, or a snubber network are the preferred methods for reducing ringing. Resistors R9 and R10 are shown as placeholders in Figure 7. They can be added to the PCB layout to allow for the possibility that series gate resistance may be needed. In most cases they are not required and can be considered optional. If they are added to the design, the default value of 0Ω should initially be used.

## SW NODE CLAMP

At higher output currents, the switching node can momentarily swing more than a 1V below ground. This condition can interfere with the proper operation of the chip. To prevent the SW pin from being subjected to excessive negative voltage swings, a Schottky diode clamp and current limiting resistor, D1 and R11, are inserted between the actual switching node and the SW pin (pin 20). Diode D1 should be a power Schottky device rated at a minimum of 0.5A of current and at least 30V breakdown voltage. The device shown in Figure 7 is a 0.5A, 40V device in a SOD123 package. The diode should be placed as close as possible to the UCD7232 and be connected between the SW pin and PGND pin by short, wide traces. Small-signal Schottky diodes should not be used. Their forward voltage drop at higher currents is too high to provide effective clamping. Use a value of 1Ω for R11. Larger values will interfere with the anti-cross conduction logic used to control the turn-on and turn-off of the high-side FET, Q1.

## SNUBBER NETWORK

Energy stored in the parasitic inductance in the source and drain leads of the power FETs is released when the FETs abruptly turn on and off. The parasitic inductance interacts with the output capacitance $C_{OSS}$) of the FETs to form a resonant circuit. The end result is high amplitude, high frequency ringing on the switching node that is most prominent just after the high-side FET is turned on. The frequency of the ringing is commonly in the 100MHz range. Its peak amplitude can be as much as twice the input voltage. If nothing is done to damp the ringing, it can cause avalanche breakdown of the low-side FET, increase radiated EMI levels, and, most important for this discussion, interfere with the detection of an over-current condition. When left undamped, the ringing on the switching node can take several hundreds of nanoseconds to die out.

A simple series RC network connected to the switching node is commonly used to dampen or “snub” the ringing. The capacitor couples the high frequency content to the resistor, and the resistor dissipates the energy. With the correct values, the ringing can be made to decay to negligible levels in 100ns or less. C5 (2200pF) and R8 (3.01Ω) perform this function in the example circuit. R8 must be capable of dissipating several hundred milliwatts of power. The amount of power dissipated in R8 is proportional to the switching frequency and the value of C5. With the values shown, R8 will dissipate approximately 125mW at 500kHz. This will double if the switching frequency is increased to 1MHz. It is recommended that a 500mW rated resistor be used for R8. The optimum values of the snubber R and C are device and layout dependant. Some experimentation may be needed to achieve the optimum trade-off between damping time and power lost in the damping resistor. In most cases, the value of R is between 1Ω and 10Ω, and C is between 1000pF and 4700pF. Higher values of C cause more current to flow in R which increases the power dissipated.

## COMPUTING VALUES FOR $R_{DLY}$ and $R_{HS\ Sense}$

$R_{DLY}$ sets the amount of blanking time for the high speed comparator that monitors the voltage drop across the high-side FET during its on-time. This comparator fires when the high-side FET is conducting too much current. Because of the time it takes for ringing to decay on the switching node, the comparator "decision" should be delayed for a short amount of time after the high-side FET is turned on. With a proper snubber network, a delay time of 100ns should be sufficient to allow for proper over-current detection. Using the formula in the RDLY section, value of 8.03kΩ produces a 100ns delay. The nearest standard value is 8.06kΩ, so this is the value used for R7.

Note that when the duty cycle is of shorter duration than the blanking time, the high-side fault sensing circuit is blanked for the entire time. Thus *there is no high-side FET protection when the duty cycle duration is shorter than the RDLY blanking time.* This condition commonly occurs during soft-start, when the output voltage is being ramped up from zero, or when operating at high switching frequencies and attempting to produce low output voltages from high input voltages. Keep this in mind when setting operating frequency and input to output voltage ratios.

The first step in selecting a value for $R_{HS\ Sense}$, is to determine what is the maximum allowable voltage drop across the high-side FET. This is calculated from the $R_{DS(ON)}$ of the FETs, taking into account its likely junction temperature when operating at the maximum current point, and by the maximum allowable FET current. The $R_{DS(ON)}$ value on the data sheet is specified at 25°C and at a particular $V_{GS}$ voltage, typically 4.5V and 10V. In this case, neither value is correct, since this design will applying approximately 6.2V to the gate. Additionally, FET $R_{DS(ON)}$ has a high, positive temperature coefficient of typically 4000ppm/°C. This means for a 100°C rise in junction temperature, the on-resistance will go up by 40%. For a fault condition, using a 125°C junction temperature is a reasonable assumption. A valid estimate of the $R_{DS(ON)}$ with 6V of enhancement at 125°C of the CSD16322Q5 is 5mΩ.

The second step is to calculate a maximum current value for the high-side FET. Use 150% of the rated output current value, plus one half of the peak-to-peak inductor ripple current. For this example this gives a value of 1.5 × 20 × ½ × 5 = 32.5A. This level of current provides headroom for transients, start-up surge currents, and the increase in inductor ripple current as the inductance falls with increasing current. The maximum allowable voltage drop can now be calculated as just the product of the maximum current value and the "hot" $R_{DS(ON)}$. This produces a value of 162.5mV for this design. This should not be regarded as a precision value. Keep in mind that the high-side FET protection is meant to be the last protection for the power stage to prevent catastrophic damage to the power train. The maximum voltage drop value should be set high enough to prevent nuisance trips of the protection circuitry under normal operation.

The value for $R_{HS\ Sense}$ can now be calculated. Its resistance, in kΩ, is equal to the maximum high-side voltage drop, in mV, divided by 100. In our example this produces a value of 1.63kΩ. Rounding this up to the nearest standard value of 1.65kΩ gives the value for R12.

## SETTING THE ILIM THRESHOLD

The primary fault protection mechanism in the UCD7232 is the output current detection circuitry. An internal comparator monitors the voltage on the ILIM and $I_{MON}$ pins. When the voltage on $I_{MON}$ exceeds the voltage on ILIM, the FLT pin is asserted and power conversion stops. If a UCD92xx controller is used to drive the power stage, it can also monitor the voltage on $I_{MON}$ and detect an over current condition. The threshold for the fault trip point is easily set by firmware, making it flexible. The maximum current sense input voltage that can be correctly digitally sampled by a UCD92xx controller is 2.5V. (The maximum programmable limit for the fast OC threshold is 2V.) For this design it was decided to use this 2.5V level as the threshold for the ILIM comparator. In this way the digitally programmable controller will detect a slowly changing OC fault, and the ILIM comparator in the driver will protect the system from a sudden increase in current. This corresponds to an output current of approximately 31A. All that needs to be done is to set up a voltage divider that will produce 2.5V at the ILIM pin. The BP3 pin provides a convenient source of clean, regulated 3.3V. The value of R5 was arbitrarily set to 10kΩ. Simple math produces a value of 31.6kΩ for R6. These values produce the desired 2.5V on ILIM. The voltage divider only draws 80µA from the BP3 pin, which is within the allowable limits.

## INPUT AND OUTPUT CAPACITORS

At the drain of the high-side FET, current is drawn in fast, brief, rectangular pulses. It is important to provide low impedance, high frequency energy storage right at the drain of the FET. For this 20A power stage, two 22µF, 16V or 25V ceramic capacitors are recommended. C1 and C2 should be placed as close to the drain of Q1 as possible. The ground side of the capacitors should be connected as close as possible to the source lead of Q2. If designing a multiphase power supply, these capacitors should be present at each power stage. Bulk input bypass capacitance may also be required to minimize voltage variations during transient loads. This bulk capacitance is not shown on Figure 7, but it is typically required. Bulk capacitance can be shared among multiple power stages.

The inductor ripple current must be absorbed by the output capacitors. The ripple current is triangular in shape and contains significant energy at the switching frequency and its harmonics. To keep the ripple voltage amplitude to a minimum, low ESR and low ESL capacitors must be used. Multilayer ceramic capacitors are ideal devices. While bulk capacitance is also required to provide energy storage during transient events, the bulk capacitors do not typically handle much ripple current because their higher ESL and ESR make them look inductive at the ripple frequencies.

The output ripple voltage is directly proportional to the inductor ripple current. The inductor ripple current varies widely with input voltage and duty cycle. That makes it difficult to come up with a one-size-fits-all recommendation for the proper amount of ceramic output capacitance. A good starting point is approximately 100µF. In this design two 47µF capacitors are used (C7 and C8). These capacitors should be placed close to the inductor, L1, and the ground side of these caps should be connected as close as possible to the source lead of the low-side FET, Q2.

Bulk capacitance is used not only for short term transient energy storage, but also as a frequency response tailoring element in the power supply feedback loop. Several hundred microfarads, at a minimum, are commonly used in a power stage of this current capability. In this example, 330µF is being used (C9). More capacitance may be required depending on the transient response requirements of the load.

## BYPASS AND BOOTSTRAP CAPACITORS

In this design, the bypass capacitors on BP3 (C12), $V_{GG}$ (C4), and the bootstrap capacitor (C3) use the recommended values. A high frequency 0.1µF bypass capacitor, C11, has also been added at the Vin pin of the UCD7232. This cap attenuates the high frequency noise that is present on the Vin rail. It should be placed as close as possible to pin 16 and connect to analog ground with a short, direct trace.

## LAYOUT RECOMMENDATIONS

Proper component placement and trace routing can have a significant impact on overall power stage efficiency and reduce noise coupling into nearby circuits. The following are some key layout considerations.

- Locate the driver as close as possible to the power FETs, but do not place it directly under either FET. The driver is a power device and needs its own thermal cooling path. Clustering multiple hot parts too close together can increase the risk of excessive temperature rise and potentially cause a thermal shutdown event.
- Locate the $V_{GG}$ bypass and bootstrap capacitors as close as possible to the driver.
- Pay special attention to the GND trace. The ground side of the input bypass capacitors, the ground side of the output capacitors, the low-side FET source leads, and the PGND connection to the driver should connected together in a tight “single point” ground, using wide, low inductance traces and few, if any vias. Use of a ground plane is strongly encouraged.
- Connect the power-pad on the bottom of the driver to analog ground. The power-pad is not intended to be a high current carrying connection. The analog ground and power ground should be connected together at one point, near the AGND pin. Care should be taken to insure that heavy currents are not pulled through the analog ground traces.
- The switching node trace should be kept short and compact. This is the noisiest node in the system with high dV/dt slew rates.
- Use wide traces for the HS Gate and LS Gate signals closely following the associated switching node and ground traces. Use 0.050” to 0.080” (1.27 to 2.03 mm) wide traces if possible. Use at least two vias if the gate drive trace has to be routed from one layer to another.
- Keep the low level input and output traces away from the switching node. The high dV/dt signal present there can induce significant noise into the relatively high impedance nodes. Pay particular attention to the routing of the CSP and CSN traces.

## INDUCTOR CURRENT SENSE TRACE LAYOUT

Since matching of the L/DCR to RC time constants is important to obtain an accurate replica of the inductor current, the PCB layout must be done correctly to insure that the voltage drop across the inductor is sensed properly. For best results, the current sensing connections should be made by separate, non-current-carrying traces that connect *directly* to the inductor solder pads. The sensing connections should *not* be made to current carrying traces that lead to the switching node or the output capacitors. An example of a correct and incorrect layout is given in Figure 8.

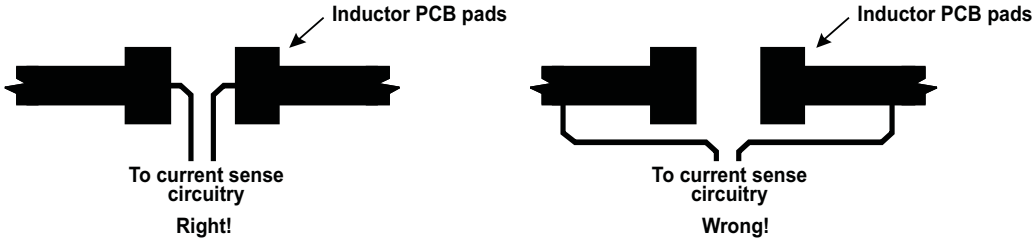



**Figure 8. Inductor Current Sense Trace Layout**

The current carrying traces have finite resistance that exhibit an additional voltage drop which will contaminate the sensed readings. It represents an additional DCR that is not taken into account in the current sensing equations. The trace resistance varies with the thickness of the PCB copper used on the board. This thickness can vary from batch to batch of pc boards, so the additional resistance of the traces is not a tightly controlled value. Even a short length of PCB trace can introduce a significant amount of added resistance. Remember, milliohms matter. By making a Kelvin connection to the inductor pads, the effects of PCB trace resistance can be minimized.

## LIMITATIONS OF DCR CURRENT SENSING

The accuracy of the DCR current sense method is limited by the stability of the DCR and L values of the power inductor. In practice, the inductance value of the power inductor decreases with increasing load current. Most inductors will exhibit a 20% to 30% reduction in inductance as load current changes from no load to full rated current. The DCR sense method *cannot* detect inductor saturation or a cracked core, both of which cause greatly increased ac current to flow in the inductor.

The resistance of the inductor windings is strongly affected by temperature. Most inductors use copper wire, and copper has a resistance temperature coefficient of approximately +3800ppm/°C. This means that if the winding temperature of the inductor rises by 40°C, its DCR will increase by 15.2%. This will cause the sensed voltage at CSP and CSN to increase by 15.2% as well for the same current flow. If high accuracy of measured current is important, then some form of temperature correction needs to be applied to the DCR sensed reading. This requires some form of temperature sensing and a method to correlate the sensed temperature to the actual winding temperature.

Since it is impractical to place a temperature sensor inside the inductor to sense the winding temperature, a practical alternative is to sense the high-side FET device temperature. Tests have shown that a small analog-output temperature sensor placed under the high-side FET on the back side of the board works well as a substitute. Its temperature output correlates strongly to the inductor winding temperature. The voltage proportional to temperature can be fed to the Temp input of the UCD92xx family of Digital Power Controllers. The firmware internal to the controller can use the temperature reading to correct for the temperature effects on the DCR current sense readings.

## RELATED PRODUCTS

| DEVICE | DESCRIPTION | LITERATURE NUMBER |
|---|---|---|
| UCD9240 | Digital Point of Load System Controller | SLUS766C |
| UCD9220 | Digital PWM System Controller | SLUS904 |
| UCD9112 | Digital Dual-Phase Synchronous Buck Controller | SLVS711C |

## RELATED LITERATURE

| DESCRIPTION | LITERATURE NUMBER |
|---|---|
| QFN/SON PCB Attachment | SLUA271A |
| Quad Flatpack No-Lead Logic Packages | SCBA017D |
| Reducing Ringing Through PCB Layout Techniques | SLPA005 |

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| UCD7232RTJR | Active | Production | QFN (RTJ) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD7232 |
| UCD7232RTJR.B | Active | Production | QFN (RTJ) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD7232 |
| UCD7232RTJT | Active | Production | QFN (RTJ) \| 20 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD7232 |
| UCD7232RTJT.B | Active | Production | QFN (RTJ) \| 20 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD7232 |
| UCD7232RTJTG4 | Active | Production | QFN (RTJ) \| 20 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD7232 |
| UCD7232RTJTG4.B | Active | Production | QFN (RTJ) \| 20 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD7232 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

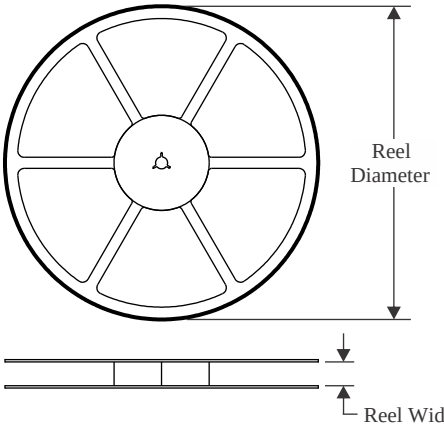
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

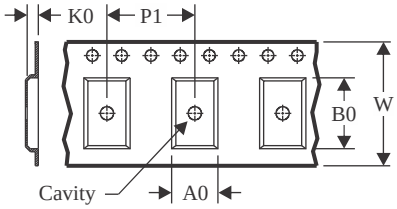
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

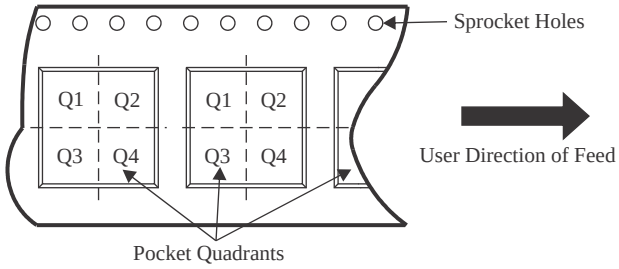



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

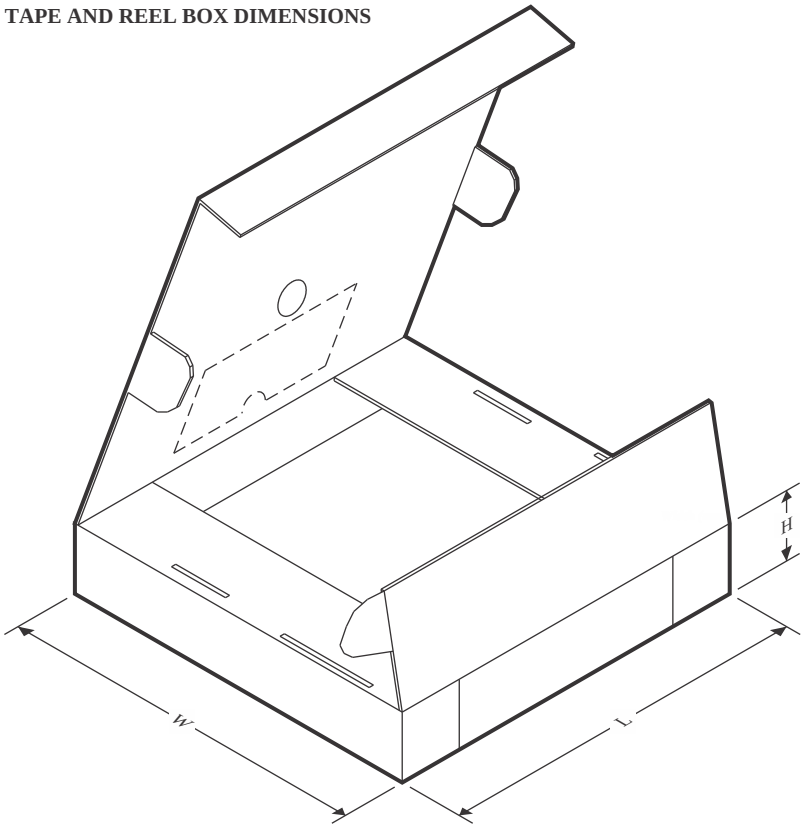
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCD7232RTJR | QFN | RTJ | 20 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| UCD7232RTJT | QFN | RTJ | 20 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| UCD7232RTJTG4 | QFN | RTJ | 20 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCD7232RTJR | QFN | RTJ | 20 | 3000 | 353.0 | 353.0 | 32.0 |
| UCD7232RTJT | QFN | RTJ | 20 | 250 | 213.0 | 191.0 | 35.0 |
| UCD7232RTJTG4 | QFN | RTJ | 20 | 250 | 213.0 | 191.0 | 35.0 |

# GENERIC PACKAGE VIEW

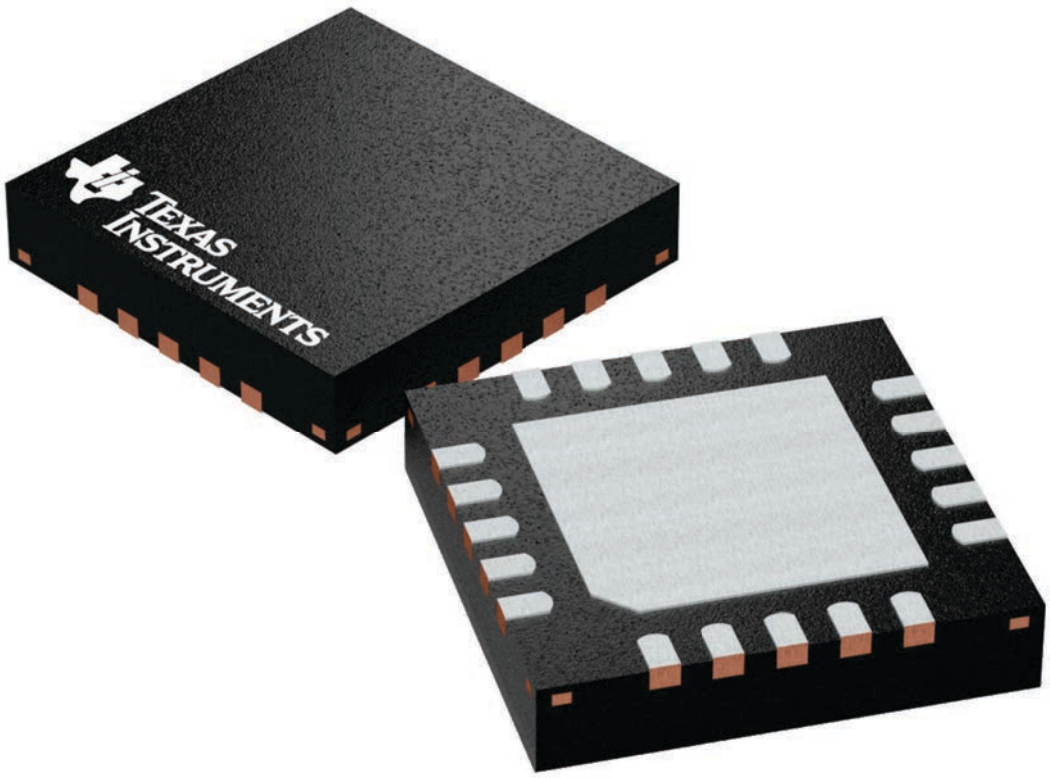
## RTJ 20

## WQFN - 0.8 mm max height

**4 x 4, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4224842/A

# DATA BOOK
# PACKAGE OUTLINE

| LEADFRAME EXAMPLE |
| --- |
| 4222370 |

| | | | |
| --- | --- | --- | --- |
| DRAFTSMAN: H. DENG | DATE: 09/12/2016 | | DIMENSIONS IN MILLIMETERS |
| DESIGNER: H. DENG | DATE: 09/12/2016 | TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS | CODE IDENTITY NUMBER 01295 |
| CHECKER: V. PAKU & T. LEQUANG | DATE: 09/12/2016 | ePOD, RTJ0020D / WQFN, 20 PIN, 0.5 MM PITCH | |
| ENGINEER: T. TANG | DATE: 09/12/2016 | | |
| APPROVED: E. REY & D. CHIN | DATE: 10/06/2016 | | |
| RELEASED: WDM | DATE: 10/24/2016 | | |
| TEMPLATE INFO: EDGE# 4218519 | DATE: 04/07/2016 | | |

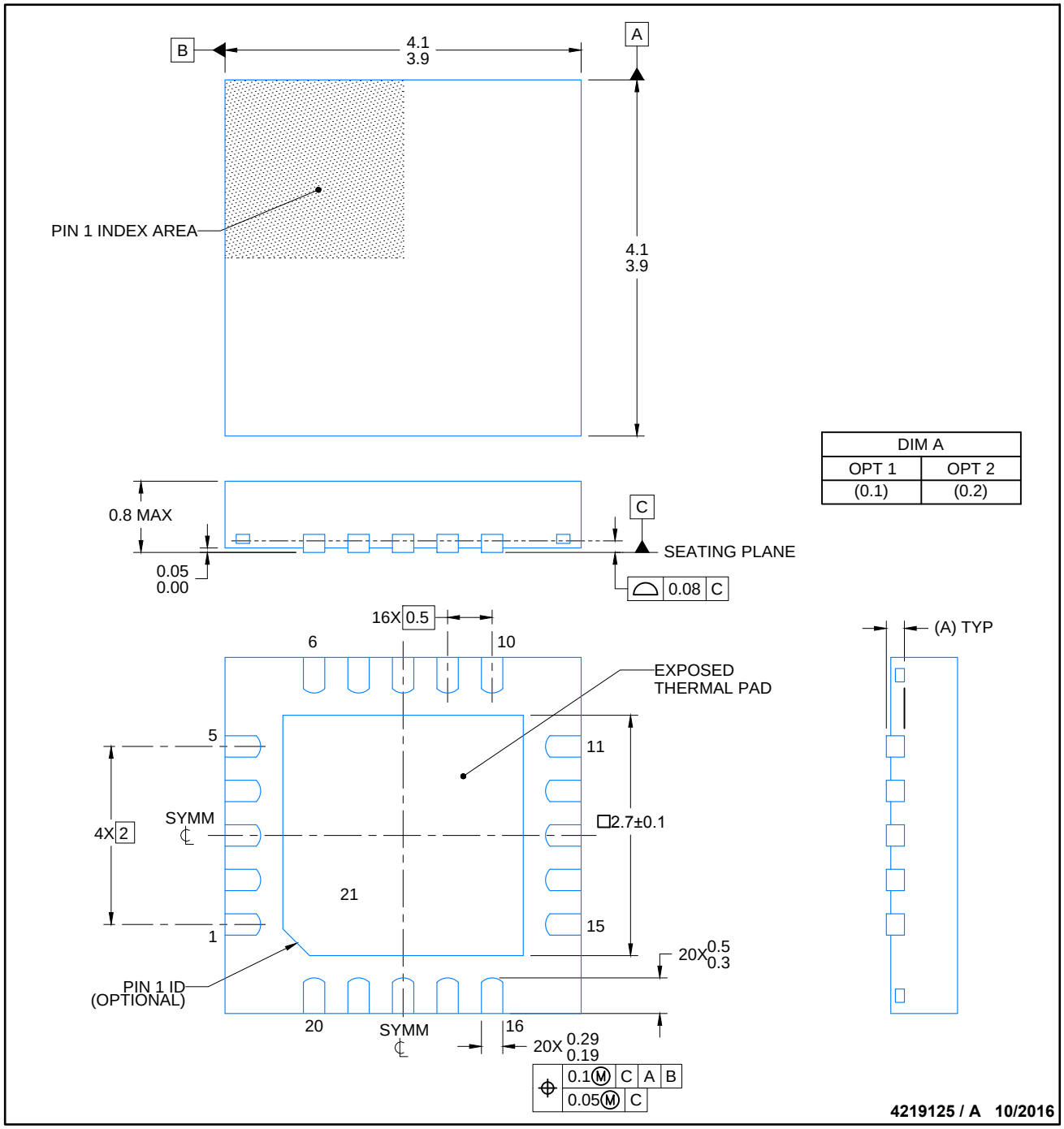
| SCALE | SIZE | | REV | PAGE |
| --- | --- | --- | --- | --- |
| 15X | A | 4219125 | A | 1 OF 5 |

# PACKAGE OUTLINE

## RTJ0020D

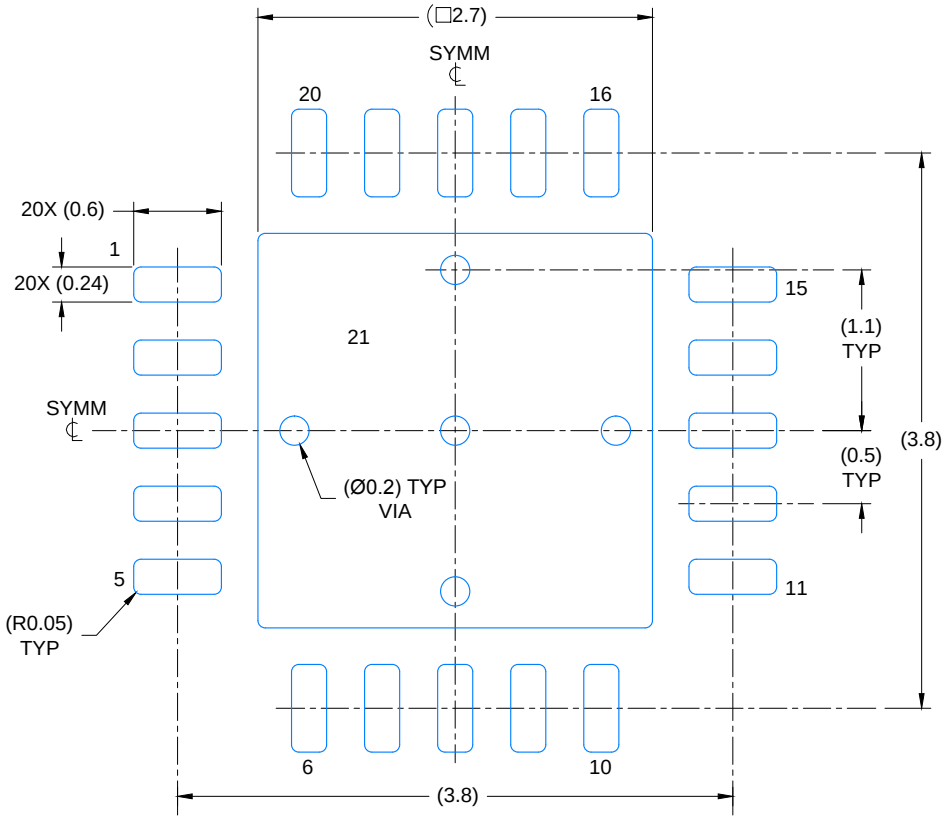
### WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



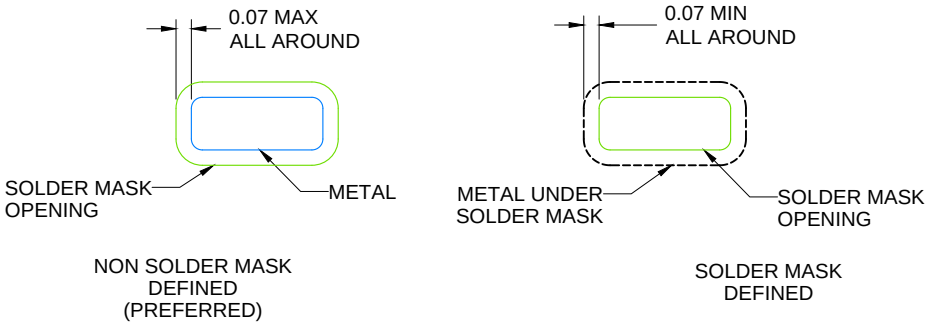

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE

SCALE: 20X




SOLDER MASK DETAILS

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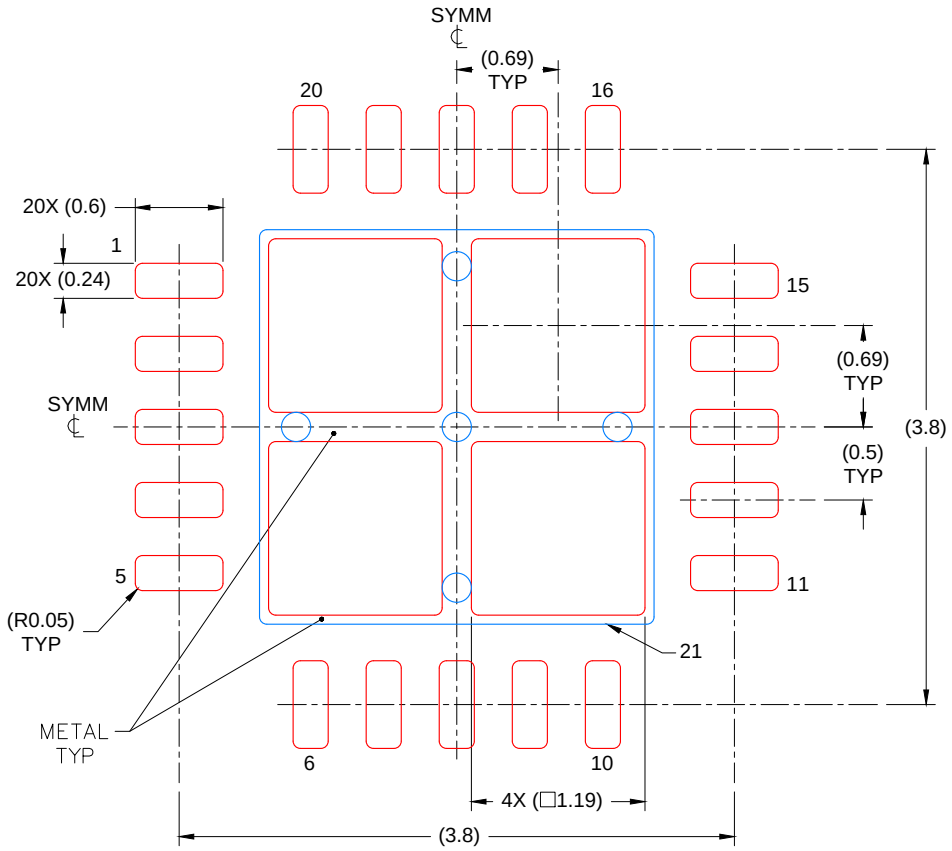
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

## REVISIONS

| REV | DESCRIPTION | ECR | DATE | ENGINEER / DRAFTSMAN |
|---|---|---|---|---|
| A | RELEASE NEW DRAWING | 2160736 | 10/24/2016 | T. TANG / H. DENG |

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