UCD91320 32-Rail PMBus™ Power Sequencer and System Manager

1 Features

- Sequence and monitor up to 24 analog or digital (power good) rails + 8 digital only rails
- PWM margining on up to 16 rails
- Cascade up to 4 devices to sequence up to 128 rails
- Active trim function allows user to trim output voltage
- Monitor and respond to OV, UV, time-out, and GPI-triggered faults
- Flexible sequencing dependencies, delay times, Boolean logic, and GPIO configurations
- Rail status dependent sequencing, delay times, and LGPO pins for complex sequencing applications
- Four rail profiles for adaptive voltage identification (AVID) voltage regulator
- Nonvolatile fault event logging with RTC and timestamping
  - Single-event fault log (100 entries)
  - Black box fault log saves fault information and status of all rails - for the first fault and the last fault before a power down event
- Continue monitoring rails during configuration activities to maximize up-time
- Programmable watchdog timer and system reset
- GPI Controlled Rail Groups
- SEU mitigation & ECC (single-error correct + double-error detect)
- PMBus™ 1.2 compliant
- PMBus security profile Level 0 with custom commands to enable features in security profile Level 2

2 Applications

- Wired networking
- Wireless infrastructure
- Datacom module
- Data center and enterprise computing
- Factory automation and control
- Test and measurement
- Medical

3 Description

The UCD91320 device is a 32-rail PMBus controlled power sequencer.

Dedicated pins (MONx) monitor up to 32 voltage rails in either analog or digital modes. 32 rail enable (ENx) pins allow regulators to be sequenced. 16 margining (MARx) pins can be used to push regulators to high or low limits (margins) for testing, or actively trim outputs for enhanced accuracy. The output state of 16 logical GPO (LGPOx) pins can be controlled by the state of GPIs, rail status, and other LGPOs.

Nonvolatile event logging preserves fault events after power dropout. The Black Box Fault Log preserves the fault information and the status of all rails. This occurs for the first fault as well as the last fault before a power down event. The cascading feature offers convenient ways to manage up to 128 voltage rails.

A user defined fault pin coordinates the cascaded devices to take synchronized fault responses.
The user can select up to 8 groups of rail configurations using 3 GPIs. These configurations can implement system low-power modes as outlined in the *Advanced Configuration and Power Interface* (ACPI) specification.

The Sequencer Studio™ software is an intuitive PC-based graphic user interface (GUI) that can configure, store, and monitor all system operating parameters.

Packaging Information Table

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
UCD91320SPZR	LQFP (100)	14.0 mm × 14.0 mm
UCD91320SZAWR	nFBGA (100)	9.0 mm × 9.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

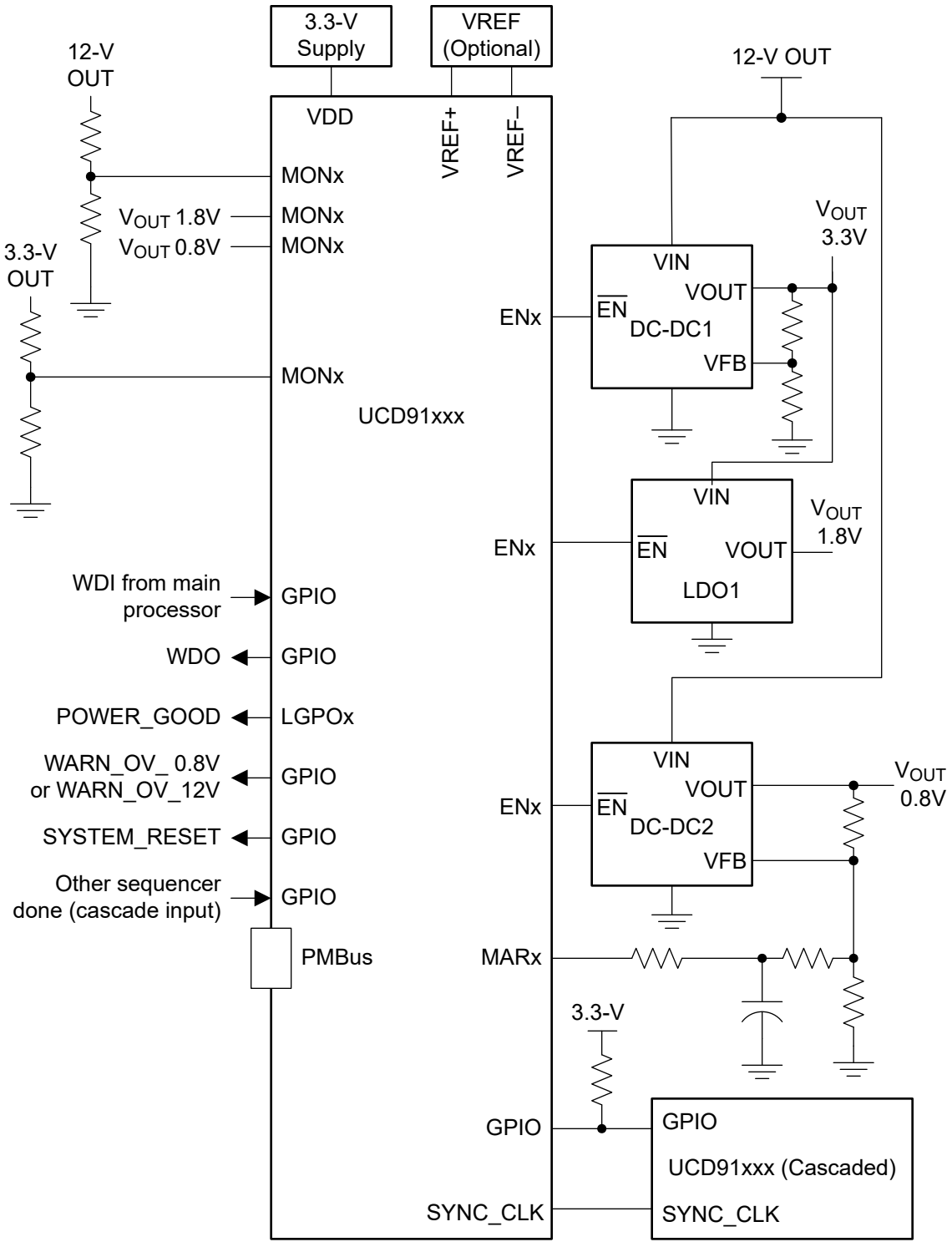

Figure 3-1. Simplified Application Diagram

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4 Pin Configuration and Functions

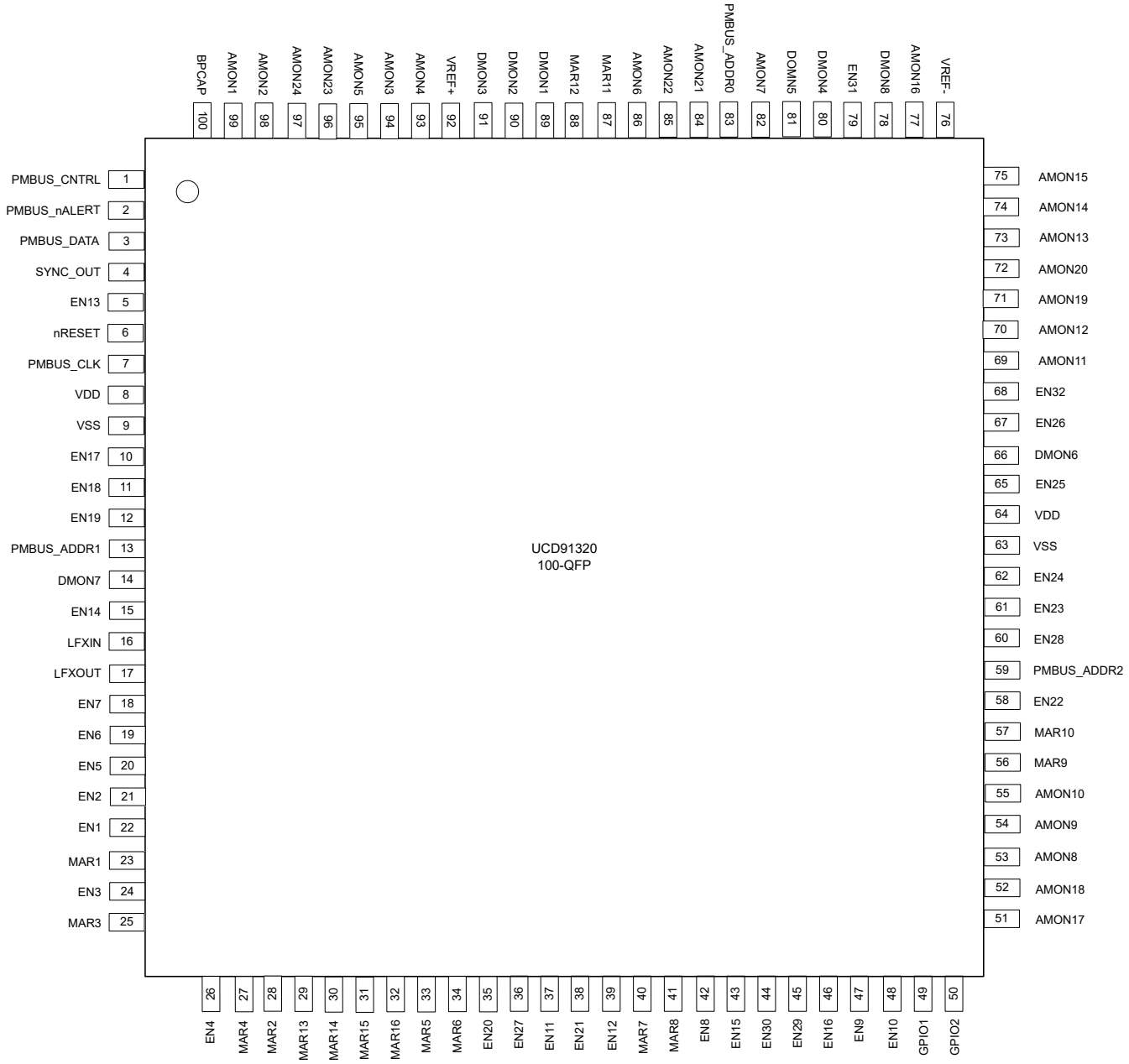


Figure 4-1. PZ Package 100-Pin LQFP Top View

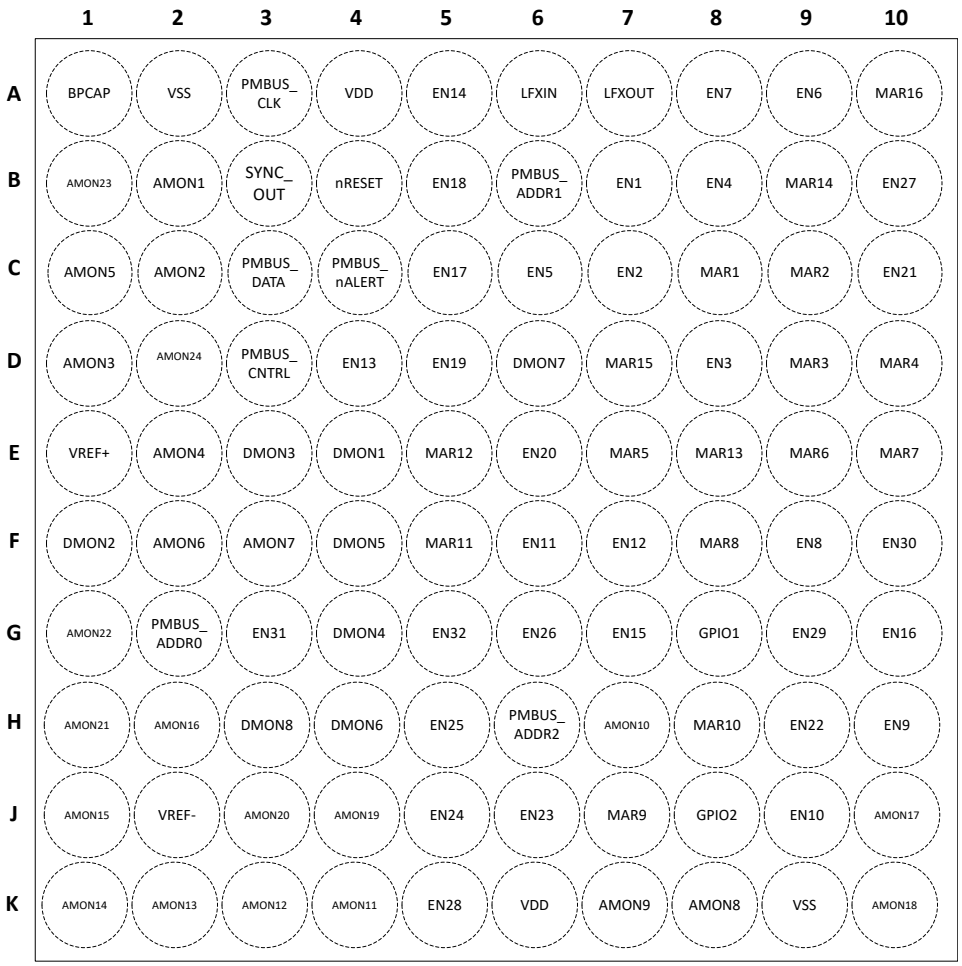


Figure 4-2. ZAW Package 100-Pin nFBGA Top View

Table 4-1. Pin Functions

PIN			TYPE		DESCRIPTION
NAME	100-QFP	100-nFBGA		Pin ID	
MONITORING INPUTS (MONx)					
MON1	99	B2	I/O	1	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON2	98	C2	I/O	2	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON3	94	D1	I/O	3	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON4	93	E2	I/O	4	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON5	95	C1	I/O	5	Analog or Digital Monitor (0V – 3.3V)
MON6	86	F2	I/O	6	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON7	82	F3	I/O	7	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON8	53	K8	I/O	8	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON9	54	K7	I/O	9	Analog Monitor (0V – 3.3V)[1]
MON10	55	H7	I/O	10	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON11	69	K4	I/O	11	Analog or Digital Monitor (0V – 3.3V), or GPIO

[1] Utilize MON9 only as an analog monitoring pin.

Table 4-1. Pin Functions (continued)

PIN			TYPE		DESCRIPTION
NAME	100-QFP	100-nFBGA		Pin ID	
MON12	70	K3	I/O	12	Analog Monitor (0V – 3.3V)[2]
MON13	73	K2	I/O	13	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON14	74	K1	I/O	14	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON15	75	J1	I/O	15	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON16	77	H2	I/O	16	Analog Monitor (0V – 3.3V)[3]
MON17	51	J10	I/O	17	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON18	52	K10	I/O	18	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON19	71	J4	I/O	19	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON20	72	J3	I/O	20	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON21	84	H1	I/O	21	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON22	85	G1	I/O	22	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON23	96	B1	I/O	23	Analog or Digital Monitor (0V – 3.3V), or GPIO
MON24	97	D2	I/O	24	Analog or Digital Monitor (0V – 3.3V), or GPIO
Digital Monitoring (DMONx)					
DMON1	89	E4	I/O	25	Digital Monitor (0V – 3.3V), or GPIO
DMON2	90	F1	I/O	26	Digital Monitor (0V – 3.3V), or GPIO
DMON3	91	E3	I/O	27	Digital Monitor (0V – 3.3V), or GPIO
DMON4	80	G4	I/O	28	Digital Monitor (0V – 3.3V), or GPIO
DMON5	81	F4	I/O	29	Digital Monitor (0V – 3.3V), or GPIO
DMON6	66	H4	I/O	30	Digital Monitor (0V – 3.3V), or GPIO
DMON7	14	D6	I/O	31	Digital Monitor (0V – 3.3V), or GPIO
DMON8	78	H3	I/O	32	Digital Monitor (0V – 3.3V), or GPIO
Rail Enables (ENx)					
EN1(GPIO)	22	B7	I/O	33	Rail enable signal, digital output, or GPIO
EN2(GPIO)	21	C7	I/O	34	Rail enable signal, digital output, or GPIO
EN3(GPIO)	24	D8	I/O	35	Rail enable signal, digital output, or GPIO
EN4(GPIO)	26	B8	I/O	36	Rail enable signal, digital output, or GPIO
EN5(GPIO)	20	C6	I/O	37	Rail enable signal, digital output, or GPIO
EN6(GPIO)	19	A9	I/O	38	Rail enable signal, digital output, or GPIO
EN7(GPIO)	18	A8	I/O	39	Rail enable signal, digital output, or GPIO
EN8(GPIO)	42	F9	I/O	40	Rail enable signal, digital output, or GPIO
EN9(GPIO)	47	H10	I/O	41	Rail enable signal, digital output, or GPIO
EN10(GPIO)	48	J9	I/O	42	Rail enable signal, digital output, or GPIO
EN11(GPIO)	37	F6	I/O	43	Rail enable signal, digital output, or GPIO
EN12(GPIO)	39	F7	I/O	44	Rail enable signal, digital output, or GPIO

[2] Utilize MON12 only as an analog monitoring pin.
[3] Utilize MON16 only as an analog monitoring pin.

Table 4-1. Pin Functions (continued)

PIN			TYPE		DESCRIPTION
NAME	100-QFP	100-nFBGA		Pin ID	
EN13(GPIO)	5	D4	I/O	45	Rail enable signal, digital output, or GPIO
EN14(GPIO)	15	A5	I/O	46	Rail enable signal, digital output, or GPIO
EN15(GPIO)	43	G7	I/O	47	Rail enable signal, digital output, or GPIO
EN16(GPIO)	46	G10	I/O	48	Rail enable signal, digital output, or GPIO
EN17(GPIO)	10	C5	I/O	49	Rail enable signal, digital output, or GPIO
EN18(GPIO)	11	B5	I/O	50	Rail enable signal, digital output, or GPIO
EN19(GPIO)	12	D5	I/O	51	Rail enable signal, digital output, or GPIO
EN20(GPIO)	35	E6	I/O	52	Rail enable signal, digital output, or GPIO
EN21(GPIO)	38	C10	I/O	53	Rail enable signal, digital output, or GPIO
EN22(GPIO)	58	H9	I/O	54	Rail enable signal, digital output, or GPIO
EN23(GPIO)	61	J6	I/O	55	Rail enable signal, digital output, or GPIO
EN24(GPIO)	62	J5	I/O	56	Rail enable signal, digital output, or GPIO
EN25(GPIO)	65	H5	I/O	57	Rail enable signal, digital output, or GPIO
EN26(GPIO)	67	G6	I/O	58	Rail enable signal, digital output, or GPIO
EN27(GPIO)	36	B10	I/O	59	Rail enable signal, digital output, or GPIO
EN28(GPIO)	60	K5	I/O	60	Rail enable signal, digital output, or GPIO
EN29(GPIO)	45	G9	I/O	61	Rail enable signal, digital output, or GPIO
EN30(GPIO)	44	F10	I/O	62	Rail enable signal, digital output, or GPIO
EN31(GPIO)	79	G3	I/O	63	Rail enable signal, digital output, or GPIO
EN32(GPIO)	68	G5	I/O	64	Rail enable signal, digital output, or GPIO
Closed-Loop Margin Pins (MARx)					
MAR1(GPIO)	23	C8	I/O	65	Closed-loop margin PWM output, or GPIO
MAR2(GPIO)	28	C9	I/O	66	Closed-loop margin PWM output, or GPIO
MAR3(GPIO)	25	D9	I/O	67	Closed-loop margin PWM output, or GPIO
MAR4(GPIO)	27	D10	I/O	68	Closed-loop margin PWM output, or GPIO
MAR5(GPIO)	33	E7	I/O	69	Closed-loop margin PWM output, or GPIO
MAR6(GPIO)	34	E9	I/O	70	Closed-loop margin PWM output, or GPIO
MAR7(GPIO)	40	E10	I/O	71	Closed-loop margin PWM output, or GPIO
MAR8(GPIO)	41	F8	I/O	72	Closed-loop margin PWM output, or GPIO
MAR9(GPIO)	56	J7	I/O	73	Closed-loop margin PWM output, or GPIO
MAR10(GPIO)	57	H8	I/O	74	Closed-loop margin PWM output, or GPIO
MAR11(GPIO)	87	F5	I/O	75	Closed-loop margin PWM output, or GPIO
MAR12(GPIO)	88	E5	I/O	76	Closed-loop margin PWM output, or GPIO
MAR13(GPIO)	29	E8	I/O	77	Closed-loop margin PWM output, or GPIO
MAR14(GPIO)	30	B9	I/O	78	Closed-loop margin PWM output, or GPIO
MAR15(GPIO)	31	D7	I/O	79	Closed-loop margin PWM output, or GPIO
MAR16(GPIO)	32	A10	I/O	80	Closed-loop margin PWM output, or GPIO

Table 4-1. Pin Functions (continued)

PIN			TYPE		DESCRIPTION
NAME	100-QFP	100-nFBGA		Pin ID	
General Purpose Inputs and Outputs (GPIOx)					
GPIO1	49	G8	I/O	81	Boolean-Logical Output, or GPIO
GPIO2	50	J8	I/O	82	Boolean-Logical Output, or GPIO
PMBus COMM INTERFACE					
PMBUS_CLK	7	A3	I/O	N/A	PMBus clock (must have pullup to 3.3V)
PMBUS_DATA	3	C3	I/O	N/A	PMBus data (must have pullup to 3.3V)
PMBUS_nALERT	2	C4	O	N/A	PMBus alert, active-low, open-drain output (must have pullup to 3.3V)
PMBUS_CNTRL	1	D3	I	N/A	PMBus control (must have pullup to 3.3V)
PMBUS_ADDR0	83	G2	I	N/A	PMBUS Address Select
PMBUS_ADDR1	13	B6	I	N/A	PMBUS Address Select
PMBUS_ADDR2	59	H6	I	N/A	PMBUS Address Select
INPUT POWER, GROUNDS, AND CLOCKING					
LFXOUT	17	A7	CLK	N/A	Low-frequency crystal out
LFXIN	16	A6	CLK	N/A	Low-frequency crystal in
nRESET	6	B4	I	N/A	Active-low device reset input. Recommend pulling up to VDD if not required by application. Hold low for at least 1.5µs to perform a boot reset, or 1s for a power-on-reset (POR)
SYNC_OUT	4	B3	O	N/A	Synchronization clock I/O (5kHz) for multiple chip cascading
VREF+	92	E1	I	N/A	(Optional) positive node of external reference voltage
VREF-	76	J2	P	N/A	(Optional) negative node of external reference voltage[4]
VDD	8,64	A4, K6	P	N/A	Input 3V to 3.6V supply. Refer to the Layout Guidelines section
VSS	9,63	A2, K9	P	N/A	Device ground
BPCAP	100	A1	P	N/A	0.47µF bypass capacitor. Refer to the Layout Guidelines section

[4] When the VREF- pin is not utilized, connect it to ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin	–0.3	4.1	V
V_I	Input voltage	Applied to any 5V tolerant open-drain pins	–0.3	5.5	V
V_I	Input voltage	Applied to any common tolerance pins	–0.3	V_{DD} + 0.3 (4.1 MAX)	V
I_{VDD}	Current into VDD pin (source)	-40°C ≤ Tj ≤ 130°C		80	mA
	Current into VDD pin (source)	-40°C ≤ Tj ≤ 85°C		100	mA
I_{VSS}	Current out of VSS pin (sink)	-40°C ≤ Tj ≤ 130°C		80	mA
	Current out of VSS pin (sink)	-40°C ≤ Tj ≤ 85°C		100	mA
I_{IO}	Current of device pin	Current sunk or sourced by device pin		6	mA
I_D	Supported diode current	Diode current at any device pin except VREF-		±2(3)	mA
T_J	Junction temperature	Junction temperature	-40	130	°C
T_{stg}	Storage temperature(2)	Storage temperature(2)	–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Apply higher temperatures during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
(3) VREF- has an internal connection for testing purposes, there is no injection current allowed on this pin.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	2.9		3.6	V
C_{VDD}	Capacitor connected between VDD and VSS (1)		10		uF
C_{BPCAP}	Capacitor connected between BPCAP and VSS (1) (2)		470		nF
T_A	Ambient temperature, S version	–40		125	°C
T_J	Max junction temperature, T version			125	°C

(1) Connect C_{VDD} and C_{BPCAP} between VDD/VSS and BPCAP/VSS, respectively, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD} and C_{BPCAP}.
(2) The BPCAP pin must only be connected to C_{BPCAP}. Do not supply any voltage or apply any external load to the BPCAP pin.

5.4 Thermal Information

THERMAL METRIC(1)		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-100 (PZ)	72.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		21.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		54.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		53.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	nfBGA-100 (ZAW)	53.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		21.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		32.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		32.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Vin_{(ADC)}$	Analog input voltage range(1)	Applies to all ADC analog input pins	0		VDD	V
V_{R+}	Positive ADC reference voltage	V_{R+} sourced from VDD		VDD		V
T_s	ADC sample time per channel			250		ns
F_S	ADC sampling frequency (per channel)			10		ksps
$I_{(ADC)}$	Operating supply current into VDD terminal	V_{R+} = VDD		1.5(2)		mA
$C_{S/H}$	ADC sample-and-hold capacitance			3.3		pF
Rin	ADC input resistance			0.5		kΩ
ENOB	Effective number of bits	External reference	12.3	12.5		bit
		Internal reference, V_{R+} = 2.5V	9.9	10.8		
SNR	Signal-to-noise ratio	External reference (3)		78		dB
		Internal reference, V_{R+} = 2.5V		66		
$PSRR_{DC}$	Power supply rejection ratio, DC	External reference (3), VDD = $VDD_{(min)}$ to $VDD_{(max)}$		62		dB
		VDD = $VDD_{(min)}$ to $VDD_{(max)}$ Internal reference, V_{R+} = 2.5V		53		
$PSRR_{AC}$	Power supply rejection ratio, AC	External reference (3), ΔVDD = 0.1V at 1kHz		61		dB
		ΔVDD = 0.1V at 1kHz Internal reference, V_{R+} = 2.5V		52		

(1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) The internal reference (VREF) supply current is not included in current consumption parameter $I_{(ADC)}$.
(3) All external reference specifications are measured with V_{R+} = VREF+ = VDD = 3.3V and V_{R-} = VREF- = VSS = 0V and external 1uF cap on VREF+ pin

5.6 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
EI	Integral linearity error (INL)	External reference (2)	External reference (2)	-2		2	LSB
E_D	Differential linearity error (DNL) Ensured no missing codes	External reference (2)	External reference (2)	-1		1	LSB
E_O	Offset error	Internal or External reference (2)		-2		2	mV
E_G	Gain error	External reference (2)		-3		3	LSB

(1) Total Unadjusted Error (TUE) can be calculated from E_I , E_O , and E_G using the following formula: TUE = $\sqrt{(E_I^2 + |E_O|^2 + E_G^2)}$
Note: Convert all of the errors into the same unit, usually LSB, for the above equation to be accurate
(2) All external reference specifications are measured with V_{R+} = VREF+ = VDD and V_{R-} = VSS = 0V, external 1uF cap on VREF+ pin.

5.7 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
		Falling (2)			0.01	
		Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising (1)	1.04	1.30	1.5	V
V_{POR-}		Falling (1)	0.99	1.25	1.48	V
$V_{HYS, POR}$	POR hysteresis		30	58	74	mV
V_{BOR+}	Brown-out-reset voltage	Rising (1) (2)	2.88	2.96	3.04	V
V_{BOR-}		Falling (1) (2)	2.85	2.93	3.01	
$V_{BOR, STBY}$		STANDBY mode (1)	2.80	2.92	3.02	
$V_{HYS,BOR}$	Brown-out reset hysteresis	Level 0 (1)		14	18	mV
		Levels 1-3 (1)		34	38	

(1) |dVDD/dt| ≤ 3V/s
(2) Device operating in RUN, SLEEP, or STOP mode.

5.8 Low Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency crystal oscillator (LFXT)						
f_{LFXT}	LFXT frequency			32768		Hz
DC_{LFXT}	LFXT duty cycle		30		70	%
OA_{LFXT}	LFXT crystal oscillation allowance			419		kΩ
$C_{L, eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start, LFXT}$	LFXT start-up time			483	640	ms

(1) The integrated effective load capacitance includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{LFXIN} \times C_{LFXOUT}/(C_{LFXIN}+C_{LFXOUT})$, where C_{LFXIN} and C_{LFXOUT} are the total capacitance at LFXIN and LFXOUT, respectively.

5.9 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta			10	mA

5.9 Flash Memory Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta			10	mA
Endurance						
NWEC	Erase/program cycle endurance		10			k cycles
$NE_{(MAX)}$	Total erase operations before failure (1)		802			k erase operations
Retention						
t_{RET_85}	Flash memory data retention	-40°C <= Tj <= 85°C	60			years
t_{RET_105}	Flash memory data retention	-40°C <= Tj <= 105°C	11.4			years
t_{RET_130}	Flash memory data retention	-40°C <= Tj <= 130°C	2.4			years
Fault and Event Logging						
NF	Total number of fault event records before failure		64			Million event logs

(1) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.

6 Detailed Description

6.1 Overview

Electronic systems such as CPUs, DSPs, microcontrollers, FPGAs, and ASICs can have multiple voltage rails, and require precise power-ON and power-OFF sequences in order to function correctly. The UCD91320 can sequence up to 32 voltage rails, monitor voltages and fault conditions, and report system health information through a PMBus interface.

The UCD91320 protects electronic systems by enacting pre-configured responses to power system faults. A fault immediately triggers the Black Box Fault Log to store a comprehensive system status report, but subsequent fault logs are stored inside nonvolatile memory.

System reliability can be validated through four-corner testing. A voltage rail can be commanded to operate at the minimum and maximum output voltages – this is known as margining. The device can perform accurate closed-loop margining on up to 16 voltage rails. During normal operation, UCD91320 can actively trim DC output voltages using the same margining circuitry on those 16 pins.

The UCD91320 contains a pool of 32 GPIO pins. Many of these pins have primary functionality as ENx, MARx, or LGPOx pins, but they can also be configured as general purpose I/Os (GPIO) to allow the device to interact with external circuitry. The pin description table shows the primary functionality of each pin. GPIO states can be controlled in several ways:

- Command-controlled GPO – These outputs can be set by PMBus commands
- GPIOs – These pins can be used to generate faults, enable/disable margining, or influence the state of other GPIOs
- Boolean-logic controlled (LGPO) – The UCD91320 allows any GPIO to be configured as an LPGO (Up to 16 LGPOs are supported). The states of these pins are dependent on the states of items such as rail status, or fault events.

The device provides additional features such as cascading, pin-selected states, system watchdog, system reset, run time clock, reset counter, and so forth. Cascading feature offers convenient ways to cascade up to four UCD91320 devices and manage up to 128 voltage rails. Pin-selected states feature allows users to define up to 8 rail states. These states can implement system low-power modes as set out in the *Advanced Configuration and Power Interface (ACPI)* specification.

6.2 Feature Description

6.2.1 TI Sequencer Studio Software

The PC-based Texas Instruments Sequencer Studio software communicates with the device via a PMBus interface, and enables the design engineer to configure the operating parameters for the application. This is done without having to learn low level PMBus commands. The software saves the configuration to on-chip nonvolatile memory, and can be used to observe system status during debug efforts. After configuration, the device will perform independently on startup. Download the *Sequencer Studio* software from the UCD91320 web page.

6.2.2 PMBUS Interface

PMBus is a serial interface designed to support power management applications The PMBus interface is based on the SMBus interface that is built on the I^2C physical specification. The UCD91320 device supports PMBus 1.3. Standard PMBus interface commands support the function of the device, and unique features are configurable through MFR_SPECIFIC commands. These commands are defined in the *UCD91320 Sequencer and System Health Controller PMBUS Command Reference*. The most current UCD91320 PMBus Command Reference can be found within the Sequencer Studio software through the Help Menu *(Help, Documentation & Help Center, Sequencers tab, Documentation* section).

This data sheet makes frequent mention of the PMBus specification. Specifically, this document is *PMBus Power System Management Protocol Specification Part II – Command Language*, Revision 1.2, dated 6 September 2010. The specification is published by the Power Management Bus Implementers Forum and is available from www.pmbus.org.

The UCD91320 device meets all of the requirements of the *Compliance* section of the PMBus specification. The firmware complies with the SMBus 1.2 specification, including support for the SMBus ALERT function. The hardware supports either 100-kHz or 400-kHz PMBus operation.

6.2.3 PMBUS Security

The UCD91320 device line maintains PMBus security level 0, with support for custom commands enabling features up to PMBus security level 2.

To comply with PMBus security level 0, the UCD91320 device maintains support for the following features:

1. **PASSKEY** command
2. **ACCESS_CONTROL** command

6.3 Device Functional Modes

6.3.1 Black Box Fault Logging

The first fault in a system failure event may be critical to diagnose the root cause. When UCD91320 detects an initial fault, the device records and saves the status of each rail in a special area (Black Box) of the NVM reserved for this function. The device does not save the subsequent faults and monitoring statuses into the Black Box Fault Log, but instead records them into the standard fault log. The last fault log when the BOR voltage is crossed is also saved to the black box fault log. The Black Box Fault Log must be cleared via a PMBus command before another black box fault log can be collected.

6.3.2 PMBus Address Selection

Three digital inputs are used to select the PMBus address. These pins should be set either high or low.

Table 6-1. PMBus Address Configuration

PMBUS_ADDR2	PMBUS_ADDR1	PMBUS_ADDR0	PMBUS ADDRESS SELECTED	
L	L	L	17d	0010001b
L	L	H	19d	0010011b
L	H	L	23d	0010111b
L	H	H	49d	0110001b
H	L	L	51d	0110011b
H	L	H	113d	1110001b
H	H	L	115d	1110011b
H	H	H	119d	1110111b

6.3.3 Brownout

The UCD91320 device triggers brownout event when the VDD pin voltage drops below the brownout threshold voltage (V_{BOR}). During a brownout event, the device continues to write fault logs into the NVM that occurred before the brownout event. The device fully shuts down when the VDD pin voltage is below the shutdown threshold voltage (V_{SHDN}). Any fault event that has not been written into the NVM before the device shutdown is lost.

If several faults happen immediately before the brownout event, the device requires a capacitance of 500 µs to write the first fault event into the NVM. The write function requires an additional 4 ms to write the Black Box fault log into the NVM. The user must provide enough local capacitance to maintain the VDD rail above VSHDN for 500 µs (or 4.5 ms with the Black Box fault log) to preserve the first fault log. More capacitance allows more fault events to be written into the NVM during brownout.

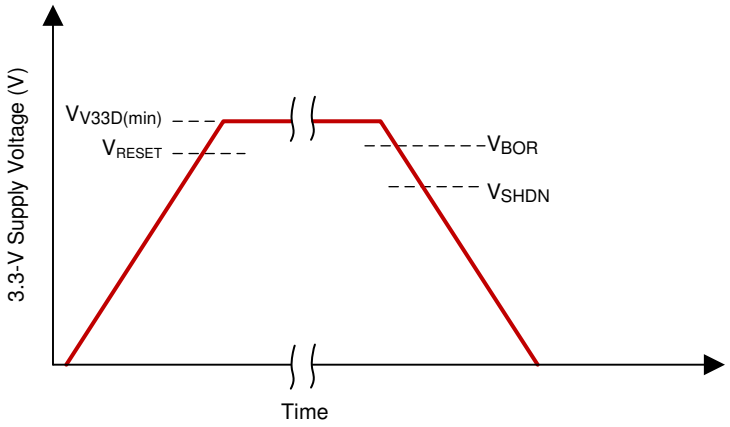


Figure 6-1. Reset and Brownout Thresholds

Failure Analysis and Returns

The UCD91xxx devices utilize multiple security safeguards to maintain integrity of the device firmware and configuration. Because of this, TI may not be able to read out the device configuration and firmware during failure analysis or in the case of a return. Please keep record of the firmware version running on your device, as well as the configuration parameters in the device. This ensures that the TI team is able to replicate any conditions for a return.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The UCD91320 device can be used to sequence and monitor up to 32 voltage rails, and margin up to 16 voltage rails. Up to four UCD91320 devices can be cascaded to allow the user to monitor up to 128 rails, and record synchronized fault responses. Typical applications include automatic test equipment, telecommunication and networking equipment, servers, and storage systems. Device configuration can be performed using the *Sequencer Studio* software provided by TI. No coding skill is required.

7.2 Typical Application

Figure 7-1 shows a simplified system diagram. For simplification, this diagram shows only three rails, but each UCD91320 device can manage up to 32 rails.

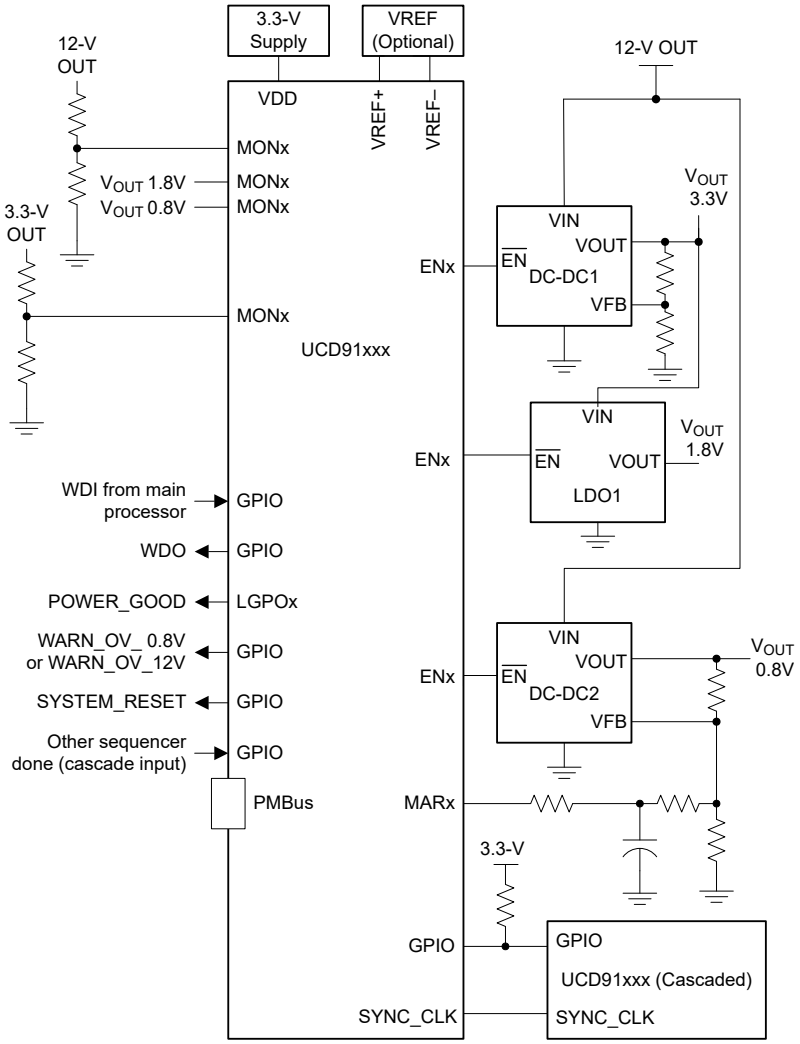


Figure 7-1. Simplified System Diagram

7.2.1 Design Requirements

UCD91320 requires decoupling capacitors on the VDD, BPCAP, and VREF+ pins. The capacitance values for VDD, BPCAP, and VREF+ are specified in the Electrical Characteristics. Consider these capacitor design configurations as options.

- If an application does not use the nRESET signal, the nRESET pin must be tied to VDD, either by direct connection to the VDD pin, or by an R-C circuit as shown in Figure 7-2. The R-C circuit in Figure 7-2 can be also used to delay reset at power up. If an application uses the nRESET external pin, the trace of the nRESET signal must be kept as short as possible. Be sure to place any components connected to the nRESET signal as close to the device as possible.
- Holding the nRESET pin low for <1s triggers a BOOT Reset, and holding nRESET low for >1s triggers a POR/Power On Reset.
- The analog monitoring pins are capable of monitoring voltage rails between 0V and 3.3V. Ensure the input of the MONx pin does not move outside of this range.
- It is mandatory that the VDD power be stable and no device reset be fired during the device programming. Resets triggered while the device is programming can cause corruption.
- TI recommends connecting a combination of a 10-µF and a 0.1-µF low-ESR ceramic decoupling capacitor across the VDD and VSS pins, as well as placing these capacitors as close as possible to the supply pins that they decouple (within a few millimeters) to achieve a minimal loop area. The 10-µF bulk decoupling capacitor is a recommended value for most applications, but this capacitance can be adjusted if needed based upon the PCB design and application requirements. For example, larger bulk capacitors can be used, but this can affect the supply rail ramp-up time.
- A 0.47-µF tank capacitor is required for the BPCAP pin and must be placed close to the device with minimum distance to the device ground. Do not connect other circuits to the BPCAP pin.

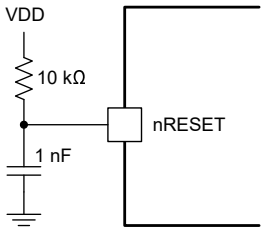


Figure 7-2. nRESET Pin With R-C Network

7.2.2 Detailed Design Procedure

The *Sequencer Studio* software can be used to design the device configuration online or offline (with or without a UCD91320 device connected to the computer). In offline mode, the software prompts the user to create or open a project file (.xml) at launch. In online mode, the software automatically detects the device via the PMBus interface and extracts the configuration data from the device. A USB Interface Adapter EVM available from TI is required to connect *Sequencer Studio* software to PMBus.

The general design steps are included. Details of the steps are described in the *Section 6*, and are easily accessed within the *Sequencer Studio* software.

1. Rail setup
2. Rail monitoring configuration
3. GPI configuration
4. Rail sequence configuration
5. Fault response configuration
6. GPO configuration
7. Margining configuration
8. Other configurations including but not limited to:
   - Pin Selected Rail States
   - Watchdog Timer

- System Reset
- Sync Clock
- Fault Pins

Click **Write to Hardware** to apply the changes. In online mode, then click **Store RAM to Flash** to permanently store the new configuration into the data flash of the device.

7.2.3 Application Curves

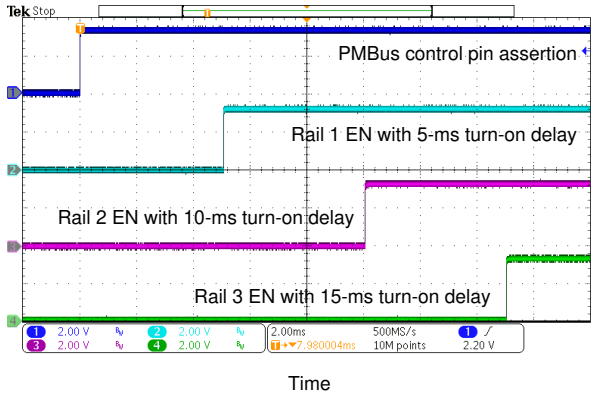


Figure 7-3. Start-Up Waveforms

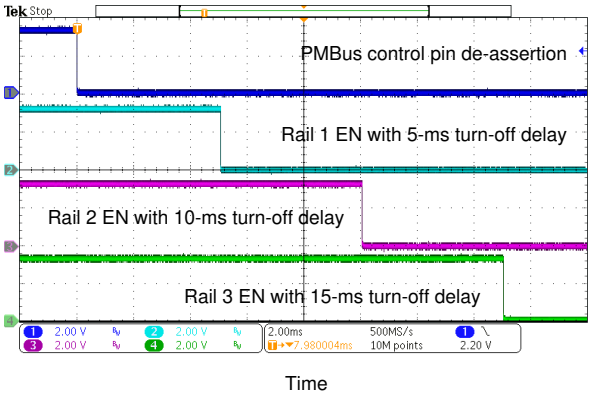


Figure 7-4. Shut-Down Waveforms

7.3 Power Supply Recommendations

Power the UCD91320 device from a 3.3V power supply.

If internal reference is used, VDD acts as ADC reference and is assumed to be exactly 3.3V. Any input voltage deviation from 3.3V introduces an error to ADC reference and to the ADC results. Therefore, the 3.3V power supply must be tightly regulated and allow only a very small voltage fluctuation (including voltage ripple and voltage deviation caused by load transients).

If external reference (VREF+) is used, the 3.3V power supply needs to meet only the minimum requirements specified in the Section 5.3 and Section 5.5.

7.4 Layout

7.4.1 Layout Guidelines

- Place the decoupling capacitors as close as possible to the device
- Connect the BPCAP decoupling capacitors as close as possible to the BPCAP pin
- Margin pins (MARx) output PWM signals that have fast edges. Route these signals away from sensitive analog signals

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

PMBus™ is a trademark of SMIF, Inc..
Sequencer Studio™ is a trademark of TI.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCD91320SPZR	Active	Production	LQFP (PZ) | 100	1000 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD91320S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

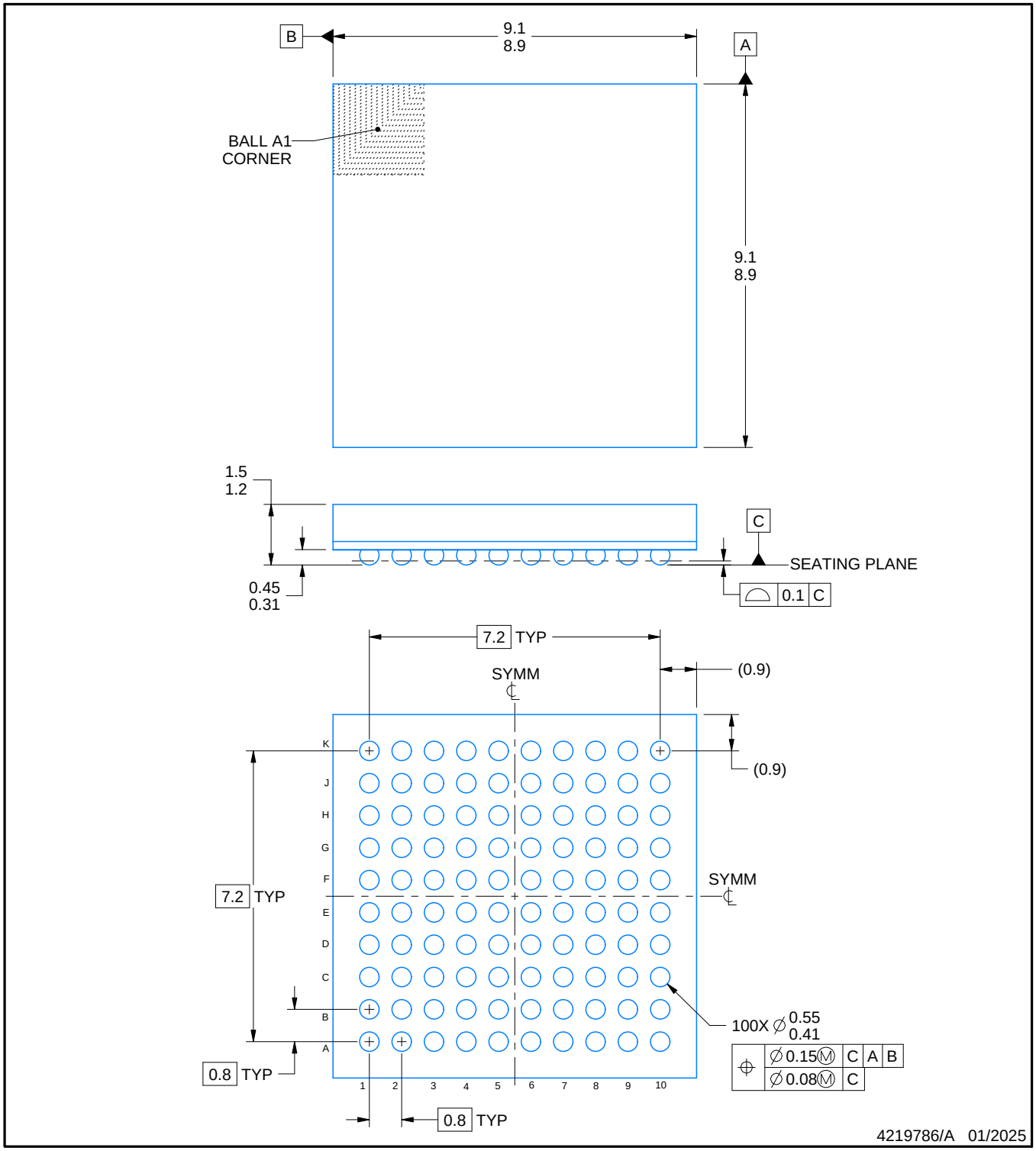
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

ZAW0100A

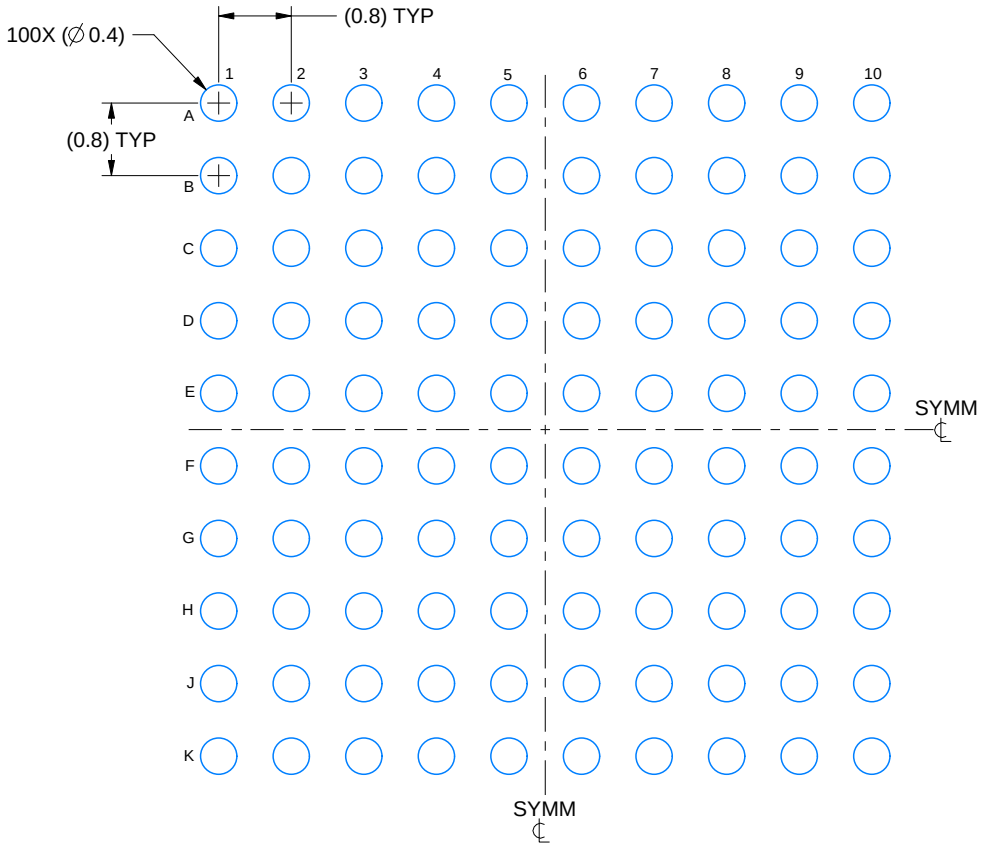
NFBGA - 1.5 mm max height

PLASTIC BALL GRID ARRAY

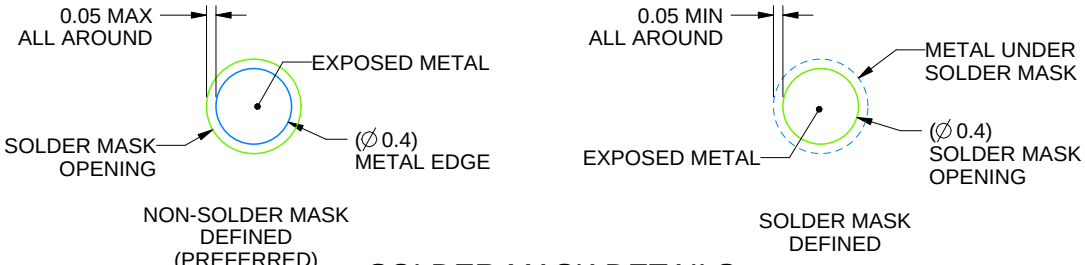


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

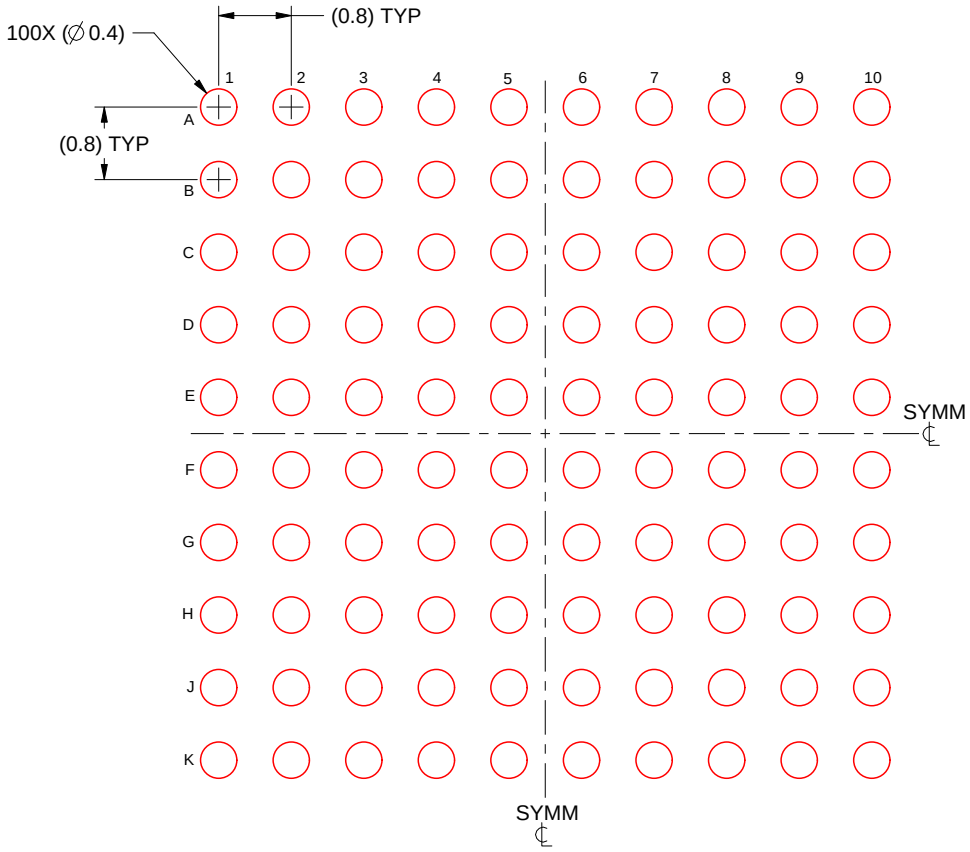


SOLDER MASK DETAILS
NOT TO SCALE

4219786/A 01/2025

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

4219786/A 01/2025

NOTES: (continued)

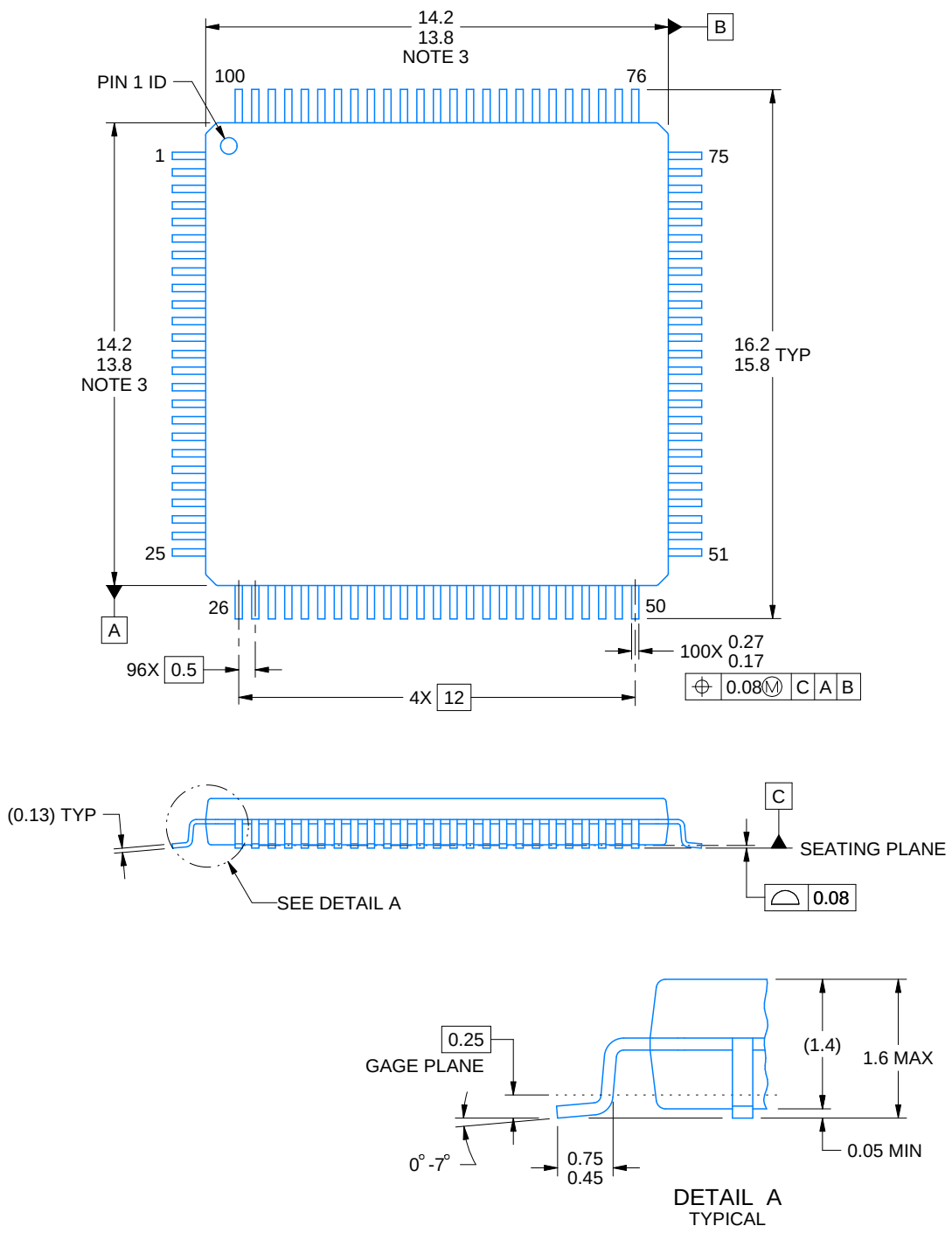
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

PZ0100A

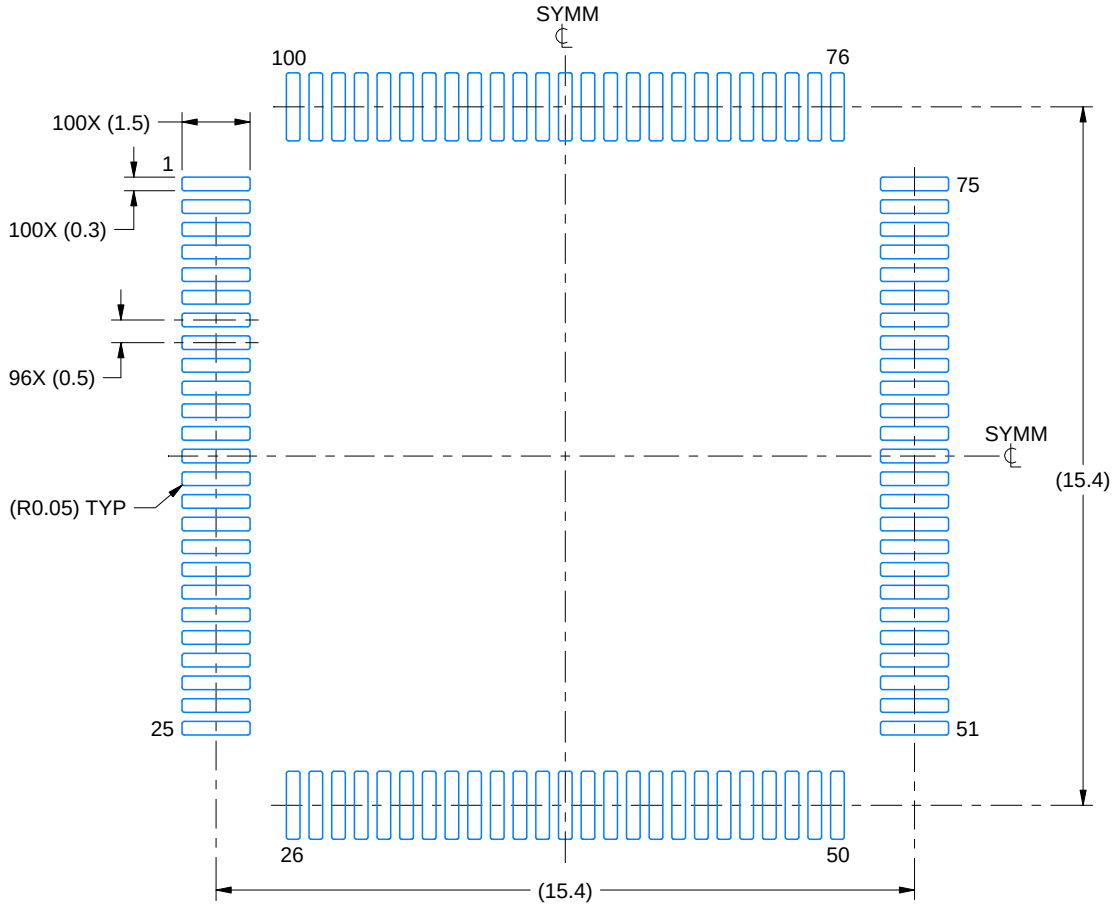
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

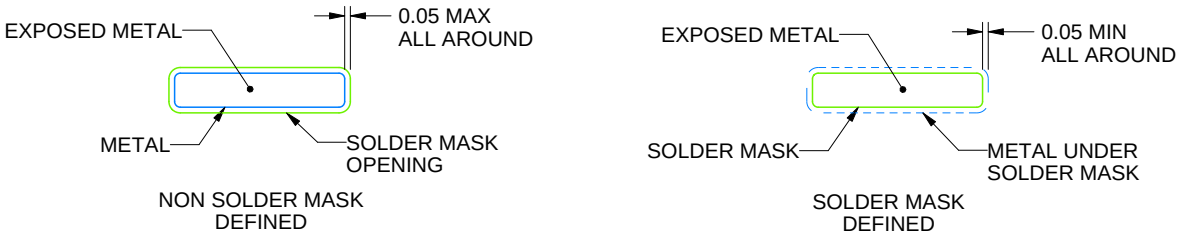


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

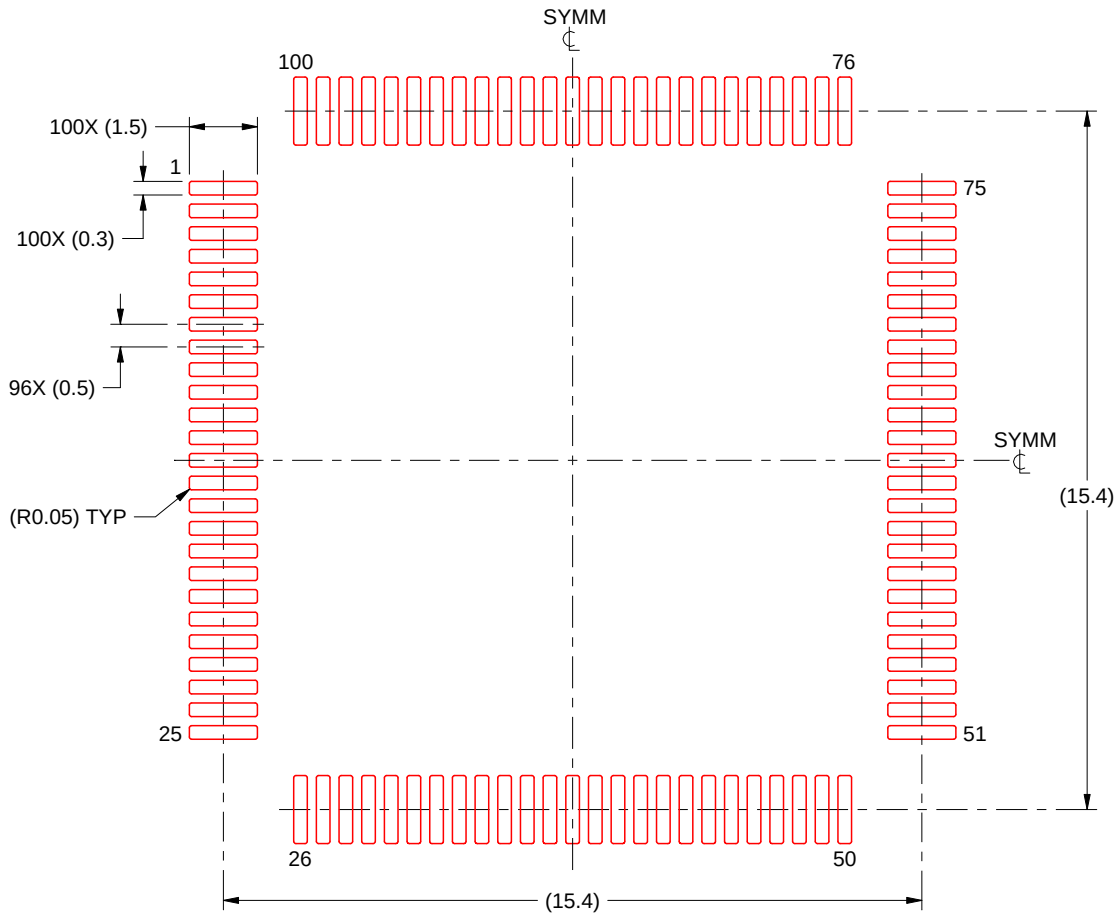


SOLDER MASK DETAILS

4215169/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215169/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025