Errata

DLP® Products Advisory for the DLPR410 and DLPR910 Devices

ABSTRACT

AMD Xilinx stopped production of the XCF16P Configuration PROMs used as the base device for the following TI devices: 2510442-0005, DLPR410YVA, DLPR410AYVA, DLPR410BYVA, DLPR910YVA, DLPR910AYVA. This document details the Texas Instruments product design updates and support.

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1 Affected Products

AMD Xilinx has stopped production of the XCF16P configuration PROMs used as the base device for the following TI devices:

- 2510442-0005
- DLPR410YVA
- DLPR410AYVA
- DLPR410BYVA
- DLPR910YVA
- DLPR910AYVA

2 Master Serial Peripheral Interface Flash Configuration Method

Product designs that use the DLPC910 or DLPC410 Controller will need to be updated to implement Xilinx Master Serial Peripheral Interface (SPI) Flash configuration method.

3 SPI Flash Configuration Method

See the following AMD Xilinx information on how to connect a DLPC910 and DLPC410 (Virtex-5 FPGA) to SPI flash for configurations.

3.1 Configuration Guide

Xilinx Virtex-5 Configuration Guide:

https://docs.xilinx.com/v/u/en-US/ug191

3.2 FPGA Pinout Information

Xilinx Virtex-5 XC5VLX30FF676 FPGA Pinout Information:

http://www.xilinx.com/content/dam/xilinx/support/packagefiles/v5packages/5vlx30ff676.pkg.txt

3.3 Design Details Supporting SPI Flash Configuration Method

Design details to support the Master Serial Peripheral Interface (SPI) Flash configuration with the DLPC910 and DLPC410 are as follows:

1. Master Serial Peripheral Interface Flash configuration mode M[2..0] pins on FPGA controllers must be changed to M[2:0] = 001.

   Please see page 62 of the Xilinx Virtex-5 Configuration guide UG191 for more information:
2. FS[2:0] pins must be connected correctly to determine the type of read commands used by the SPI Flash chosen to connect to the FPGA controller. The table below (Table 2-8 in UG191 – Xilinx Virtex-5 Configuration Guide) describes the available selections:

Table 2-8: **Virtex-5 Device SPI Read Command Variant Select Table**

FS[2:0]	SPI Read Command	Comments
000	0xFF	
001	RCMD[7:0]	RCMD[7:0] on ADDR[7:0] are sampled by the INIT_B rising edge, along with M[2:0] and FS[2:0]. RCMD[7:0] can be used to support any SPI read commands not supported here. The timing requirements for FS[2:0] and RCMD[7:0] are the same as for M[2:0].
010	0x52	
011	Reserved	
100	0x55	
101	0x03	
110	0xE8	
111	0x0B	

FS2 = pin AB11 of DLPC910 Controller and DLPC410 Controller

FS1 = pin AA13 of DLPC910 Controller and DLPC410 Controller

FS0 = pin AA14 of DLPC910 Controller and DLPC410 Controller

3.4 SPI Flash Layout Connections

The DLPC910 and DLPC410 Controllers must be connected to SPI Flash using the connections described in the diagram below

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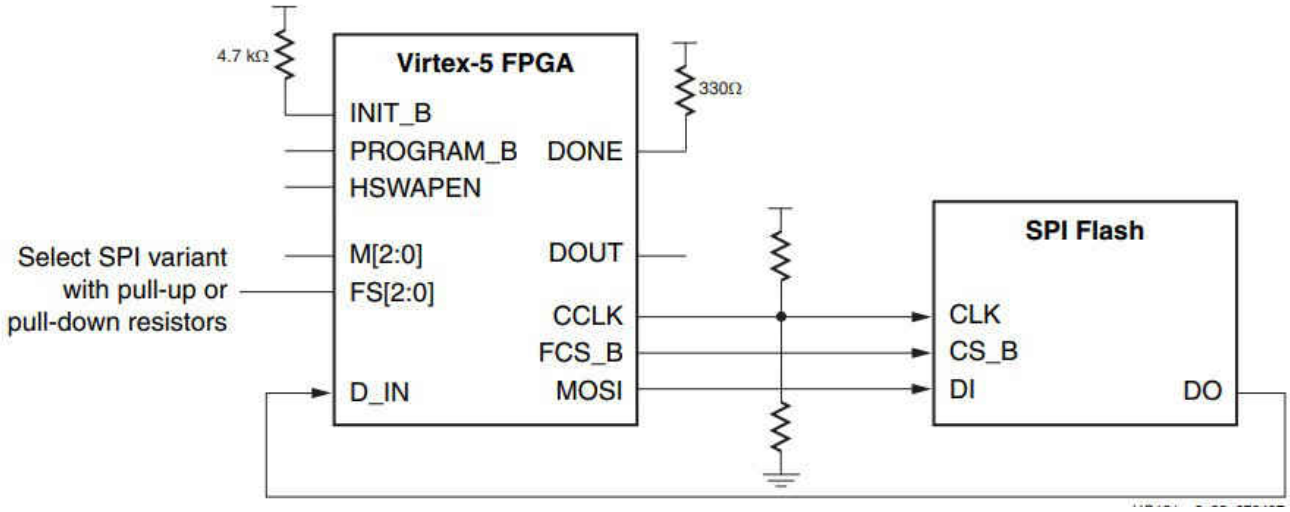
SPI Flash Write Protect (WP#) should be pulled high to allow for programming through the Virtex 5 JTAG interface. SPI Flash Reset (RESET#) or Hold (HOLD#) should be pulled high to prevent the SPI Flash from pausing serial communications with the DLPC410 and DLPC910 controllers.

For additional details on how the SPI Configuration Flash is connected to the DLPC410 Controller and DLPC910 Controller, please refer to the schematics for the DLPLCRC910EVM and DLPLCRC410EVM.



FCS_B = pin AA10 of DLPC910 Controller and DLPC410 Controller

MOSI = pin AA9 of DLPC910 Controller and DLPC410 Controller

CCLK = pin J10 of DLPC910 Controller and DLPC410 Controller

D_IN = pin K11 of DLPC910 Controller and DLPC410 Controller

3.5 Approved SPI PROMs

The list of Xilinx approved SPI PROMs for Virtex-5 can be found in the device listing in the **Xilinx ISE Impact Tool Version 14.1**.

Note

During the PCB re-design, ensure you leave the existing secure PROM (DLPR410, DLPR910) in the design and just add layout support for the configuration SPI Flash.

3.5.1 Current List of AMD Xilinx Approved SPI Flash for Virtex-5

Manufacturer	Part Number
Adesto Technologies	AT45DB321E
ISSI	IS25LP128
Infineon	S25FL064P
Infineon	S25FL128
Infineon	S25FL128LAGMFM010
Infineon	S25FL129P

3.5.2 Xilinx Support Forum

For further support contact AMD Xilinx Support Forum http://support.xilinx.com/.

4 Common Question and Answers

1. Can we use any of the of AMD Xilinx approved SPI PROMs?

   Yes the list is provided by AMD Xilinx of the SPI flash they support with the Virtex-5. If you have specific questions please contact AMD Xilinx.

2. Would we buy them via TI or at a distributor?

   TI will not be selling the SPI flash for the DLPC410, DLPC910.

3. How would be the SPI Flash be programmed?

   End customer will program the SPI flash, either before PCB assembly or via the Xilinx tools after assembly. TI will post the firmware configuration files on TI.com at: https://www.ti.com/product/DLPR410 **and** https://www.ti.com/product/DLPR910.

4. When should we start redesigning our DLPC410 and DLPC910 PCBs.

   TI recommends you compete and test your PCB redesigned by 2Q 2023. Note during your PCB redesign ensure you leave the existing secure PROM (DLPR410, DLPR910) in the design and just add layout support for the configuration SPI Flash.

5 Revision History

DATE	REVISION	NOTES
February 2023	*	Initial Release

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