

Errata to MSC1210, Datasheet Literature Number SBAS203A

The MSC1210 device conforms functionally to the product data sheet (SBAS203A), except for the anomalies described below.

Errata Index

1. Internal SRAM corruption may occur in SPI™ FIFO mode.
2. Flash memory write operation fails when an additional MOVX command is issued before the operation is complete (only when system is executing from external program memory).

Erratum #1

Brief Description of Issue

SPI FIFO mode improper operation and internal SRAM corruption.

Detailed Description of Issue

SPI data transfers occur in a circular fashion (that is, the byte residing in the master buffer transfers to the slave buffer, and vice versa). Therefore, a data write and read are both occurring in each device during an SPI transfer. When using the SPI in FIFO mode, the address and/or data during the data transfer may be corrupted by the DMA controller. If the data is corrupted during the transfer, then incorrect data may be written into internal SRAM. If the address is corrupted during the transfer, then the data will be written to an incorrect address in SRAM (the internal SRAM address range is 00h-FFh). In either case, data in the internal SRAM will be corrupted.

Impact to Customer

Use of the SPI in FIFO mode is not recommended; instead, the SPI should only be used in double-buffer mode.

SW or HW Workaround

None.

Affected Devices

MSC1210Y2, MSC1210Y3, MSC1210Y4, and MSC1210Y5.

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Erratum #2

Brief Description of Issue

Using the MOVX command (from non-boot ROM program memory) after the MSC1210 has initiated an internal flash write may cause the flash memory to become corrupted.

Detailed Description of Issue

When a flash write is initiated by the MOVX @DPTR, ACC command, the value in the accumulator is placed onto the data input lines of the flash memory. If another MOVX @DPTR, ACC command is issued while the write operation is still in progress, the data input lines are updated with the new accumulator value. Thus, the area in flash memory that is being written to may be corrupted by the second memory write.

Note: The address of the second MOVX has no effect on the flash write destination.

Impact to Customer

The behavior is only observed when MSC1210 is executing code from non-boot ROM program memory. It has no effect on the customer if the system is executing from flash memory or boot ROM memory. The user has to ensure the flash write is completed before executing the next write command by polling the FLSBSY bit in register FMCON. Since the length of the flash write operation is 60µs, this latency must be accounted for in the user application.

SW or HW Workaround

While flash memory is being written, ensure that the FLSBSY bit in register FMCON is low before initiating the next MOVX @DPTR, ACC command.

Affected Devices

MSC1210Y2, MSC1210Y3, MSC1210Y4, and MSC1210Y5.

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