

UR Bit Incorrectly Set in the Uncorrectable Error Status Register When the ANFES Bit Is Set

This document is provided to summarize the errata seen on XIO2213 PG 2.0 silicon during validation.

1.1 Detailed Description

After a configuration transaction to an invalid function or a memory transaction to in an invalid memory window of the XIO2213, the Unsupported Request bit in the Uncorrectable Error Status Register and the Advisory Non-Fatal Error Status bit in the Correctable Error Status Register are both set. In this scenario, only the Advisory Non-Fatal Error Status bit should be set as this does not result in an uncorrectable error.

1.2 Overall Impact

This causes a failure in the PCI SIG PTC Gold suite testing to Spec. revision 1.1. Revision 1.0a will continue to pass.

1.3 Workaround Proposal

None at this time as software does not implement AER.

1.4 Corrective Action

None for current device.

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