

# ERRATA

DATE: March 2004

Document Being Updated: 5–6 K Interface Board EVM – (SLAU104)

This Errata (SLAZ006) ships with the 5–6 K Interface Board EVM Hardware Kit.

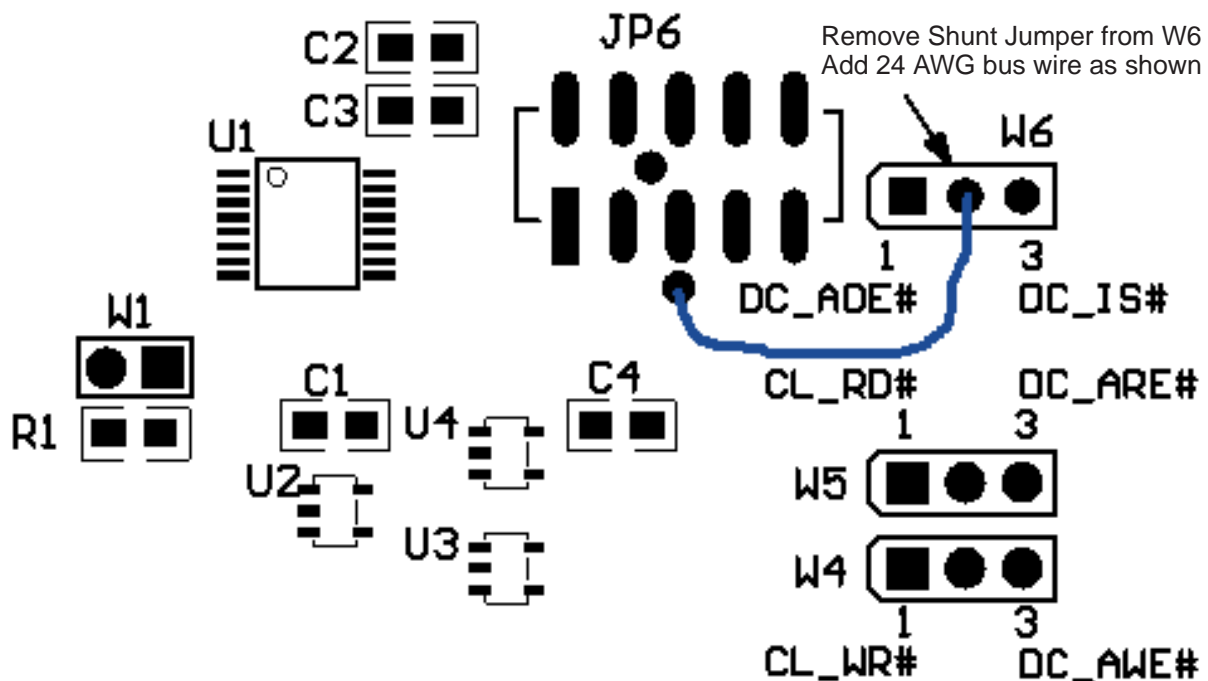
**Page:**            **Change or Add:**

N/A                PWB Revision A

A recent discovery on the 5–6K interface board may prevent parallel EVMs mounted to the interface board from being written to when used in association with C6000 series DSKs. The DC\_AOE# signal at pins 1–2 of W6 only becomes active during read operations. It does not allow the address bits to toggle through U1 during write operations.

If this functionality is critical to the operation of the parallel EVM mounted on the interface board, please completely remove the shunt jumper at W6 and tie pin 2 (the center pin) to digital ground at JP6 pin 5.

This item as well as additional enhancements will be added to the next hardware revision of the 5–6K interface board.



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