

MSP430F1132 Device Erratasheet

1 Functional Errata Revision History

Errata impacting device's operation, function or parametrics.

✓ The check mark indicates that the issue is present in the specified revision.

| Errata Number | Rev I | Rev G | Rev E |
|-----------------------|-------|-------|-------|
| ADC22 | ✓ | ✓ | ✓ |
| BCL5 | ✓ | ✓ | ✓ |
| PORT3 | ✓ | ✓ | ✓ |
| RES4 | ✓ | ✓ | ✓ |
| TA12 | ✓ | ✓ | ✓ |
| TA16 | ✓ | ✓ | ✓ |
| TA21 | ✓ | ✓ | ✓ |
| TAB22 | ✓ | ✓ | ✓ |
| US13 | ✓ | ✓ | ✓ |
| US15 | ✓ | ✓ | ✓ |
| WDG2 | ✓ | ✓ | ✓ |

2 Preprogrammed Software Errata Revision History

Errata impacting pre-programmed software into the silicon by Texas Instruments.

✓ The check mark indicates that the issue is present in the specified revision.

The device doesn't have Software in ROM errata.

3 Debug only Errata Revision History

Errata only impacting debug operation.

✓ The check mark indicates that the issue is present in the specified revision.

| Errata Number | Rev I | Rev G | Rev E |
|-----------------------|-------|-------|-------|
| EEM20 | ✓ | ✓ | ✓ |

4 Fixed by Compiler Errata Revision History

Errata completely resolved by compiler workaround. Refer to specific erratum for IDE and compiler versions with workaround.

✓ The check mark indicates that the issue is present in the specified revision.

| Errata Number | Rev I | Rev G | Rev E |
|----------------------|-------|-------|-------|
| CPU4 | ✓ | ✓ | ✓ |

Refer to the following MSP430 compiler documentation for more details about the CPU bugs workarounds.

TI MSP430 Compiler Tools (Code Composer Studio IDE)

- [MSP430 Optimizing C/C++ Compiler](#): Check the --silicon_errata option
- [MSP430 Assembly Language Tools](#)

MSP430 GNU Compiler (MSP430-GCC)

- [MSP430 GCC Options](#): Check -msilicon-errata= and -msilicon-errata-warn= options
- [MSP430 GCC User's Guide](#)


IAR Embedded Workbench

- [IAR workarounds for msp430 hardware issues](#)

5 Package Markings


DW20


SOP (DW), 20 Pin

| | |
|----------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|
|  NNNNNNN M430Fxxxx REV # ○ | # = Die revision ○ = Pin 1 location N = Lot trace code |
|----------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|

PW20

TSSOP (PW), 20 Pin

| | |
|----------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|
| 4Fxxxx  NNN # NNNN ○ | # = Die revision ○ = Pin 1 location N = Lot trace code |
|----------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|

| | |
|------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|
| 4Fxxxx  NNNG4 NNNN # ○ | # = Die revision ○ = Pin 1 location N = Lot trace code |
|------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|

RHB32

QFN (RHB), 32 Pin

| | |
|--------------------------------------------|--------------------------------------------------------------|
| ○ MSP430™ Fxxxx TI NNN# NNNNG4 | # = Die revision ○ = Pin 1 location N = Lot trace code |
|--------------------------------------------|--------------------------------------------------------------|

6 Detailed Bug Description

ADC22 *ADC10 Module*

| | |
|--------------------|---------------------------------------------------------------------------------------------|
| Category | Functional |
| Function | ADC10MEM register is not read only |
| Description | The ADC10MEM register is read and writable and not read only as stated in the user's guide. |
| Workaround | None |

BCL5 *BCS Module*

| | |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Category | Functional |
| Function | RSELx bit modifications can generate high frequency spikes on MCLK |
| Description | When DIVMx = 00 or 01 the RSELx bits of the Basic Clock Module are incremented or decremented in steps of 2 or greater, the DCO output may momentarily generate high frequency spikes on MCLK, which may corrupt CPU operation. This is not an issue when DIVMx = 10 or 11. |
| Workaround | Set DIVMx = 10 or 11 to divide the MCLK input prior to modifying RSELx. After the RSELx bits are configured as desired, the DIVMx setting can be changed back to the original selection. |

CPU4 *CPU Module*

| | |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Category | Compiler-Fixed |
| Function | PUSH #4, PUSH #8CPU4 - Bug |
| Description | The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The number of clock cycles is different: PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction |
| Workaround | Refer to the table below for compiler-specific fix implementation information. |

| IDE/Compiler | Version Number | Notes |
|-------------------------------------------------|-----------------------------------|---------------------------------------------------------------------------------|
| IAR Embedded Workbench | IAR EW430 v2.x until v6.20 | User is required to add the compiler flag option below. --hw_workaround=CPU4 |
| IAR Embedded Workbench | IAR EW430 v6.20 or later | Workaround is automatically enabled |
| TI MSP430 Compiler Tools (Code Composer Studio) | v1.1 or later | |
| MSP430 GNU Compiler (MSP430-GCC) | MSP430-GCC 4.9 build 167 or later | |

| | |
|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EEM20 | <i>EEM Module</i> |
| Category | Debug |
| Function | Debugger might clear interrupt flags |
| Description | During debugging read-sensitive interrupt flags might be cleared as soon as the debugger stops. This is valid in both single-stepping and free run modes. |
| Workaround | None. |
| PORT3 | <i>PORT Module</i> |
| Category | Functional |
| Function | Port interrupts can get lost |
| Description | Port interrupts can get lost if they occur during CPU access of the P1IFG and P2IFG registers. |
| Workaround | None |
| RES4 | <i>RESET Module</i> |
| Category | Functional |
| Function | No reset if external resistor exceeds certain value |
| Description | <p>No reset of the device is performed if the external pull down resistor on RST/NMI pin is above a certain limit. The limits are:</p> <p>Vcc = 1.8V: maximum pull down resistor = 12 kohm</p> <p>Vcc = 3.0V: maximum pull down resistor = 5 kohm</p> <p>Vcc = 3.6V: maximum pull down resistor = 2.5 kohm</p> <p>In addition, a higher current consumption occurs during high/low RST/NMI signal transition when using improper resistors.</p> |
| Workaround | Use external pulldown resistors below the listed values or directly drive RST/NMI low to generate a reset. |
| TA12 | <i>TIMER_A Module</i> |
| Category | Functional |
| Function | Interrupt is lost (slow ACLK) |
| Description | <p>Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the Timer_A counter has incremented again. Therefore the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.</p> |

Workaround Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TA16 *TIMER_A Module*

Category Functional

Function First increment of TAR erroneous when IDx > 00

Description The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

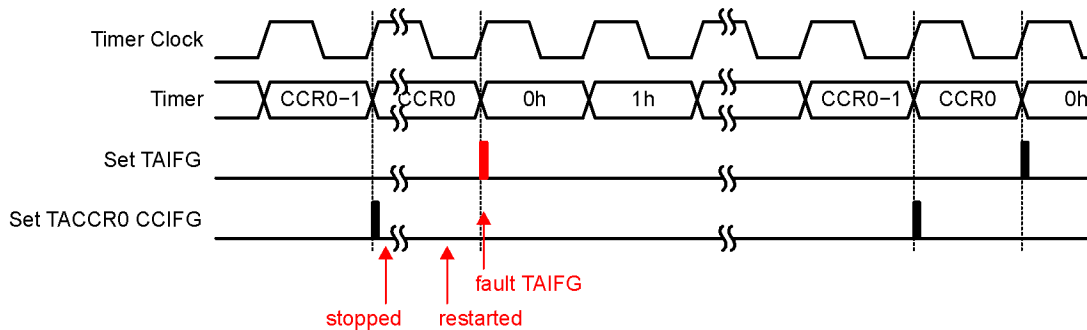
Workaround None

TA21 *TIMER_A Module*

Category Functional

Function TAIFG Flag is erroneously set after Timer A restarts in Up Mode

Description In Up Mode, the TAIFG flag should only be set when the timer counts from TACCR0 to zero. However, if the Timer A is stopped at TAR = TACCR0, then cleared (TAR=0) by setting the TACLR bit, and finally restarted in Up Mode, the next rising edge of the TACLK will erroneously set the TAIFG flag.



Workaround None.

TAB22 *TIMER_A/TIMER_B Module*

Category Functional

Function Timer_A/Timer_B register modification after Watchdog Timer PUC

Description Unwanted modification of the Timer_A/Timer_B registers TACTL/TBCTL and TAIV/TBIV can occur when a PUC is generated by the Watchdog Timer(WDT) in Watchdog mode and any Timer_A/Timer_B counter register TACCRx/TBCCRx is incremented/decremented (Timer_A/Timer_B does not need to be running).

Workaround Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC may not fully initialize the register). TAIV/TBIV is automatically cleared following this initialization.

Example code:

```
MOV.W #VAL, &TACTL
```

or

```
MOV.W #VAL, &TBCTL
```

Where, VAL=0, if Timer is not used in application otherwise, user defined per desired function.

US13

USART Module

Category

Functional

Function

Unpredictable program execution

Description

USART interrupts requested by URXS can result in unpredictable program execution if this request is not served within two bit times of the received data.

Workaround

Ensure that the interrupt service routine is entered within two bit times of the received data.

US15

USART Module

Category

Functional

Function

UART receive with two stop bits

Description

USART hardware does not detect a missing second stop bit when SPB = 1.

The Framing Error Flag (FE) will not be set under this condition and erroneous data reception may occur.

Workaround

None (Configure USART for a single stop bit, SPB = 0)

WDG2

WDT Module

Category

Functional

Function

Incorrectly accessing a flash control register

Description

If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to the expected PUC.

Workaround

None

7 Document Revision History

Changes from family erratasheet to device specific erratasheet.

1. Package DW28 was removed
2. Package PW28 was removed
3. Errata TA22 was renamed to TAB22
4. Description for TAB22 was updated

Changes from device specific erratasheet to document Revision A.

1. Errata EEM20 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. Errata TA21 was added to the errata documentation.

Changes from document Revision B to Revision C.

1. Silicon Revision I was added to the errata documentation.

Changes from document Revision C to Revision D.

1. Package Markings section was updated.

Changes from document Revision D to Revision E.

1. TA21 Description was updated.

Changes from document Revision E to Revision F.

1. Function for CPU4 was updated.
2. Workaround for CPU4 was updated.

Changes from document Revision F to Revision G.

1. Erratasheet format update.
2. Added errata category field to "Detailed bug description" section

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated