*Errata*
# MSP430G2332 Microcontroller

![Texas Instruments logo]

**ABSTRACT**

This document describes the known exceptions to the functional specifications (advisories).

## Table of Contents

# 1 Functional Advisories

Advisories that affect the device's operation, function, or parametrics.

✓ The check mark indicates that the issue is present in the specified revision.

| Errata Number | Rev B | Rev A |
|---|---|---|
| BCL12 | ✓ | ✓ |
| BCL14 | ✓ | ✓ |
| SYS15 | ✓ | ✓ |
| TA12 | ✓ | ✓ |
| TA16 | ✓ | ✓ |
| TA21 | ✓ | ✓ |
| TAB22 | ✓ | ✓ |
| USI4 | ✓ | ✓ |
| USI5 | ✓ | ✓ |
| XOSC5 | ✓ | ✓ |

# 2 Preprogrammed Software Advisories

Advisories that affect factory-programmed software.

✓ The check mark indicates that the issue is present in the specified revision.

The device does not have any errata for this category.

# 3 Debug Only Advisories

Advisories that affect only debug operation.

✓ The check mark indicates that the issue is present in the specified revision.

| Errata Number | Rev B | Rev A |
|---|---|---|
| EEM20 | ✓ | ✓ |

# 4 Fixed by Compiler Advisories

Advisories that are resolved by compiler workaround. Refer to each advisory for the IDE and compiler versions with a workaround.

✓ The check mark indicates that the issue is present in the specified revision.

| Errata Number | Rev B | Rev A |
|---|---|---|
| CPU4 | ✓ | ✓ |

Refer to the following MSP430 compiler documentation for more details about the CPU bugs workarounds.

**TI MSP430 Compiler Tools (Code Composer Studio IDE)**

- MSP430 Optimizing C/C++ Compiler: Check the --silicon_errata option
- MSP430 Assembly Language Tools

**MSP430 GNU Compiler (MSP430-GCC)**

- MSP430 GCC Options: Check -msilicon-errata= and -msilicon-errata-warn= options
- MSP430 GCC User's Guide

**IAR Embedded Workbench**

- IAR workarounds for msp430 hardware issues

# 5 Nomenclature, Package Symbolization, and Revision Identification

The revision of the device can be identified by the revision letter on the Package Markings or by the HW_ID located inside the TLV structure of the device.

## 5.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

**XMS** – Experimental device that is not necessarily representative of the final device's electrical specifications

**MSP** – Fully qualified production device

Support tool naming prefixes:

**X**: Development-support product that has not yet completed Texas Instruments internal qualification testing.

**null**: Fully-qualified development-support product.

XMS devices and X development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format.
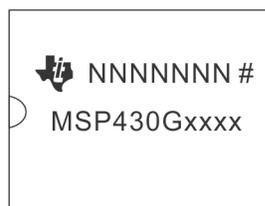
## 5.2 Package Markings

**PW14**                    *TSSOP (PW), 14 Pin*

```
┌──────────────────────┐
│    Gxxxx             │        #  = Die revision
│  🔴 NNNG4           │        ○  = Pin 1 location
│    NNNN #           │        N  = Lot trace code
│ ○                    │
└──────────────────────┘
```

**N20**                    *PDIP (N), 20 Pin*

```
┌──────────────────────┐
│ 🔴 NNNNNNN #        │        #  = Die revision
│ ⌐ MSP430Gxxxx       │        N  = Lot trace code
│                      │
│                      │
└──────────────────────┘
```

**PW20**                    *TSSOP (PW), 20 Pin*

```
┌─────────────────────┐
│    Gxxxx            │
│  [ti] NNNG4         │
│    NNNN #           │
│ ○                   │
└─────────────────────┘
```

| | |
|---|---|
| # | = Die revision |
| ○ | = Pin 1 location |
| N | = Lot trace code |

**RSA16**          *QFN (RSA), 16 Pin*

```
┌─────────────────────┐
│ ○                   │
│    M430G            │
│    xxxx             │
│    TI NNN #         │
│    NNNN             │
└─────────────────────┘
```

| | |
|---|---|
| # | = Die revision |
| ○ | = Pin 1 location |
| N | = Lot trace code |
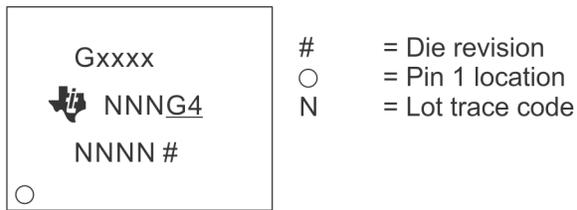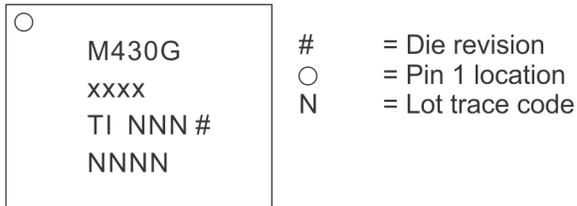
## 5.3 Memory-Mapped Hardware Revision (TLV Structure)

This device does not support reading the hardware revision from memory.

Further guidance on how to locate the TLV structure and read out the HW_ID can be found in the device User's Guide.

# 6 Advisory Descriptions

**BCL12**          *BCL Module*

**Category**       Functional

**Function**       Switching RSELx or modifying DCOCTL can cause DCO dead time or a complete DCO stop

**Description**    After switching RSELx bits (located in register BCSCTL1) from a value of >13 to a value of <12 OR from a value of <12 to a value of >13, the resulting clock delivered by the DCO can stop before the new clock frequency is applied. This dead time is approximately 20 us. In some instances, the DCO may completely stop, requiring a power cycle.

Furthermore, if all of the RSELx bits in the BSCTL1 register are set, modifying the DCOCTL register to change the DCOx or the MODx bits could also result in DCO dead time or DCO hang up.

**Workaround**     - When switching RSEL from >13 to <12, use an intermediate frequency step. The intermediate RSEL value should be 13.

| Current RSEL | Target RSEL | Recommended Transition Sequence |
|---|---|---|
| 15 | 14 | Switch directly to target RSEL |
| 14 or 15 | 13 | Switch directly to target RSEL |
| 14 or 15 | 0 to 12 | Switch to 13 first, and then to target RSEL (two step sequence) |
| 0 to 13 | 0 to 12 | Switch directly to target RSEL |

AND

- When switching RSEL from <12 to >13 it's recommended to set RSEL to its default value first (RSEL = 7) before switching to the desired target frequency.

AND
- In case RSEL is at 15 (highest setting) it's recommended to set RSEL to its default value first (RSEL = 7) before accessing DCOCTL to modify the DCOx and MODx bits. After the DCOCTL register modification the RSEL bits can be manipulated in an additional step.

In the majority of cases switching directly to intermediate RSEL steps as described above will prevent the occurrence of BCL12. However, a more reliable method can be implemented by changing the RSEL bits step by step in order to guarantee safe function without any dead time of the DCO.

Note that the 3-step clock startup sequence consisting of clearing DCOCTL, loading the BCSCTL1 target value, and finally loading the DCOCTL target value as suggested in the in the "TLV Structure" chapter of the MSP430x2xx Family User's Guide is not affected by BCL12 if (and only if) it is executed after a device reset (PUC) prior to any other modifications being made to BCSCTL1 since in this case RSEL still is at its default value of 7. However any further changes to the DCOx and MODx bits will require the consideration of the workaround outlined above.

**BCL14**          *BCL Module*

**Category**       Functional

**Function**       Oscillator fault forced in bypass mode when P2SEL.7 bit is not set

**Description**     When the LFXT1 oscillator is used in bypass mode and P2SEL.7 is not set, the oscillator fault flag (OFIFG) will be forced to set and cannot be cleared. Due to the failsafe logic, LFXT1 cannot be used as MCLK in this case. The bug only affects the behavior of the oscillator fault, the clocking itself works properly.

**Workaround**     Set both P2SEL.6 and P2SEL.7 if the application requires correct function of the oscillator fault flag (e.g. MCLK failsafe logic).

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**Note**

Setting P2SEL.7 bit disables the GPIO functionality and enables the input schmitt trigger of the pin. P2.7 should be tied to a fixed voltage level (VCC or GND) to prevent cross current.

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**CPU4**     *CPU Module*

**Category**     Compiler-Fixed

**Function**     PUSH #4, PUSH #8

**Description**     The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The number of clock cycles is different:

PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction
PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

**Workaround**     Refer to the table below for compiler-specific fix implementation information.

| IDE/Compiler | Version Number | Notes |
|---|---|---|
| IAR Embedded Workbench | IAR EW430 v2.x until v6.20 | User is required to add the compiler flag option below. --hw_workaround=CPU4 |
| IAR Embedded Workbench | IAR EW430 v6.20 or later | Workaround is automatically enabled |
| TI MSP430 Compiler Tools (Code Composer Studio) | v1.1 or later | |
| MSP430 GNU Compiler (MSP430-GCC) | MSP430-GCC 4.9 build 167 or later | |

**EEM20**     *EEM Module*

**Category**     Debug

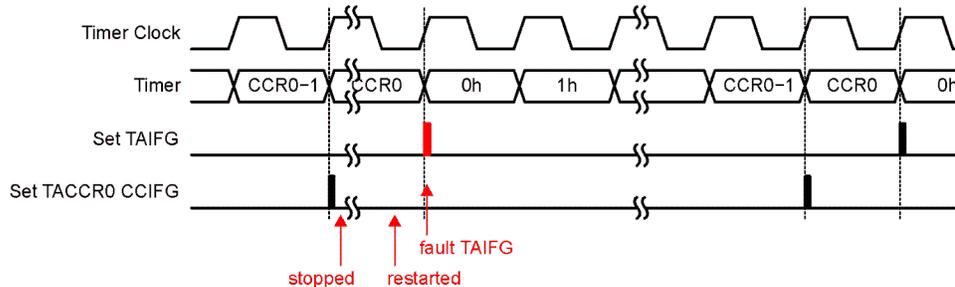**Function**     Debugger might clear interrupt flags

**Description**     During debugging read-sensitive interrupt flags might be cleared as soon as the debugger stops. This is valid in both single-stepping and free run modes.

**Workaround**     None.

**SYS15**     *SYS Module*

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| Category | Functional |
|---|---|
| **Function** | LPM3 and LPM4 currents exceed specified limits |
| **Description** | LPM3 and LPM4 currents may exceed specified limits if the SMCLK source is switched from DCO to VLO or LFXT1 just before the instruction to enter LPM3 or LPM4 mode. |
| **Workaround** | After clock switching, a delay of at least four new clock cycles (VLO or LFXT1) must be implemented to complete the clock synchronization before going into LPM3 or LPM4. |

## TA12 — *TA Module*

| Category | Functional |
|---|---|
| **Function** | Interrupt is lost (slow ACLK) |
| **Description** | Timer_A counter is running with slow clock (external TACLK or ACLK)compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the Timer_A counter has incremented again. Therefore the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt gets lost. |
| **Workaround** | Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards. |

## TA16 — *TA Module*

| Category | Functional |
|---|---|
| **Function** | First increment of TAR erroneous when IDx > 00 |
| **Description** | The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings. |
| **Workaround** | None |

## TA21 — *TA Module*

| Category | Functional |
|---|---|
| **Function** | TAIFG Flag is erroneously set after Timer A restarts in Up Mode |
| **Description** | In Up Mode, the TAIFG flag should only be set when the timer counts from TACCR0 to zero. However, if the Timer A is stopped at TAR = TACCR0, then cleared (TAR=0) by setting the TACLR bit, and finally restarted in Up Mode, the next rising edge of the TACLK will erroneously set the TAIFG flag. |

| | | |
|---|---|---|
| **Workaround** | None. | |

---

| **TAB22** | *TAB Module* |
|---|---|
| **Category** | Functional |
| **Function** | Timer_A/Timer_B register modification after Watchdog Timer PUC |
| **Description** | Unwanted modification of the Timer_A/Timer_B registers TACTL/TBCTL and TAIV/TBIV can occur when a PUC is generated by the Watchdog Timer(WDT) in Watchdog mode and any Timer_A/Timer_B counter register TACCRx/TBCCRx is incremented/decremented (Timer_A/Timer_B does not need to be running). |
| **Workaround** | Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC may not fully initialize the register). TAIV/TBIV is automatically cleared following this initialization. |

Example code:

```
MOV.W #VAL, &TACTL
or
MOV.W #VAL, &TBCTL
```

Where, VAL=0, if Timer is not used in application otherwise, user defined per desired function.

---

| **USI4** | *USI Module* |
|---|---|
| **Category** | Functional |
| **Function** | I2C Slave mode can generate a glitch at SCL |
| **Description** | USI I2C Slave Operation at slower communication rates (less than 20kbps). During I2C bus active operation, if USICNT is written while SCL is high, I2C module will generate a glitch on SCL that can corrupt the I2C bus sequence. |
| **Workaround** | Verify that SCL is low before writing USICNT register. |

```
//STOP
---END---
```
For HP8/G2MICRO/MSP430V334 device, the erratum is listed as I2C1.

I2C16: MSP430V334 I2C Slave Mode

Function: MSP430V334 I2C Slave Device can generate a glitch on SCL

Description: MSP430V334 I2C slave operation can generate glitches when operated at

slow communication rates (less than 20 kbps) and this can corrupt the I2C bus sequence.

Workaround: None

| | |
|---|---|
| **USI5** | ***USI Module*** |
| **Category** | Functional |
| **Function** | SPI master generates one additional clock after module reset Bug |
| **Description** | Initalizing the USI in SPI MASTER mode with the USICKPH bit set generates one additional clock pulse than defined by the value in the USICNTx bits on the SCLK pin during the first data transfer after module reset. For example, if the USICNTx bits hold the value eight, nine clock pulses are generated on the SCLK pin for the first transfer only. |
| **Workaround** | Load USICNTx with a count of N-1 bits (where N is the required number of bits) for the first transfer only. |

| | |
|---|---|
| **XOSC5** | ***XOSC Module*** |
| **Category** | Functional |
| **Function** | LF crystal failures may not be properly detected by the oscillator fault circuitry |
| **Description** | The oscillator fault error detection of the LFXT1 oscillator in low frequency mode (XTS = 0) may not work reliably causing a failing crystal to go undetected by the CPU, i.e. OFIFG will not be set. |
| **Workaround** | None |

# 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from May 12, 2021 to May 17, 2021**                      **Page**

- Changed the document format and structure; updated the numbering format for tables, figures, and cross references throughout the document.................................................................................................................6

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