

Errata

ADS1274EVM-PDK / ADS1278EVM-PDK (PCB Revision F)

Affected EVMs	ADS1274EVM-PDK, PCB Rev F, BOM Rev E ADS1278EVM-PDK, PCB Rev F, BOM Rev E
Problem Description:	Pin 3 of DIP switch S2 is permanently shorted to the GND plane. This pin drives the CLKDIV pin on the ADS1274/8. CLKDIV is a digital input that sets the modulator frequency for the device.
Affected Modes of Operation:	Low-Speed Mode Low-Power Mode High-Resolution Mode
Low-Speed Mode:	In Low-Speed Mode, CLKDIV = 0 is a supported configuration and the device will perform as expected in this mode. The user will not be able to change CLKDIV to 1 using neither the GUI nor the DIP switch S2. The GUI software will still allow the user to select CLKDIV = 1, but the hardware will not reflect this setting. Therefore, the master clock frequency has to be limited to 5.4 MHz using the PLL setting in the GUI or by an external clock.
Low-Power Mode:	In Low-Power Mode, CLKDIV = 0 is a supported configuration and the device will perform as expected in this mode. The user will not be able to change CLKDIV to 1 using neither the GUI nor the DIP switch S2. The GUI software will still allow the user to select CLKDIV = 1, but the hardware will not reflect this setting. Therefore, the master clock frequency has to be limited to 13.5 MHz using the PLL setting in the GUI or by an external clock.
High-Resolution Mode:	In High-Resolution Mode, CLKDIV = 0 is not a supported configuration of the device. The device performance cannot be evaluated in this mode using this EVM revision.

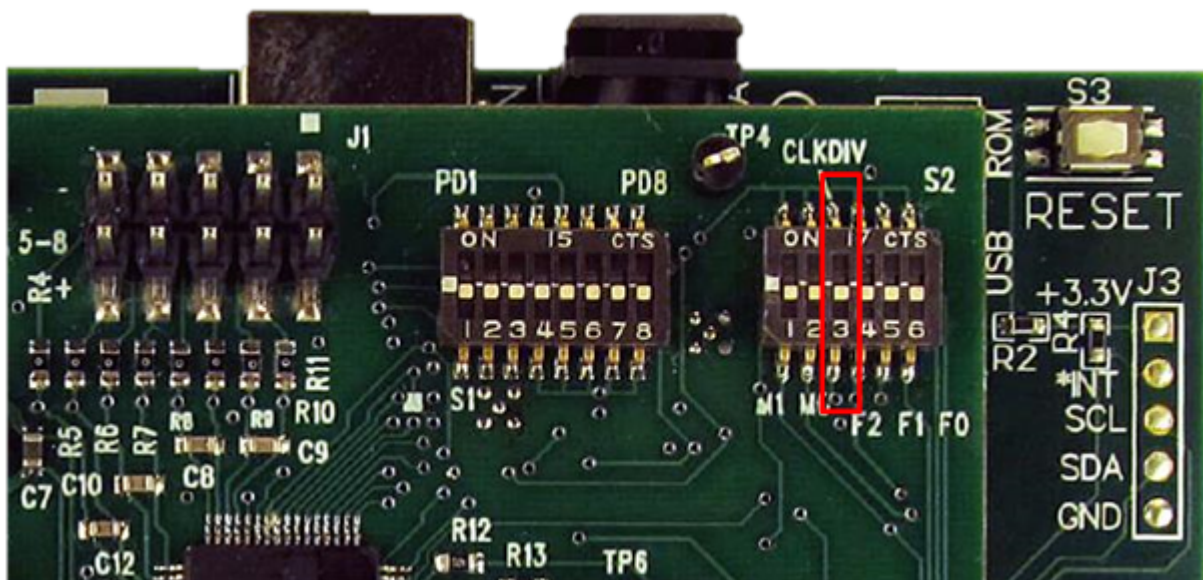


Figure 1. Highlighting Affected DIP Switch

Table 1 provides an overview of the different device operation modes. The modes highlighted in red cannot be evaluated with this EVM PCB revision.

Table 1. Operating Modes

Mode Selection	MODE [1:0]	CLKDIV	Max f_{CLK} (MHz)	f_{MOD}	OSR = f_{MOD}/f_{DATA}
High-Speed	00	X ⁽¹⁾	37	$f_{CLK}/4$	64
High-Resolution	01	1 0 ⁽²⁾	27 – ⁽²⁾	$f_{CLK}/4$ – ⁽²⁾	128 – ⁽²⁾
Low-Power	10	1 0	27 13.5	$f_{CLK}/8$ $f_{CLK}/4$	64 64
Low-Speed	11	1 0	27 5.4	$f_{CLK}/40$ $f_{CLK}/8$	64 64

⁽¹⁾ CLKDIV setting ignored in High-Speed mode

⁽²⁾ Setting not supported by device

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