TAS5508A Errata

1 Bass/Treble Filter Set

1.1 Problem Description

The TAS5508A has an intermittent problem when writing to the treble and bass filter-set registers or when a sample-rate change occurs which causes the bank switching in the TAS5508A to write these registers.

1.2 System Impact

Audio might be corrupted in a few channels.

1.3 Workaround

The filter-set registers should be written twice with at least 1.375 ms (66 LRCLKs @ 48 kHz) between writes. The high-pass filter should be enabled to prevent dc output. Do not use bass/treble filter-set update as a part of bank switching.

1.4 Comments

This issue will be corrected in all future releases of this device.

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2 PWM Channels Shut Down

2.1 Problem Description

A PWM channel could lose output if, following a sample-rate-change event, another sample-rate-change event occurs while the volume unmute transition is in progress (volume is muted and then unmuted for a sample-rate change).

2.2 System Impact

One PWM channel could lose its audio output.

2.3 Workaround

Enable the hard unmute bit to minimize the chance of occurrence during a sample-rate change.

2.4 Comments

This issue will be corrected in all future releases of this device.

3 Soft Mute

3.1 Problem Description

If the output mixer has a nondefault configuration, then an incorrect PWM channel stops as a response to channel mute.

3.2 System Impact

Wrong channels mutes when MUTE command is issued. So, channel soft mute should not be used with output mixing.

3.3 Workaround

Use a low channel volume (Master + Ch > –109 dB; 0x1FC) and enable automute, or do not use output mixing.

3.4 Comments

This issue will be corrected in all future releases of this device.

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4 Channel-4 Audio Corruption

4.1 Problem Description

Occasionally, the channel-4 biquad becomes corrupted when a DAP coefficient update occurs during a volume ramp.

4.2 System Impact

When this problem occurs, channel-4 audio is corrupted.

4.3 Workaround

Wait until volume ramp is complete to write any DAP coefficient. Time is slew-rate dependent, as set in register 0xD0.

4.4 Comments

This issue will be corrected in all future releases of this device.

5 AM-Mode Disable

5.1 Problem Description

The TAS5508A continues to use the AM-mode switching frequency even after the AM-mode disable bit has been set.

5.2 System Impact

The TAS5508A remains at the AM-mode switching frequency, which could result in decreased dynamic range.

5.3 Workaround

1. Put the TAS5508A in mute. Write to register 0xD9 (data = 0x0000 0245).
2. Write to register 0x2F (data = 0x81).
3. Write to register 0x00 (data = 0x6D).
4. Write to register 0xDE (data = 0x0010 0520).
5. Write to AM interference avoidance register to disable AM interference. Write to register 0xDE (data = 0x0000 0000).
6. Write to register 0x2F (data = 0x80).
7. Write to register 0x2F (data = 0x00).
8. Unmute the TAS5508A. Write original volume value to register 0xD9.

5.4 Comments

This issue will be corrected in all future releases of this device.

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6 PSVC Control when Using Subwoofer as Lineout

6.1 Problem Description

Volume corruption can occur when the subwoofer is configured as lineout while PSVC is enabled.

One of the PSVC modes is called *subwoofer not part of PSVC calculation*. Normally, this mode is used when the subwoofer is configured as lineout. However, an audible problem occurs during volume changes. In this case, the subwoofer is always used for PSVC calculation even though it is configured not to do so (e.g., as lineout). So, during the volume ramp, the transient values are not correct, thereby creating audible artifacts.

6.2 System Impact

When the subwoofer is configured as lineout with PSVC enabled, audible artifacts can occur during volume changes.

6.3 Workaround

None. The subwoofer cannot be used as lineout if PSVC is enabled.

7 Use of 5-V CMOS I²C Drivers

7.1 Problem Description

In systems using 5-V CMOS buffers for the I²C interface, special pullup resistors are required.

The I²C specification requires that V_{IH} is $0.7 \times V_{DD} = 3.5$ V when V_{DD} is 5 V. In some 5-V CMOS systems, the normal value for the I²C pullup resistor is 4.7 kΩ. This could cause the voltage not to rise above 3.47 V, which violates the specification. The root cause has been identified as a TAS5508B 5-V-tolerant buffer issue.

7.2 System Impact

1. No impact for 3.3-V operation.
2. No impact for TTL operation.
3. Impact only for 5-V CMOS operation where V_{IH} could be lower than the specification of 3.5 V.

7.3 Workaround

It is recommended that the I²C pullup resistors R_P be 3.3 kΩ (see Figure 1). If there is a series resistor in the circuit (see Figure 2), then the series resistor R_S should be less than or equal to 300 Ω.

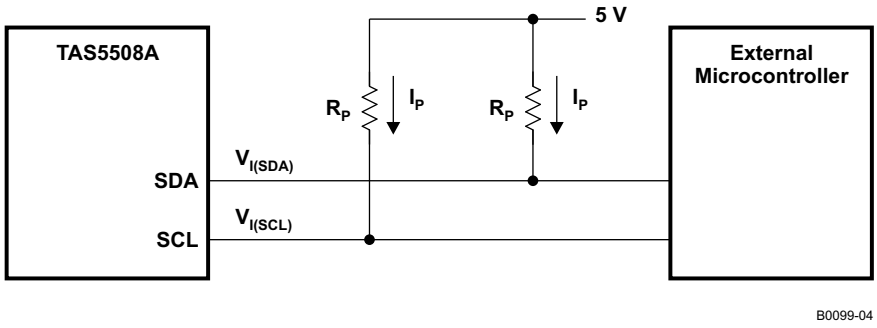
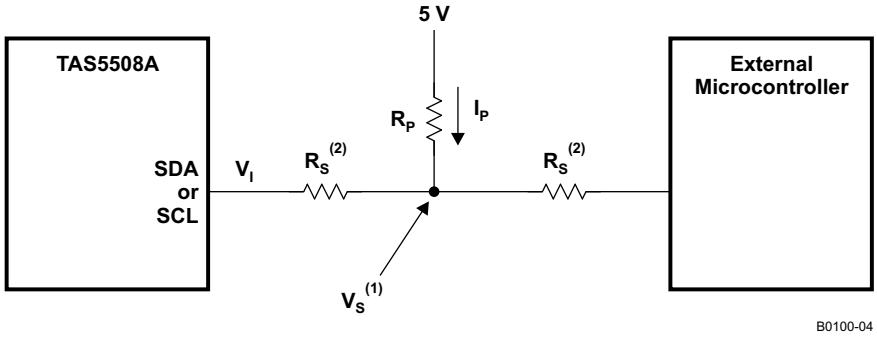


Figure 1. I²C Pullup Circuit (With No Series Resistor)



(1) $V_S = 5 \times R_S/(R_S + R_P)$. When driven low, $V_S << V_{IL}$ requirements.

(2) $R_S \leq 300\ \Omega$

Figure 2. I²C Pullup Circuit (With Series Resistor)

8 One-Sample Delay in Channels 3, 4, 7, and 8

8.1 Problem Description

The TAS5508A exhibits a one-sample delay on channels 3, 4, 7, and 8 for sample rates of 32, 44.1, and 48 kHz. The delay occurs in the PWM section.

8.2 System Impact

This time misalignment can impact applications where the TAS5508A is used to provide crossover filtering and bi-amplification, as in powered loudspeakers. The problem that occurs in these cases is that a one-sample time delay between either the high-pass or low-pass path causes an error in the overall crossover frequency response.

The one-sample delay is not anticipated to cause any impact in other applications, because this corresponds to relatively small position change, 7,19 mm or 0.28 in. for a 48-kHz sample rate.

8.3 Workaround

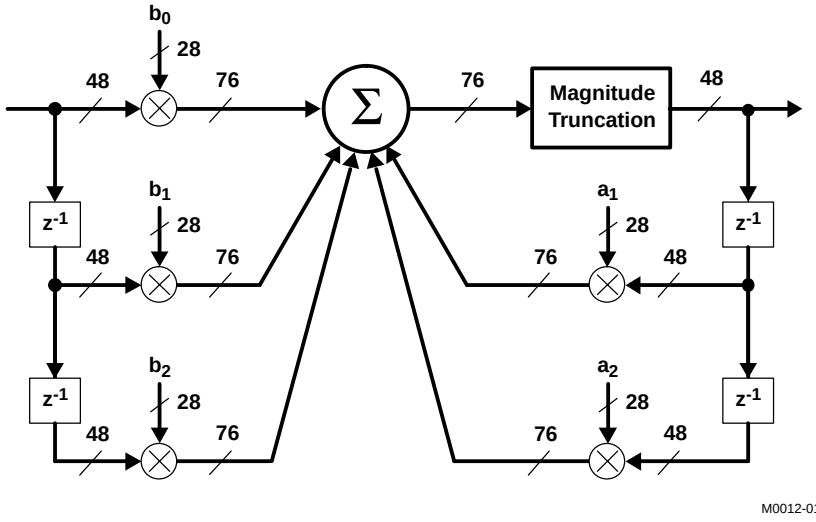
The time misalignment can be corrected by using a biquad to provide a one-sample delay for each of the nondelayed PWM channels for the 48-, 44.1-, and 32-kHz sample rates.

An example of this solution is the following:

When the 8 × 2 crossbar mixer provides a 1:1 input-to-output connection, an eight-channel loudspeaker configuration uses one of the seven biquads in channels 1, 2, 5, and 6 to provide a one-sample delay.

To produce a one-sample delay with one of the TAS5508A biquads:

1. Set the b1 biquad coefficients to a gain of 1.
2. Set all of the other biquad coefficients (b0, b2, a1, and a2) to a gain of 0, as shown in the following diagram and table.



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The one-sample delay setting is programmed using the following I²C register settings.

I²C SUBADDRESS	COEFFICIENT	HEX VALUE
Biquad I²C register Subaddress N	b_0—u(31:28), b0(27:24), b0(23:16), b0(15:8), b0(7:0)	0x00, 0x00, 0x00, 0x00
	b_1—u(31:28), b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0x00, 0x80, 0x00, 0x00
	b_2—u(31:28), b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0x00, 0x00, 0x00, 0x00
	a_1—u(31:28), a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0x00, 0x00, 0x00, 0x00
	a_2—u(31:28), a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0x00, 0x00, 0x00, 0x00

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