Errata to the TLK2711, 1.6-to-2.7 GBPS Transceiver Data Sheet– PLL False Lock Problem

Overview

A known device issue was recently uncovered on the TLK2711 device by a customer, in that when the device has LOOPEN enabled (in the internal loopback mode) and when the received data comprises of Ethernet Idle pattern only- the CDR (Clock Data Recovery) may false-lock to the incoming serial data (in internal loopback) 0.5UI out of phase causing erroneous data to be presented on the receive data bus (RXD0-RXD15) and error condition to be detected on RKxSB. This is a benign problem that manifests itself only when the device is in internal loopback (self-test) mode – and should not cause any device operation issues at the systems level.

Conditions of Occurrence:

Condition 1: Device is in internal loopback mode.

and

Condition 2: Device is receiving Ethernet Idle pattern only.

Solution/Workaround:

Recovering from this problem is possible by:

1. Switching the device from the internal loopback mode (toggle LOOPEN)
2. Generation of random data (such as PRBS) in place of Idle patterns

Design Fix:

Texas Instruments is making the necessary design fix to ensure that TLK2711A device does not have this issue. The new device TLK2711A will be a pin-for-pin drop-in replacement for the TLK2711 and is the recommended solution for this issue. Other than fixing this false lock problem- the new device will be the same as the previous device in form, fit, and function and performance and therefore should not necessitate any additional action.

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