TMS320UC5409/TMS320VC5409

Digital Signal Processors

Silicon Errata

TEXAS INSTRUMENTS

Contents

TEXAS
INSTRUMENTS

1   Introduction

This document describes the silicon updates to the functional specifications for the TMS320UC5409/ TMS320VC5409. The updates are applicable to:

- TMS320UC5409 (144-pin LQFP, PGE suffix)

- TMS320UC5409 (144-pin MicroStar BGA™, GGU suffix)

- TMS320VC5409 (144-pin LQFP, PGE suffix)

- TMS320VC5409 (144-pin MicroStar BGA™, GGU suffix)

1.1   Quality and Reliability Conditions

TMX Definition

Texas Instruments (TI) does not warranty either (1) electrical performance to specification, or (2) product reliability for products classified as "TMX." By definition, the product has not completed data sheet verification or reliability performance qualification according to TI Quality Systems Specifications.

The mere fact that a "TMX" device was tested over a particular temperature and voltage ranges should not, in any way, be construed as a warranty of performance.

TMP Definition

TI does not warranty product reliability for products classified as "TMP." By definition, the product has not completed reliability performance qualification according to TI Quality Systems Specifications; however, products are tested to a published electrical and mechanical specification.

TMS Definition

Fully-qualified production device.

MicroStar BGA is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

1.2 Revision Identification

The device revision can be determined by the lot trace code marked on the top of the package. The locations for the lot trace codes for the PGE and the GGU packages are shown in Figure 1 and Figure 2, respectively.

Figure 1. Example, Typical Lot Trace Code for TMS320VC5409 (PGE)

Lot trace code without second letter

Lot trace code with A
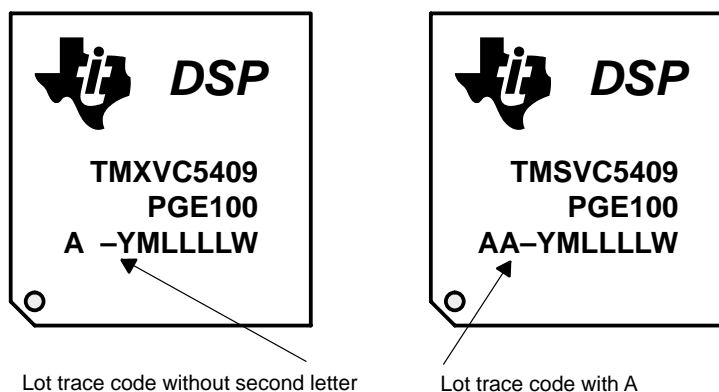
Lot Trace Code	Silicon Revision	Comments
Blank (no second letter in prefix)	Initial Silicon	This silicon revision is available in TMX and TMS versions.
A (second letter in prefix is an "A")	Silicon Revision A	This silicon revision is available as TMS (production).

Figure 2. Example, Typical Lot Trace Code for TMS320VC5409 (GGU)
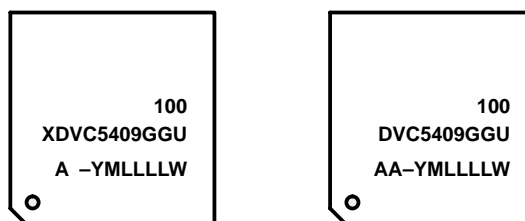
NOTE: Qualified devices in the PGE package are marked with the letters "TMS" at the beginning of the device name, while nonqualified devices in the PGE package are marked with the letters "TMX" or "TMP" at the beginning of the device name. Similarly, qualified devices in the GGU package are marked with the letters "DV" at the beginning of the device name, and nonqualified devices in the GGU package are marked with the letters "XDV" or "PDV" at the beginning of the device name.

2 Known Design Marginality/Exceptions to Functional Specifications

Table 1. Summary of Exceptions

Description	Revision Affected	Page
DMPREC	Initial and Revision A Silicon	6
Round (RND) Instruction Clears Pending Interrupts	Initial and Revision A Silicon	7
Far Branches/Calls/Interrupts from Active Repeat Blocks (BRAF)	Initial and Revision A Silicon	7
NMI	Initial and Revision A Silicon	8
HPI Hint	Initial and Revision A Silicon	8
McBSP BCLKX/BCLKR Mux	Initial and Revision A Silicon	8
Bootloader Serial EEPROM Mode	Initial Silicon	9
Bootloader McBSP Serial EEPROM Init	Initial Silicon	9
Bootloader Destination Address in 8-Bit Parallel Mode	Initial Silicon	9
Boundoff	Initial Silicon	10
Bootloader End-of-Boot Detection in 8-Bit I/O Mode	Initial Silicon	10
DMA Overlap	Initial Silicon	11
DMA External Read/Write	Initial Silicon	11
DMA Ready Edge Detection	Initial Silicon	12
IDLE3 Current	None	12

Advisory	*DMPREC*

Revision(s) Affected: Initial Silicon and Revision A Silicon

Details: When updating the DE bits of the DMPREC register while one or more DMA channel transfers are in progress, it is possible for the write to the DMPREC to cause an additional transfer on one of the active channels.

The problem occurs when an active channel completes a transfer at the same time that the user updates the DMPREC register. When the transfer completes, the DMA logic attempts to clear the DE bit corresponding to the complete channel transfer, but the register is instead updated with the CPU write (usually an ORM instruction) which can set the bit and cause an additional transfer on the channel. Refer to the example below for further clarification:

Example:
DMPREC value = 00C1h, corresponding to the following channel activity:

Channel 0 – enabled and running.	(DE0 = 1)
Channel 1 – disabled.	(DE1 = 0)
Channel 2 – disabled.	(DE2 = 0)
Channel 3 – disabled.	(DE3 = 0)
Channel 4 – disabled.	(DE4 = 0)
Channel 5 – disabled.	(DE5 = 0)

If the following conditions occur simultaneously:

Channel 0 transfer completes and DMA logic clears DE0 internally.

User code attempts to enable another channel (e.g., ORM #2, DMPREC)

The user code will re-enable channel 0 (DMPREC value written = 00C3h), and an additional, unintended transfer will begin on channel 0.

Workaround: There are a few use conditions under which this problem does not occur. If all active DMA channels are configured in ABU mode or in auto initialization mode, then the problem does not occur because the channels remain enabled until they are disabled by user code. The problem is also avoided in applications that use only one DMA channel at a time.

Systems that use multiple DMA channels simultaneously in multiframe mode, without autoinitialization are most likely to have this problem. In such systems one of the following methods can be used to avoid the problem:

- Always wait for all channels to complete existing transfers before re-enabling any channels, and always enable all channels at the same time.

- Before enabling a channel, check the progress of any on-going transfers by reading the element and frame counts of each active channel. If any active channel is within two element transfers of completing a block transfer, then wait until the active channel completes the block transfer before writing to the DMPREC register. Otherwise, if all active channels have more than two element transfers left in a block transfer, it is safe to update the DMPREC register.

| **Advisory** | *Round (RND) Instruction Clears Pending Interrupts* |

Revision(s) Affected: Initial Silicon and Revision A Silicon

Details: The round (RND) instruction opcode is decoded incorrectly and will write to the interrupt flag register (IFR) with the data from the data write bus (E bus). Therefore, it could cause the pending interrupt to be missed.

Workaround: Replace the RND instruction with an ADD instruction as follows:

| **For this instruction ...** | **Use ...** |

```
RND src[,dst]                 ADD #1,15,src[,dst]
```

| **Advisory** | *Far Branches/Calls/Interrupts from Active Repeat Blocks (BRAF)* |

Revision(s) Affected: Initial Silicon and Revision A Silicon

Details: When a block repeat is interrupted by a far call, far branch, or interrupt to another page; and a program memory address in the called routine happens to have the same lower 16 bits as the block-repeat end address (REA), a branch to the 16-bit block-repeat start address (RSA) is executed on the current page until the block-repeat counter decrements to 0. The XPC is ignored during these occurrences.

Workaround: Use one of the following workarounds:

1. If the called routine must be on a different page and has a program memory address that has the same lower 16 bits as the REA, save ST1 and clear the BRAF in the vector table before entering the called routine with the following two instructions:

    ```
    PSHM ST1
    RSBX BRAF
    ```

    Then, restore ST1 before returning from the called routine. In the case of an interrupt service routine, these two instructions can be included in the delay slots following a delayed-branch instruction (BD) at the interrupt vector location. Then, the ST1 is restored before returning from the routine. With this method, BRAF is always inactive while in the called routine. If BRAF was not active at the time of the call, the RSBX BRAF has no effect.

2. Put the called routine on the same page as the interruptible block-repeat code. This can be achieved automatically by placing the interrupt vector table and the interrupt service routines or other called routines on the overlay pages. If this approach is used, far branches/calls are not necessary and the bug is completely avoided.

3. Avoid putting the called routine on other pages where a program memory address has the same lower 16 bits as the REA.

4. Use the BANZ instruction as a substitute for the block repeat.

TEXAS INSTRUMENTS

Advisory	*NMI*

Revision(s) Affected: Initial Silicon and Revision A Silicon

Details: An NMI can be ignored if the internal CPU interrupt logic is not adequately prepared.

Workaround: Avoid generating an NMI during the time when other interrupts are being serviced. Alternatively, use one of the other external interrupts, appropriately enabled, to serve the NMI function.

Advisory	*HPI Hint*

Revision(s) Affected: Initial Silicon and Revision A Silicon

Details: The HPI will become locked up, with HRDY stuck low, if both the host processor and the 5409 CPU write a one (1) to HINT at the same time.

Workaround: Do not perform redundant operations to the HINT bit. Both the HOST and the CPU should check to see if HINT is set before trying to write a one (1) to this bit.

For ...	**IF ...**	**Then ...**
the HOST	HINT is *not* set ...	Do not try to clear HINT by writing a one (1) to it, because the CPU may try to set it.
the CPU	HINT is *already* set...	Do not try to set HINT again by writing a one (1) to it, since the HOST may try to clear it.

Advisory	*McBSP BCLKX/BCLKR Mux*

Revision(s) Affected: Initial Silicon and Revision A Silicon

Details: The McBSP sample rate generator can reference an external clock source via BCLKX or BCLKR. This feature was designed to allow external clock references without the BCLKS pin. The internal mux cannot be used because of possible internal contention with the clock sources.

Workaround: None. Bit 7 of the McBSP pin configuration register (PCR) should be considered reserved and should always be written as zero to disable this feature.

TEXAS INSTRUMENTS

Advisory	*Bootloader Serial EEPROM Mode*

Revision(s) Affected: Initial Silicon

Details: The McBSP drives data on the rising edge of the clock, and latches input data on the falling edge; while the SPI-based EEPROMs latch input data on the rising edge of the clock, and drive data on the falling edge. This causes unreliable operation since both the McBSP and EEPROM are latching data at the same clock edge that the data signal transitions.

Workaround: Using an external inverter to invert the BCLKX signal provides a reliable bootload setup. This workaround has the disadvantage of requiring an external component.

This problem is corrected on Revision A silicon.

Advisory	*Bootloader McBSP Serial EEPROM Init*

Revision(s) Affected: Initial Silicon

Details: In the 5409 bootloader, the serial EEPROM mode can be initiated with an interrupt on the INT3 pin. The bootloader is programmed to toggle the BDX1 pin, which can be tied to the INT3 pin to signal that the serial EEPROM mode is the desired boot mode.

Workaround: Although McBSP2 is used to boot in serial EEPROM mode, the BDX1 pin on McBSP1 should be used to signal an interrupt on the INT3 pin. For corrected devices, the BDX2 pin on McBSP2 will be programmed to toggle for serial EEPROM mode.

This problem is corrected in Revision A silicon.

Advisory	*Bootloader Destination Address in 8-Bit Parallel Mode*

Revision(s) Affected: Initial Silicon

Details: When the bootloader is used in 8-bit parallel mode, the destination address may be incorrectly generated due to a sign extension error. This problem depends on the contents of the boot table and may not occur in all cases.

Workaround: D8–D15 should be pulled down or driven low during boot load in this mode.

This problem is corrected in Revision A silicon.

TEXAS INSTRUMENTS

Advisory	*Boundoff*

Revision(s) Affected: Initial Silicon

Details: The current logic implementation does not consistently ensure that the BOUNDOFF condition can be achieved. When the DSP is in the BOUNDOFF state, all output pins of the DSP are placed into the high-impedance state. The BOUNDOFF is exclusively used for testing. This does not affect debugging on the 5409.

Workaround: None. This problem is corrected in Revision A silicon.

Advisory	*Bootloader End-of-Boot Detection in 8-Bit I/O Mode*

Revision(s) Affected: Initial Silicon

Details: In 8-bit I/O boot mode, the bootloader incorrectly interprets the end of the first data block because of a failure to mask the upper bits in the accumulator when the end-of-block marker (0000h) is evaluated. The result is that code can be loaded using this mode, but the bootloader will not branch to the loaded code.
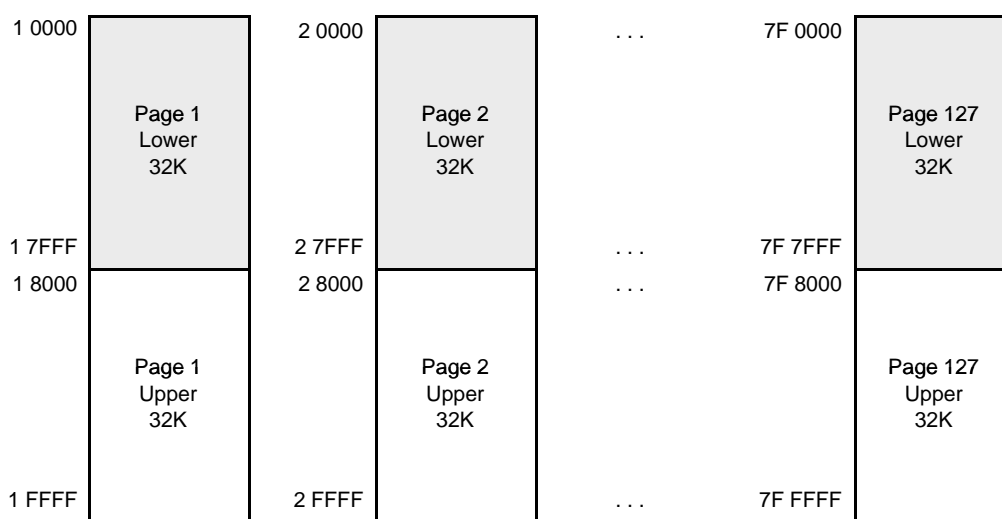
Workaround: None. This problem is corrected in Revision A silicon.

Advisory	*DMA Overlap*

Revision(s) Affected: Initial Silicon

Details: The DMA on the 5409 can access up to 128 pages of data, I/O, and program memory. When DMA write accesses are performed on the lower 32K words of extended data or program pages 1 through 127 (areas shaded in grey in Figure 3), the writes affect both the external memory location on the selected page, and the internal memory location corresponding to the same 16-bit address of page 0.

Figure 3. DMA Memory Map Extended Program/Data Pages

Workaround: The lower 32K words of extended program and data pages 1 through 127 within the DMA memory map should be considered reserved and not used.

This problem is corrected in Revision A silicon.

Advisory	*DMA External Read/Write*

Revision(s) Affected: Initial Silicon

Details: The DMA on the 5409 supports one external read and one external write simultaneously. Under a small boundary condition, the DMA will not complete the read if initiated with the write. The DMA will incorrectly signal that the read was successfully completed.

Workaround: The user can circumvent the behavior by avoiding the use of the DMA for both external reads and writes simultaneously.

This problem is corrected in Revision A silicon.

TEXAS INSTRUMENTS

Advisory	*DMA Ready Edge Detection*

Revision(s) Affected: Initial Silicon

Details: The DMA on the 5409 supports external wait states generated by the READY signal. For CPU bus cycles, READY is sampled on the falling edge of CLKOUT. For DMA accesses, READY is sampled on the rising edge of CLKOUT. The setup and hold times for READY remain the same with respect to both the rising and falling edges of CLKOUT.

Workaround: Use software wait-state generation if at all possible. If software wait-state generation cannot be used, READY timings for the DMA accesses should be referenced on the rising edges of CLKOUT. For CPU access, READY timings should be referenced to the falling edges of CLKOUT. Since the distinction between CPU and DMA cycles may not necessarily be straightforward, an enhanced memory-mapping scheme can be used in order to make this distinction, if possible, within the system architecture.

This problem is corrected in Revision A silicon.

Advisory	*IDLE3 Current*

Revision(s) Affected: None

Details: This problem does not affect any 5409 silicon revisions. This text remains as an override note for a previous revision of this document, which incorrectly states that device revision A is affected.

Workaround: Not applicable.

TEXAS
INSTRUMENTS

3   Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: **http://www.ti.com.**

To access documentation on the web site:

1. Go to **http://www.ti.com**

2. Open the "**Products**" dialog box and select "**Digital Signal Processors**"

3. Scroll to **"C54X™ DSP Generation"** and click on **"DEVICE INFORMATION"**

4. Click on a device name and then click on the documentation type you prefer.

For further information regarding the TMS320UC5409/TMS320VC5409, please refer to:

- *TMS320UC5409 Fixed-Point Digital Signal Processor* data sheet*,* literature number SPRS101

- *TMS320VC5409 Fixed-Point Digital Signal Processor* data sheet*,* literature number SPRS082

- *TMS320C54x™ DSP Functional Overview,* literature number SPRU307

The five-volume *TMS320C54x DSP Reference Set,* literature number SPRU210, consisting of:

- *Volume 1: CPU and Peripherals,* literature number SPRU131

- *Volume 2: Mnemonic Instruction Set,* literature number SPRU172

- *Volume 3: Algebraic Instruction Set,* literature number SPRU179

- *Volume 4: Applications Guide,* literature number SPRU173

- *Volume 5: Enhanced Peripherals,* literature number SPRU302

The reference set describes in detail the TMS320C54x™ DSP products currently available and the hardware and software applications, including algorithms, for fixed-point TMS320™ DSP family of devices.

TMS320C54x, C54x, and TMS320 are trademarks of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265