

# AM64x Processor Silicon Revision 1.0



## ABSTRACT

This document describes the known exceptions to the functional specifications (advisories). This document may also contain usage notes. Usage notes describe situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness.

---

## Table of Contents

<b>1 Usage Notes and Advisories Matrices</b> .....	<b>2</b>
<b>2 Silicon Revision 1.0 Usage Notes and Advisories</b> .....	<b>3</b>
<b>Trademarks</b> .....	<b>5</b>
<b>Revision History</b> .....	<b>6</b>

## 1 Usage Notes and Advisories Matrices

[Table 1-1](#) lists all usage notes and the applicable silicon revision(s). [Table 1-2](#) lists all advisories, modules affected, and the applicable silicon revision(s).

**Table 1-1. Usage Notes Matrix**

ID	DESCRIPTION	SILICON REVISIONS AFFECTED
		AM64x
		1.0

**Table 1-2. Advisories Matrix**

MODULE	DESCRIPTION	SILICON REVISIONS AFFECTED
		AM64x
		1.0
ECC_AGGR	<a href="#">i2049</a> — ECC_AGGR: Potential IP Clockstop/Reset Sequence Hang due to Pending ECC Aggregator Interrupts	YES
RAT	<a href="#">i2062</a> — RAT: Error Interrupt Triggered Even When Error Logging Disable Is Set	YES
Internal Diagnostic Modules	<a href="#">i2103</a> — Incorrect Reporting of ECC_GRP, ECC_BIT and ECC_TYPE Information for Functional Safety Errors	YES

### 1.1 Devices Supported

This document supports the following devices:

- AM64x

Reference documents for the supported devices are:

- AM64x Processors Technical Reference Manual (SPRUIM3)
- AM64x Processors Datasheet (SPRSP56)

## 2 Silicon Revision 1.0 Usage Notes and Advisories

This section lists the usage notes and advisories for this silicon revision.

### 2.1 Silicon Revision 1.0 Usage Notes

No known usage notes for this silicon revision.

### 2.2 Silicon Revision 1.0 Advisories

#### **i2049** ***ECC\_AGGR: Potential IP Clockstop/Reset Sequence Hang due to Pending ECC Aggregator Interrupts***

---

**Details:** The ECC Aggregator module is used to aggregate safety error occurrences (which are rare) and generate interrupts to notify software. The ECC Aggregator provides software control over the enabling/disabling and clearing of safety errors interrupts.

When software is performing a clockstop/reset sequence on an IP, the sequence can potentially not complete because the IP's associated ECC Aggregator instance is not idle. The ECC Aggregator idle status is dependent upon any pending safety error interrupts either enabled or disabled, which have not been cleared by software. As a result, the IP's clockstop/reset sequence may never complete (hang) if there are any pending safety errors interrupts that remain uncleared.

**Workaround(s):** General Note:  
Clockstopping the ECC Aggregator is not supported in functional safety use-cases. Software should use the following workaround for non-functional safety use-cases:

1. Enable all ECC Aggregator interrupts for the IP
2. Service and clear all Pending interrupts
3. Step 3:
  - a. Disable all interrupt sources to the ECC Aggregator, followed by performing Clockstop/reset sequence.
  - b. Perform Clockstop/reset sequence, while continuing to service/clear pending interrupts.

Due to interrupts being external stimuli, software has two options for step 3:

1. Disable all interrupt sources (EDC CTRL checkers) that can generate pending ECC\_AGGR interrupts prior to performing the clockstop/reset sequence
2. Continue to service/clear pending interrupts that occur while performing the clkstop/reset sequence. The sequence would proceed when all interrupts are cleared.

Software in general may need to detect pending interrupts that continuously fire during this entire sequence (ex. in the case of a stuck-at fault scenario), and disable their associated EDC CTRL safety checkers to allow the clockstop/reset sequence to progress towards completion.

#### **i2062** ***RAT: Error Interrupt Triggered Even When Error Logging Disable Is Set***

---

**Details:** If the RAT error logging is programmed to disable logging and enable interrupts, then an error will incorrectly trigger an interrupt but the error log registers will correctly not be updated. The error interrupt should not have been generated.

**Workaround(s):** If the RAT error logging is disabled, then the error interrupt should also be disabled by software.

#### **i2103** ***Internal Diagnostics Modules: Incorrect Reporting of ECC\_GRP, ECC\_BIT and ECC\_TYPE Information for Functional Safety Errors***

---

- Details:** For functional safety errors, the logged information - ECC\_GRP, ECC\_BIT, and ECC\_TYPE in the Error Status Registers may be incorrect for certain safety checkers. This only applies to safety checkers that map to ECC\_GRP = 0,15,31,47,63...(N\*16-1). In the case for the DDR Bridge/Controller, the issue only applies to the safety checkers where ECC\_GRP = 0,31,63...(N\*32-1).
- This issue affects all Internal Diagnostics Module instances and their sub-banks.
- Note: The detection and interrupt signaling of these safety errors is unaffected. Only the logging of the aforementioned fields of the Error Status Registers are affected.
- Workaround(s):** None. For these specific safety checkers, software is limited to knowing whether a correctable or uncorrectable error occurred and which Internal Diagnostics Module instance had the error (thus knowing the IP module), but not which exact safety checker encountered the error.

## Trademarks

All trademarks are the property of their respective owners.

## Revision History

DATE	REVISION	NOTES
January 2021		Initial version

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated