

CC1050 Errata Note

The CC1050 Single-Chip Very Low Power RF Transmitter is described in the CC1050 Data Sheet. This document describes issues that may be encountered when using the part according to the above mentioned document. Where applicable, the relevant revisions of the CC1050, or the data sheet are specified.

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1 Known Issues

1.1 PLL unable to lock with certain frequency word combinations

Switching between certain combinations of frequency words (FREQ) in CC1050 may cause the PLL never to be able to lock. This is most likely to occur in frequency hopping systems. A software fix solves the problem.

1.1.1 Issue Description

When a new frequency is selected by updating the FREQ registers or changing the MAIN.F_REG bit, a non-valid value can be latched due to internal clock skew. This non-valid value may put the PLL in a deadlock situation and prevent the PLL from locking.

The deadlock situation can happen if the 3 most significant bits of the FREQ words are different for the two frequencies. If the 3 most significant bits are equal, the deadlock will not occur. To ensure that the most significant bits are equal, use the same reference frequency divider value (REFDIV) for all channels.

1.1.2 Suggested Workarounds

Alternative 1:

As the problem only rise when the MSBs of the FREQ words are different, the first solution is to select the same reference frequency divider value (REFDIV) for all channels. Using a crystal frequency of 14.7456 MHz or above make it possible to generate 50 channels with the same REFDIV value, see AN011.

Alternative 2:

If the three MSBs of the FREQ words cannot be made the same for all channels, a software workaround must be used.

Alternative 2a:

The general software workaround is to write a “safe” frequency value to the FREQ register before the new frequency is written. The “safe” frequency word is FREQ_2A (or FREQ_2B) = E0h. This workaround involves only one additional write operation: This is the suggestion for a software workaround:

1. Write FREQ_2A (register 01h) = E0h. (Presuming that frequency A is used.)
2. Write new frequency word to FREQ_A, or set MAIN.F_REG = 1 in order to swap the frequency word and use FREQ_B.

Alternative 2b:

An alternative software workaround is to reset the frequency synthesizer. After the new frequency word is programmed, the FS_RESET_N bit must be toggled by writing to the FSCTRL register, first setting the bit low, then high. This means two write operations to the register.

This is the suggestion for a software workaround:

1. Write new frequency word to `FREQ_A` or `FREQ_B`
2. First write `FSCTRL` (register 13h) = 00h
3. Then write `FSCTRL` (register 13h) = 01h

1.1.3 Fix

This problem is solved by a software workaround.

1.1.4 Batches affected

This errata note applies to all chip batches and revisions of the chip.

1.2 PLL not locking at low temperatures

Operating the CC1050 at supply voltage greater than 3.0 V and temperatures below 0°C may cause the frequency synthesizer PLL to fail if the register settings given by SmartRF Studio rev. 4.5 (or earlier) is used in the 433-MHz and 868-MHz frequency bands. In the 315 MHz band the register change applies across the CC1050 supply voltage range and data rates. Modifying the register settings for the prescaler solve the problem.

1.2.1 Issue Description

A combination of high supply voltage (> 3.0 V) and low temperature (< 0°C) may cause the prescaler in the frequency synthesizer to fail for some devices in the 433 MHz and 868 MHz frequency bands. The failure is due to a too large signal swing in the prescaler dividers. In the 315 MHz frequency band the signal swing needs to be increased from the default value stated in the data sheet for all supply voltages.

1.2.2 Suggested Workarounds

The suggested workaround is to change the register setting in the `PRESCALER.PRE_SWING[1:0]` from 00b to 01b in the 433 MHz and 868 MHz frequency bands. This will reduce the signal amplitude into the prescaler and ensure correct operation over the full operating range (2.1 to 3.6 V, -40 to +85°C). In the 315 MHz frequency band the suggested workaround is to change the register setting in the `PRESCALER.PRE_SWING[1:0]` from 00b to 10b.

1.2.3 Fix

Set the `PRESCALER` register (address 1Ch) to 40h for data rates up to 38.4 kBaud. Use 44h for data rates 38.4 and 76.8 kBaud as `DISCONNECT_C` = 1. This both applies to the 433 MHz and 868 MHz frequency bands. Set the `PRESCALER` register (address 1Ch) to 80h in the 315 MHz frequency band

1.2.4 Batches affected

This errata note applies to all CC1050 batches.

2 References

1. CC1050 Data sheet ([SWRS044](#))

3 Revision History

Revision	Date	Description
A	April 2014	Added changes to PRESCALER register at 315 MHz for the PLL not locking at low temperatures. Converted to TI format.

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