AWR1243 Device Errata Silicon Revisions 1.0, 2.0, and 3.0

1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (AWR1243).

2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / mmWave sensor devices. Each of the Radar devices has one of the two prefixes: X1x or AWR1x (for example: **AWR1243**FBIGABLRQ1). These prefixes represent evolutionary stages of product development from engineering prototypes (X1x) through fully qualified production devices (AWR1x).

Device development evolutionary flow:

X1x — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

AWR1x — Production version of the silicon die that is fully qualified.

X1x devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

3 Device Markings

Figure 1 shows an example of the AWR1243 Radar Device's package symbolization.

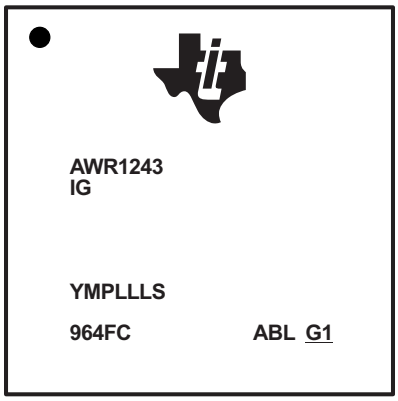

Figure 1. Example of Device Part Markings

This identifying number contains the following information:

- **Line 1:** Device Number
- **Line 2:** Temperature and Security Grade
- **Line 3:** Lot Trace Code
  - YM = Year/Month Code
  - PLLL = Assembly Lot
  - S = Assembly Site Code
- **Line 4:**
  - 964 = AWR1243 Identifier
  - F = ES3.0
  - D = ES2.0
  - BLANK = ES1.0
  - ABL = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

4 Advisory to Silicon Variant / Revision Map

Table 1. Advisory to Silicon Variant / Revision Map

Advisory Number	Advisory Title	AWR1243		
		ES1.0	ES2.0	ES3.0
Master Subsystem				
MSS#06	Internal Pulls on QSPI Data Lines not Enabled by the Device Bootloader	X	X	
MSS#18	Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application	X	X	
Analog / Millimeter Wave				
ANA#01	Noise Figure Degradation	X		
ANA#02	VCO#1 [76-77GHz] Minimum Frequency Falls Short of Target	X		
ANA#03	Spurs from LVDS Output Coupling into Synthesizer	X		
ANA#04	Receiver Gain Range Availability	X		
ANA#06	Return Loss Measurement on TX: S11 < –9dB, RX S11 < –6.5dB (Accepted Value of < –10dB)	X	X	
ANA#07	CSI2 Activity Coupling to Clock	X	X	
ANA#08	Doppler Spur Observed for Narrow Chirps Spanning 79.2 GHz	X	X	X
ANA#09	Synthesizer Frequency Nonlinearity at 76.8 GHz when Synthesizer (Chirp) Frequency Monitor Enabled	X	X	X
ANA#10	Unreliable Readings from Synthesizer Supply Voltage Monitor	X	X	X
ANA#11	TX, RX Gain Calibrations Sensitive to Large External Interference	X	X	X
ANA#12	Second Harmonic (HD2) is Present When Receiver is Tested Standalone Using CW Input	X	X	X
ANA#13	TX1 to TX3 Phase Mismatch Variation over Temperature is Double that of TX2/TX1 and TX3/TX2 Combinations	X	X	X

5 Known Design Exceptions to Functional Specifications

Table 2. Advisory List

MSS#06 *Internal Pulls on QSPI Data Lines not Enabled by the Device Bootloader*

Revision(s) Affected: AWR1243 ES1.0 and AWR1243 ES2.0

Description: Internal Pulls on the Data lines (D2 and D3) are not enabled by the device bootloader.

Workaround(s): Pulls on target board required (refer to reference schematics of TI EVM).

MSS#18 *Core Compare Module (CCM-R4F) may Cause nERROR Toggle After First Reset De-assertion Subsequent to Power Application*

Revision(s) Affected: AWR1243 ES1.0 and AWR1243 ES2.0

Description: The CCM-R4F module compares the outputs of the two Cortex-R4F CPU cores and generates an error on any mis-compare. This ensures the lock-step operation of the two Cortex-R4F CPUs. The nERROR signal should only be set by the CCM-R4 module by a valid core mismatch. At power-on, some uninitialized circuits may cause the CCMR4-F to falsely detect a mis-compare.

Workaround(s): The anomalous nERROR toggle would need to be ignored by the external monitoring circuit (if deployed).

ANA#01 *Noise Figure Degradation*

Revision(s) Affected: AWR1243 ES1.0

Description: Due to board limitation current typical Noise figure number is 18dB.

Workaround(s): None.

ANA#02 *VCO#1 [76-77GHz] Minimum Frequency Falls Short of Target*

Revision(s) Affected: AWR1243 ES1.0

Description: The supported frequency range is 77 GHz to 81 GHz (using VCO2).

Workaround(s): None.

ANA#03 *Spurs from LVDS Output Coupling into Synthesizer*

Revision(s) Affected: AWR1243 ES1.0

Description: For the characterization, the LVDS interface is used. In this mode, there is a package coupling to crystal oscillator pins causing spurs in LO (hence it comes out in IF spectrum).

Workaround(s): None.

ANA#04 *Receiver Gain Range Availability*

Revision(s) Affected: AWR1243 ES1.0

Description: The supported receiver gain range is 18dB (versus a specification target of 24dB).

Workaround(s): None.

ANA#06 *Return Loss Measurement on TX: S11 < –9dB, RX S11 < –6.5dB (Accepted Value of < –10dB)*

Revision(s) Affected: AWR1243 ES1.0 and AWR1243 ES2.0

Description: The return loss measurement on TX S11 is < –9dB and the return loss measurement on RX S11 is < –6.5dB. The accepted value is < –10dB.

Workaround(s): None.

ANA#07 *CSI2 Activity Coupling to Clock*

Revision(s) Affected: AWR1243 ES1.0 and AWR1243 ES2.0

Description: The activity on the CSI lines during the state transitions at the start and at the end of CSI transfer couples into the clock leading to glitches in the TX output.

Workaround(s): Increase the idle time between chirps such that the "start of transfer" and "end of transfer" occur during the idle time between two chirps.

1. The AWR1243 sends data from ADCBuffer to High Speed Peripheral. At the start of each chirp, CSI-2 changes from Low Power Mode to Standard Mode output. At the completion of the chirp, CSI-2 goes back from Standard mode to Low Power Mode output. When CSI-2 changes mode, there is a clock contamination of the ADC subsystem. In order to not contaminate the measurement, the CSI-2 data Output must be finished before the end of the idle time chirp parameter.

   Bitrate_perChirp_perLane = (numRxch * DFEoutrate * (numDFEsamples/chirp) * (complexmode+1) *(numbits/sample[12,14,16]) / (numLanes)

   perChirp_Outperiod = Bitrate_perChirp_perLane / (DDC_Clkrate * 2)

   IdleTime = MAX(Synthesizer_IdleTime, perChirp_Outperiod)

   Note: Synthesizer_IdleTime can be calculated in the mmWave Sensing Estimator.
2. If the customer uses the LVDS High Speed output format, this ADC clock disturbance is not seen.

ANA#08 *Doppler Spur Observed for Narrow Chirps Spanning 79.2 GHz*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: There is a nonlinearity of the synthesizer when crossing 79.2 GHz due to coupling from its reference to the VCO.

Implication: There is a spur in non-zero Doppler bin if the synthesizer crosses 79.2 GHz during a chirp. The exact Doppler bin depends on the slope of the ramp. This is not observed for wide bandwidth or higher ramp slopes.

Workaround(s): Avoid narrow, slow ramps near 79.2 GHz.

ANA#09 *Synthesizer Frequency Nonlinearity at 76.8 GHz when Synthesizer (Chirp) Frequency Monitor Enabled*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: When the synthesizer (chirp) frequency monitor is enabled and the synthesizer chirp reaches 76.8 GHz, the frequency error can be as high as 500 kHz due to coupling between the monitor and the synthesizer.

Implication: Increased nonlinearity in the chirp can lead to up to 20 dB degradation in the noise floor surrounding large objects, including the bumper reflection. This leads to potential loss of dynamic range when large and small objects are present simultaneously.

Workaround(s):

1. Disable the synthesizer frequency monitor during profiles where the LO crosses 76.8GHz.
2. Use non-functional chirps to detect nonlinearities in the synthesizer.

ANA#10 *Unreliable Readings from Synthesizer Supply Voltage Monitor*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: During monitoring, the thresholds used to determine if the synthesizer supply voltage is within limits are much stricter than necessary for proper circuit operation. This can lead to occasional, erroneous reporting of supply failures even when there is no adverse impact on circuit or system behavior.

Implication: The user cannot rely on supply failure indication from the supply monitors of PM, Clock and LO subsystems. The affected field is STATUS_SUPPLY_PMCLKLO in the monitoring report message: AWR_MONITOR_PMCLKLO_INTERNAL_ANALOG_SIGNALS_REPORT_AE_SB.

Workaround(s): Ignore the field STATUS_SUPPLY_PMCLKLO in the monitoring report message: AWR_MONITOR_PMCLKLO_INTERNAL_ANALOG_SIGNALS_REPORT_AE_SB.

1-dB Compression Point is –16dBm

ANA#11 *TX, RX Gain Calibrations Sensitive to Large External Interference*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: External interference present on the RX or TX pins with level >-10dBm can lead to degraded accuracy or errors in the peak detector, TX, and RX gain calibrations. If the interference changes its level while these calibrations are actively running, the calibration algorithm may interpret this as a change in signal power, leading to incorrect convergence. This applies to boot-time PD, TX, and RX calibrations, as well as run-time TX output power calibration.

Workaround(s): The incident power detector in the TX output power detector, along with the absolute level of the PA loopback used during the PA loopback monitors, are insensitive to this, and they can be used to check that the calibrations converged correctly. Calibration can be re-run if large interference was observed.

ANA#12 *Second Harmonic (HD2) is Present When Receiver is Tested Standalone Using CW Input*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: When the receiver is tested standalone using a CW input, a second harmonic (HD2) can be observed in the final ADC output at a level of –55 dBc.

Workaround(s): No workaround available at this time. However, in many typical radar use-cases the HD2 does not affect the system performance due to two reasons

1. Since the HD2 comes from a coupling to the LO signal, there is an inherent suppression of the HD2 level due to the self-mixing effect (i.e., phase noise and phase spur suppression effect at the mixer).
2. In real-life scenarios there is often a double-bounce effect of the radar signal reflected from the target, which leads to a ghost object at twice the distance of the actual object. This effect is often indistinguishable from the effect of HD2 itself.

ANA#13 *TX1 to TX3 Phase Mismatch Variation over Temperature is Double that of TX2/TX1 and TX3/TX2 Combinations*

Revision(s) Affected: AWR1243 ES1.0, AWR1243 ES2.0, and AWR1243 ES3.0

Description: TX3/TX1 combination exhibits a phase mismatch variation of ±6° from –40°C to 140°C whereas, TX2/TX1 and TX3/TX2 combinations exhibit a lower variation of ±3°C over the same temperature range.

Workaround(s): In applications requiring high phase accuracy across TX channels, a background angle calibration or a 2-point calibration can be used to control phase variation over temperature.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from December 31, 2018 to September 30, 2019 (from B Revision (December 2018) to C Revision) Page

- Figure 1 (Example of Device Part Markings: Updated/Changed figure "946FC" to "964FC" 2
- ANA#01: Updated/Changed Workaround 5
- ANA#02: Updated/Changed Workaround 5
- ANA#06: Added "Revision(s) Affected" and updated/changed "Workaround(s)", since bug issue fixed in ES3.0 6

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