Errata

AWR6843 Device Silicon Errata
Silicon Revision 2.0

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1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (AWR6843).

2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / mmWave sensor devices. Each of the Radar devices has one of the two prefixes: XAx or AWRx (for example: **XA6843**BGABL). These prefixes represent evolutionary stages of product development from engineering prototypes (XI) through fully qualified production devices (AWR).

Device development evolutionary flow:

XA —	Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
AWR —	Production version of the silicon die that is fully qualified.

XA devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

3 Device Markings

Figure 3-1 shows an example of the AWR6843 Radar Device's package symbolization.

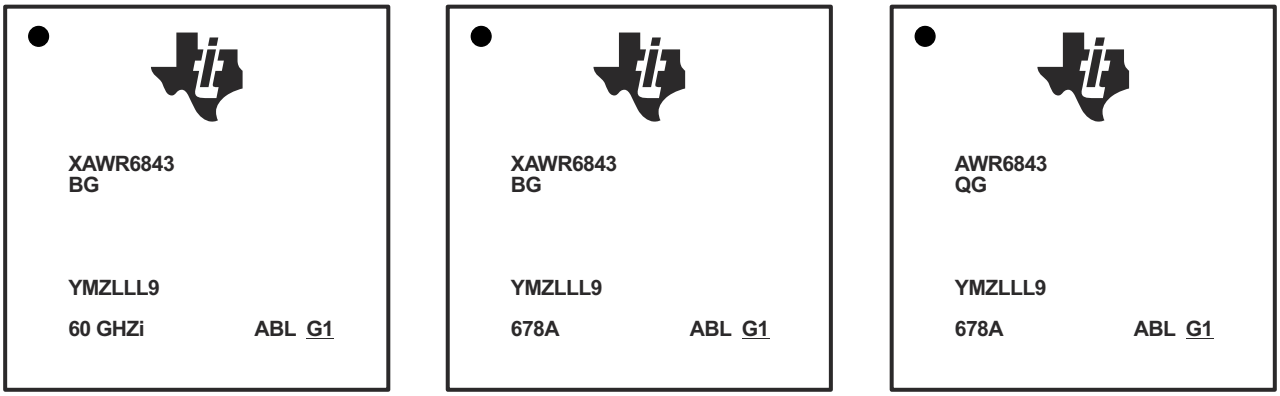

Figure 3-1. Example of Device Part Markings

This identifying number contains the following information:

- **Line 1:** Device Number
- **Line 2:** Safety Level and Security Grade
- **Line 3:** Lot Trace Code
  - –
  - YM = Year/Month Code
  - Z = Assembly Site Code
  - LLL = Assembly Lot Code
  - 9 = Primary Site Code
- **Line 4:**
  - 60 GHZi = AWR6843 (ES1.0) Identifier
  - 678A = AWR6843 (ES2.0) Identifier
  - ABL = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

4 Usage Notes

Usage notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These usage notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

4.1 MSS: SPI Speed in 3-Wire Mode Usage Note

The maximum SPI speed under 3-wire operation was only tested up to 33 MHz. This affects AWR6843 ES2.0.

5 Advisory to Silicon Variant / Revision Map

Table 5-1. Advisory to Silicon Variant / Revision Map

Advisory Number	Advisory Title	AWR6843 ES2.0
	Master Subsystem	
MSS#25	Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs	X
MSS#26	DMA Requests Lost During Suspend Mode	X
MSS#27	MibSPI in Slave Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1	X
MSS#28	A Data Length Error is Generated Repeatedly in Slave Mode When IO Loopback is Enabled	X
MSS#29	Spurious RX DMA REQ From a Slave Mode MibSPI	X
MSS#30	MibSPI RX RAM RXEMPTY Bit Does Not Get Cleared After Reading	X
MSS#31	CPU Abort Generated on a Write to Implemented CRC Space After a Write to Unimplemented CRC Space	X
MSS#32	DMMGLBCTRL BUSY Flag Not Set When DMM Starts Receiving A Packet	X
MSS#33	MibSPI RAM ECC is Not Read Correctly in DIAG Mode	X
MSS#34	HS Device Does Not Reboot Successfully on Warm Reset Getting Triggered by Watchdog Expiry	X
MSS#36	DMA Read From an Unimplemented Address Space is not Reported as a BUS Error	X
MSS#38	GPIO Glitch During Power-Up	X
MSS#39	DCC Module Frequency Comparison can Report Erroneous Results	X
	Analog / Millimeter Wave	
ANA#11	TX, RX Gain Calibrations Sensitive to Large External Interference	X
ANA#12	Second Harmonic (HD2) is Present When Receiver is Tested Standalone Using CW Input	X
ANA#13A	TX1 to TX3 Phase Mismatch Variation over Temperature is Double that of TX2/TX1 and TX3/TX2 Combinations	X
ANA#14	Doppler Spur Observed for Narrow Chirps Spanning 62.1 GHz	X
ANA#15	Excessive TX-RX Coupling or Reflection can Lead to Saturated RX Output	X
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ANA#19	Bandgap Decoupling Capacitor On-Board	X
ANA#20	Occasional Failures Observed During Calibration of the Radar Subsystem	X
ANA#21	Out of Band Radiated Spectral Emission	X
ANA#22	Overshoot and Undershoot During Inter-Chirp When Dynamic-Power Saving is Disabled	X

6 Known Design Exceptions to Functional Specifications

MSS#25	***Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs***
Revision(s) Affected:	AWR6843 ES2.0
Description:	If a system reset (nRST goes low) occurs while the debugger is performing an access on the system resource using system view, a slave error should be replied to the debugger. If the access was a read, instead the response might indicate that the access completed successfully and return unpredictable data. This issue occurs under this condition: when a system reset is asserted (nRST low) on a specific cycle, while the debugger is completing an access on the system, using the system view. An example would be, when a debugger, like the CCS-IDE memory browser window, is refreshing content using the system view. This is not an issue for a CPU only reset and, this is not an issue during a power-on-reset (nPORRST) either.
Workaround(s):	Avoid performing debug reads and writes while the device might be in reset.

MSS#26 ***DMA Requests Lost During Suspend Mode***

Revision(s) Affected: AWR6843 ES2.0

Description: While the device is halted in suspend mode by the debugger, the DMA is expected to complete the remaining transfers of a block, if the DEBUG MODE bit field of the GCTRL register is configured to '01'. Instead, the DMA does not complete the remaining transfers of a block but, rather stops after two more frames of data are transferred. Subsequent DMA requests from a peripheral to trigger the remaining frames of a block can be lost.

This issue occurs only in the following conditions:

- The device is suspended by a debugger
- A peripheral continues to generate requests while the device is suspended
- The DMA is setup to continue the current block transfer during suspend mode with the DEBUG MODE bit field of the GCTRL register set to '01'
- The request transfer type TTYPE bit in the CHCTRL registers is set to frame trigger ('0')

Workaround(s):

Workaround #1:

Use TTYPE = block transfer ('1'), when the DEBUG MODE bit field is '01' (*finish current block transfer*)

or

Workaround #2:

Use the DMA DEBUG MODE = '00' (ignore suspend), when using TTYPE = frame transfer ('0') to complete the block transfer, even after suspend/halt is asserted.

MSS#27	***MibSPI in Slave Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1***
Revision(s) Affected:	AWR6843 ES2.0
Description:	The MibSPI module, when configured in multibuffered slave mode with 3-functional pins (CLK, SIMO, SOMI) or 4-functional pins (CLK, SIMO, SOMI, nENA), could transmit incorrect data when all the following conditions are met: • MibSPI module is configured in multibuffered mode, • Module is configured to be a slave in the SPI communication, • SPI communication is configured to be in 3-pin mode or 4-pin mode with nENA, • Clock phase for SPICLK is 1, and • SPICLK frequency is MSS_VCLK frequency / 12 or slower
Workaround(s):	The issue can be avoided by setting the CSHOLD bit in the control field of the TX RAM (Multi-Buffer RAM Transmit Data Register). The nCS is not used as a functional signal in this communication; hence, setting the CSHOLD bit does not cause any other effect on the SPI communication.

MSS#28	***A Data Length Error is Generated Repeatedly in Slave Mode When IO Loopback is Enabled***
Revision(s) Affected:	AWR6843 ES2.0
Description:	When a DLEN error is created in Slave mode of the SPI using nSCS pins in IO Loopback Test mode, the SPI module re-transmits the data with the DLEN error instead of aborting the ongoing transfer and stopping. This is only an issue for an IOLPBK mode Slave in Analog Loopback configuration, when the intentional error generation feature is triggered using CTRLDLENERR (IOLPBKTSTCR.16).
Workaround(s):	After the DLEN_ERR interrupt is detected in IOLPBK mode, disable the transfers by clearing the SPIEN (bit 24) in the SPIGCR1 register and then, re-enable the transfers by resetting the SPIEN bit.

MSS#29	***Spurious RX DMA REQ From a Slave Mode MibSPI***
Revision(s) Affected:	AWR6843 ES2.0
Description:	A spurious DMA request could be generated even when the SPI slave is not transferring data in the following condition sequence: • The MIBSPI is configured in standard (non-multibuffered) SPI mode, as a slave • The DMAREQEN bit (SPIINT0.16) is set to enable DMA requests • The Chip Select (nSCS) pin is in an active state, but no transfers are active • The SPI is disabled by clearing the SPIEN (SPIGCR1.24) bit from '1' to '0' The above sequence triggers a false request pulse on the Receive DMA Request as soon as the SPIEN bit is cleared from '1' to '0'.
Workaround(s):	Whenever disabling the SPI, by clearing the SPIEN bit (SPIGCR1.24), first clear the DMAREQEN bit (SPIINT0.16) to '0', and then, clear the SPIEN bit.

MSS#30	***MibSPI RX RAM RXEMPTY bit Does Not Get Cleared After Reading***
Revision(s) Affected:	AWR6843 ES2.0
Description:	The RXEMPTY flag may not be auto-cleared after a CPU or DMA read when the following conditions are met: • The TXFULL flag of the latest buffer that the sequencer read out of transmit RAM for the currently active transfer group is 0, • A higher-priority transfer group interrupts the current transfer group and the sequencer starts to read the first buffer of the new transfer group from the transmit RAM, and • Simultaneously, the Host (CPU/DMA) is reading out a receive RAM location that contains valid received data from the previous transfers.
Workaround(s):	If at all possible, avoid transfer groups interrupting one another. If dummy buffers are used in lower-priority transfer groups, select the appropriate "BUFMODE" for them (like, SKIP/DISABLED) unless, there is a specific need to use the "SUSPEND" mode.

MSS#31	***CPU Abort Generated on a Write to Implemented CRC Space After a Write to Unimplemented CRC Space***
Revision(s) Affected:	AWR6843 ES2.0
Description:	An abort could be generated on a write to a legal address in the address offset region (0x0000–0x01FF) of the CRC register space when a normal mode write to an unimplemented address region (0x0200–0xFFFF) of the CRC register space is followed by a write to a legal address region (0x0000–0x01FF) of the CRC register space.
Workaround(s):	None.

MSS#32	***DMMGLBCTRL BUSY Flag Not Set When DMM Starts Receiving A Packet***
Revision(s) Affected:	AWR6843 ES2.0
Description:	The BUSY flag in the DMMGLBCTRL register should be set when the DMM starts receiving a packet or has data in its internal buffers. However, the BUSY flag (DMMGLBCTRL.24) may not get set when the DMM starts receiving a packet under the following condition: • The BUSY bit is set only after the packet has been received, de-serialized, and written to the internal buffers. It stays active while data is still in the DMM internal buffers. If the internal buffers are empty (meaning that no data needs to be written to the destination memory) then, the BUSY bit will be cleared.
Workaround(s):	Wait for a number of DMMCLK cycles (for example, 95 DMMCLK cycles) beyond the longest reception and deserialization time needed for a given packet size and DMM port configuration, before checking the status of the BUSY flag, and after the DMM ON/OFF bit field (DMMGLBCTRL.[3:0]) has been programmed to OFF.

MSS#33	*MibSPI RAM ECC is Not Read Correctly in DIAG Mode*
Revision(s) Affected:	AWR6843 ES2.0
Description:	A Read operation to the ECC address space of the MibSPI RAM in DIAG mode, does not return the correct ECC value for the first 128 buffers, if the Extended Buffer support is implemented but, the Extended Mode is disabled for the particular MibSPI instance.
Workaround(s):	None.

MSS#34	***HS Device Does Not Reboot Successfully on Warm Reset Getting Triggered or With Internal Software Reset***
Revision(s) Affected:	AWR6843 ES2.0
Description:	A warm reset triggered by a watchdog expiry (MSS Wdog) , a software register write (SOFTSYSRST), or an external warm reset pin does not ensure a successful reboot of the device in a secure device (HS device).
Workaround(s):	A warm reset should not be triggered externally or internally by a watchdog expiry, a software write, or other trigger mechanisms. To initiate a reset cycle, external circuitry should be used on the sensor design. The external circuitry uses the watchdog, nERROR OUT monitoring, or other kinds of GPIO signaling to trigger a reset using the nRST pin of the device.

MSS#36	***DMA Read From an Unimplemented Address Space is not Reported as a BUS Error***
Revision(s) Affected:	AWR6843 ES2.0
Description:	The MSS DMA should generate a Bus Error (BER) interrupt when the DMA detects an error due to a read from an unimplemented address location. This interrupt is not available on any of the VIM Interrupt Channels for DMA1 and DMA2. *Implication: A DMA read from an unimplemented address can go undetected.*
Workaround(s):	The DMA MPU has to be engaged with valid address range to ensure no occurrence of any read from an invalid address location happens. DMA transfers have to be covered with end-to-end CRC from source to destination.

MSS#38	*GPIO Glitch During Power-Up*
Revision(s) Affected:	AWR6843 ES2.0
Description:	During the 3.3-V supply ramp, the GPIO outputs could possibly see a short glitch (*rising above the 0 V for a short duration*). This GPIO glitch cannot be avoided by just a pulldown resistor. If the GPIO glitch during boot-up is high enough, it could be falsely detected as a “high”.
Workaround(s):	Any GPIO used for such critical controls where glitch cannot be tolerated, should be gated by the nRESET signal of the xWR device. Using a tri-state buffer (for example: SN74LVC1G126-Q1) externally to isolate the GPIO output from the system until the nRESET of xWR device is released. At this point, all the supplies are expected to be stable.

MSS#39	***DCC Module Frequency Comparison can Report Erroneous Results***
Revision(s) Affected:	AWR6843 ES2.0
Description:	The Dual-clock Comparator module, which is used to monitor a clock frequency while comparing with a known clock reference, could stop earlier than expected, and, thus, indicating the measured clock frequency to be lower. This is due to a clock domain crossing issue causing a preset to the error detection logic to get triggered.
Workaround(s):	Applicable for devices with monitoring support. Multiple measurements can be taken for the same clock pairs, and for the average, or majority of the frequencies reported. Application code, where possible, could compare the clocks using an alternate clock comparator module (CCC).

ANA#11	***TX, RX Gain Calibrations Sensitive to Large External Interference***
Revision(s) Affected:	AWR6843 ES2.0
Description:	External interference present on the RX or TX pins with level >-10dBm can lead to degraded accuracy or errors in the peak detector, TX, and RX gain calibrations. If the interference changes its level while these calibrations are actively running, the calibration algorithm may interpret this as a change in signal power, leading to incorrect convergence. This applies to boot-time PD, TX, and RX calibrations, as well as run-time TX output power calibration.
Workaround(s):	The incident power detector in the TX output power detector, along with the absolute level of the PA loopback used during the PA loopback monitors, are insensitive to this, and they can be used to check that the calibrations converged correctly. Calibration can be re-run if large interference was observed.

ANA#12	***Second Harmonic (HD2) is Present When Receiver is Tested Standalone Using CW Input***
Revision(s) Affected:	AWR6843 ES2.0
Description:	When the receiver is tested standalone using a CW input, a second harmonic (HD2) can be observed in the final ADC output at a level of –55 dBc.
Workaround(s):	No workaround available at this time. However, in many typical radar use-cases the HD2 does not affect the system performance due to two reasons 1. Since the HD2 comes from a coupling to the LO signal, there is an inherent suppression of the HD2 level due to the self-mixing effect (i.e., phase noise and phase spur suppression effect at the mixer). 2. In real-life scenarios there is often a double-bounce effect of the radar signal reflected from the target, which leads to a ghost object at twice the distance of the actual object. This effect is often indistinguishable from the effect of HD2 itself.

ANA#13A	***TX1 to TX3 Phase Mismatch Variation over Temperature is Double that of TX2/TX1 and TX3/TX2 Combinations***
Revision(s) Affected:	AWR6843 ES2.0
Description:	TX3/TX1 combination exhibits slightly a higher phase mismatch for temperature range –40°C to 105°C whereas, TX2/TX1 and TX3/TX2 combinations exhibit a lower variation of ±3°C over the same temperature range
Workaround(s):	In applications requiring high phase accuracy across TX channels, a background angle calibration or a 2-point calibration can be used to control phase variation over temperature.

ANA#14	***Doppler Spur Observed for Narrow Chirps Spanning 62.1 GHz***
Revision(s) Affected:	AWR6843 ES2.0
Description:	There is a non-linearity of the synthesizer when crossing 62.1 GHz due to coupling from its reference to the VCO. Implication: There is a spur in non-zero Doppler bin if the synthesizer crosses 62.1 GHz during a chirp. The exact Doppler bin depends on the slope of the ramp. This is not observed for wide bandwidth or higher ramp slopes
Workaround(s):	Avoid narrow, slow ramps near 62.1 GHz .

ANA#15	***Excessive TX-RX Coupling or Reflection can Lead to Saturated RX Output***
Revision(s) Affected:	AWR6843 ES2.0
Description:	If there is excessing TX-RX coupling or chassis reflection, it can lead to a saturated RX output. This situation can occur if the RX input is stronger than -15dBm at > 10kHz IF frequency.
Workaround(s):	Improve TX-to-RX antenna isolation on PCB. Radome/chassis should give low reflection amplitude and should be as close as possible to the sensor, to reduce the IF frequency.

ANA#16	*LVDS Coupling to Clock System*
Revision(s) Affected:	AWR6843 ES2.0
Description:	The digital activity in the High-Speed Serial Interfaces (HSI) state machine can couple to the clock system/FMCW synthesizer and can cause spurs in its clock output. The spur frequency is HSI rate dependent (for example, for a 600-MHz HSI clock rate, 6.25-MHz and 12.5-MHz spurs can be observed on TX/RX output, and for a 900-MHz HSI clock rate, 7-MHz and 14-MHz spurs can be observed on the TX/RX output). The spur levels are low (*near or below -65 dBc*).
Workaround(s):	The spur will not be present, when the LVDS is not used.

ANA#17	***On-Board Supply Ringing Induced Spur***
Revision(s) Affected:	AWR6843 ES2.0
Description:	Turning OFF and ON front-end modules can cause on-board supply ringing and slow the settling of the power supply. This supply ringing can manifest as a spur in the FMCW synthesizer output spectrum.
Workaround(s):	**Workaround #1:** Disable inter-chirp duty cycling of the RX. ***or*** **Workaround #2:** Design the power supply to damp out the ringing on the rails to the device.

ANA#18	*RX Digital Filtering Activity Coupling to XTAL Pins*
Revision(s) Affected:	AWR6843 ES2.0
Description:	The Digital filtering activity can potentially couple to XTAL pins and lead to spurs in the RX ADC output. The spur frequencies depend on the sampling rate (Fs) and DFE modes. Specifically, these spurs have been observed when Fs is close to 10- and 20-Msps within ±1.5 MHz. In these cases, an IF spur can appear at about 2Fs-40 MHz, 4Fs-40 MHz. The spur amplitudes vary with the frequency of the spur and are in the -35dBc range (for spur IF frequency of 200 kHz) to -75dBc range (for a spur IF frequency of 1.5 MHz) at the FMCW synthesizer output spectrum.
Workaround(s):	Avoid sampling rates of 10 ±1.5 Msps and 20 ±1.5 Msps. Exact 10-Msps and 20-Msps sampling rates are allowed, as they will not cause a spur.

ANA#19	***Bandgap Decoupling Capacitor On-Board***
Revision(s) Affected:	AWR6843 ES2.0
Description:	A 47-nF capacitor is needed on the bandgap pin. Not having correct capacitor on this pin, can cause boot up issues, especially, at negative temperatures. This requirement is being Included in the errata, as it is a recent change which may not be updated in older reference designs.
Workaround(s):	Use the recommended 47-nF capacitor. For example: part - GRM155R71E473KA88 (see the device-specific EVM and Reference Design files for updated part).

ANA#20	*Occasional Failures Observed During Calibration of the Radar Subsystem*
Revision(s) Affected:	AWR6843 ES2.0
Description:	Rare occurrences of failures have been observed in the Dual-Clock Comparator (DCC) module, as a result the APLL or Synthesizer may report a failure.
Workaround(s):	**Workaround #1:** Any APLL calibration failure needs to be responded with a reset cycle. ***or*** **Workaround #2:** Any SYNTH calibration failure reported by the BSS will require an RFinit.

ANA#21	***Out of Band Radiated Spectral Emission***
Revision(s) Affected:	AWR6843 ES2.0
Description:	14.4-GHz and 28.8-GHz frequency components on the radiated spectrum emissions, are out of band.
Workaround(s):	To help in reducing the spur, shield around the device (*excluding Antenna region*). Microwave absorbers are available and can be attached to the top of the device.

ANA#22	***Overshoot and Undershoot During Inter-Chirp When Dynamic-Power Saving is Disabled***
Revision(s) Affected:	AWR6843 ES2.0
Description:	This issue applies when Dynamic-Power Saving is disabled for Transmitters. Overshoot and Undershoot conditions cause narrower RF sweeping bandwidth. For a 500-MHz chirp bandwidth, there is MAX Overshoot of ~100 MHz, and a MAX Undershoot of ~100 MHz. This would lead to a significant reduction in effective chirp bandwidth for bandwidth-limited cases (for example, ISM band). For example: For an FMCW RF positive Ramp Chirp example, programmed for Fstart MHz to be (Fstart + 500) MHz, the effective observed transmission may span from (Fstart - 160) MHz to (Fstart + 500) MHz. Which would be an undershoot of 160 MHz. In order to compensate for such an undershoot, the programmed Chirps would have to be (Fstart + 160) MHz to (Fstart + 500) MHz. The net result is, the programmed Chirp would have to be for a reduced Bandwidth (that is, 340 MHz).
Workaround(s):	**Workaround #1:** A firmware resolution of 400 MHz is implemented in the accompanied SDK release (SDK version 3.4 or later). This allows the user to program up to 400 MHz of the available 500-MHz ISM band of 61 GHz to 61.5 GHz applications. ***or*** **Workaround #2:** To ensure the TX power amplifier is OFF during chirp idle time and not causing "on-air" emissions during the undershoot/overshoot period, keep the inter-chirp power savings ON.

7 Trademarks

All other trademarks are the property of their respective owners.

8 Revision History

Changes from April 30, 2020 to July 31, 2020 (from Revision * (April 2020) to Revision A (July 2020)) Page

- Global: Updated/Changed the numbering format for tables, figures, and cross-references throughout the document ... 2
- Changed / Updated Figure 3-1 ... 3
- (Advisory to Silicon Variant / Revision Map): Updated/Changed ANA#14, removed "58.4GHz and" as frequency is not supported in the device 5
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