Errata

AWR2944 Device Errata
Silicon Revisions 1.0

TEXAS INSTRUMENTS

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ADVANCE INFORMATION

1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (AWR2943, AWR2944).

Unless, otherwise noted, "AWR294x", when referenced, refers to both the AWR2943 and AWR2944 devices.

2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / milli-meter Wave sensor devices. Each of the Radar devices has one of the two prefixes: XAx or AWR2x (for example: **XA2943BGALT**). These prefixes represent evolutionary stages of product development from engineering prototypes (XAx) through fully qualified production devices (AWR2x).

Device development evolutionary flow:

XAx — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

AWR2x — Production version of the silicon die that is fully qualified.

XAx devices are shipped with the following disclaimer:

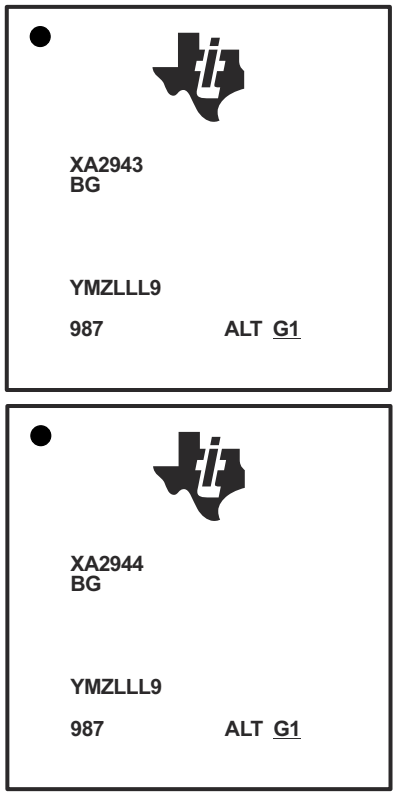
"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

3 Device Markings

Figure 3-1 shows an example of the AWR294x Radar Device's package symbolization.

Figure 3-1. Example of Device Part Markings



This identifying number contains the following information:

- **Line 1:** Device Number
- **Line 2:** Safety Level and Security Grade
- **Line 3:** Lot Trace Code
  - YM = Year/Month Date Code
  - Z = Secondary Site Code
  - LLL = Assembly Lot Code
  - 9 = Primary Site Code
- **Line 4:**
  - 987 = Device Identifier
  - ALT = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

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4 Advisory to Silicon Variant / Revision Map

Table 4-1. Advisory to Silicon Variant / Revision Map

ADVISORY NUMBER	ADVISORY TITLE	AWR294x ES1.0
MAIN SUBSYSTEM		
MSS#25	Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs	X
MSS#27	MibSPI in Peripheral Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1	X
MSS#28	A Data Length Error is Generated Repeatedly in Peripheral Mode When IO Loopback is Enabled	X
MSS#29	Spurious RX DMA REQ From a Peripheral Mode MibSPI	X
MSS#30	MibSPI RX RAM RXEMPTY Bit Does Not Get Cleared After Reading	X
MSS#33	MibSPI RAM ECC is Not Read Correctly in DIAG Mode	X
MSS#40	Any EDMA Transfer That Spans ACCEL_MEM1 +ACCEL_MEM2 Memories of Hardware Accelerator May Result In Data Corruption Without Any Notification Of Error From The SoC	X
MSS#46	Hardware Accelerator (HWA) Sniffers as a part of the Measurement Data output (MDO) interface are not operational.	X
MSS#48	Measurement Data Output (MDO) software marker inserted at FIFO threshold location other than for *Sniffer 0* is not sent out and is bound to get missed	X
MSS#49	Issues seen in potential interoperability with receiver supporting only Strict Alignment User Flow Control Stripping during Overflow message transmission in Aurora 64B/66B Protocol	X
ANALOG / MILLIMETER WAVE		
ANA#12A	Second Harmonic (HD2) Present in the Receiver	X
ANA#32	High inter-TX gain and phase mismatch drift over temperature	X
ANA#33	High inter-RX gain and phase mismatch drift over temperature	X
ANA#34	Low inter-TX isolation between adjacent channels (TX1/TX2 or TX3/TX4)	X
ANA#35	Low inter-RX isolation between adjacent channels (RX1/RX2 or RX3/RX4)	X
ANA#36	TX4 phase shifter DAC monitor and fault injection not functional	X
ANA#37	High RX gain droop across LO frequency	X
ANA#38	Return loss on RX pins not meeting the -10dB S11 target	X
ANA#39	HPF cutoff frequency 2800kHz configuration can result in incorrect RX IFA gains and filter corner frequencies	X

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5 Known Design Exceptions to Functional Specifications

MSS#25	***Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs***
Revision(s) Affected:	AWR294x ES1.0
Description:	If a system reset (nRST goes low) occurs while the debugger is performing an access on the system resource using system view, a peripheral error should be replied to the debugger. If the access was a read, instead the response might indicate that the access completed successfully and return unpredictable data. This issue occurs under this condition: when a system reset is asserted (nRST low) on a specific cycle, while the debugger is completing an access on the system, using the system view. An example would be, when a debugger, like the CCS-IDE memory browser window, is refreshing content using the system view. This is not an issue for a CPU only reset and, this is not an issue during a power-on-reset (nPORRST) either.
Workaround(s):	Avoid performing debug reads and writes while the device might be in reset.

MSS#27 ***MibSPI in Peipheral Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1***

Revision(s) Affected: AWR294x ES1.0

Description: The MibSPI module, when configured in multibuffered peripheral mode with 3-functional pins (CLK, SIMO, SOMI) or 4-functional pins (CLK, SIMO, SOMI, nENA), could transmit incorrect data when all the following conditions are met:

- MibSPI module is configured in multibuffered mode,
- Module is configured to be a peripheral in the SPI communication,
- SPI communication is configured to be in 3-pin mode or 4-pin mode with nENA,
- Clock phase for SPICLK is 1, and
- SPICLK frequency is MSS_VCLK frequency / 12 or slower

Workaround(s): The issue can be avoided by setting the CSHOLD bit in the control field of the TX RAM (Multi-Buffer RAM Transmit Data Register). The nCS is not used as a functional signal in this communication; hence, setting the CSHOLD bit does not cause any other effect on the SPI communication.

MSS#28	***A Data Length Error is Generated Repeatedly in Peripheral Mode When IO Loopback is Enabled***
Revision(s) Affected:	AWR294x ES1.0
Description:	When a DLEN error is created in Peripheral mode of the SPI using nSCS pins in IO Loopback Test mode, the SPI module re-transmits the data with the DLEN error instead of aborting the ongoing transfer and stopping. This is only an issue for an IOLPBK mode peripheral in Analog Loopback configuration, when the intentional error generation feature is triggered using CTRLDLENERR (IOLPBKTSTCR.16).
Workaround(s):	After the DLEN_ERR interrupt is detected in IOLPBK mode, disable the transfers by clearing the SPIEN (bit 24) in the SPIGCR1 register and then, re-enable the transfers by resetting the SPIEN bit.

MSS#29 ***Spurious RX DMA REQ From a Peripheral Mode MibSPI***

Revision(s) Affected: AWR294x ES1.0

Description: A spurious DMA request could be generated even when the SPI Peripheral is not transferring data in the following condition sequence:

- The MIBSPI is configured in standard (non-multibuffered) SPI mode, as a Peripheral
- The DMAREQEN bit (SPIINT0.16) is set to enable DMA requests
- The Chip Select (nSCS) pin is in an active state, but no transfers are active
- The SPI is disabled by clearing the SPIEN (SPIGCR1.24) bit from '1' to '0'

The above sequence triggers a false request pulse on the Receive DMA Request as soon as the SPIEN bit is cleared from '1' to '0'.

Workaround(s): Whenever disabling the SPI, by clearing the SPIEN bit (SPIGCR1.24), first clear the DMAREQEN bit (SPIINT0.16) to '0', and then, clear the SPIEN bit.

MSS#30	***MibSPI RX RAM RXEMPTY bit Does Not Get Cleared After Reading***
Revision(s) Affected:	AWR294x ES1.0
Description:	The RXEMPTY flag may not be auto-cleared after a CPU or DMA read when the following conditions are met: • The TXFULL flag of the latest buffer that the sequencer read out of transmit RAM for the currently active transfer group is 0, • A higher-priority transfer group interrupts the current transfer group and the sequencer starts to read the first buffer of the new transfer group from the transmit RAM, and • Simultaneously, the Host (CPU/DMA) is reading out a receive RAM location that contains valid received data from the previous transfers.
Workaround(s):	If at all possible, avoid transfer groups interrupting one another. If dummy buffers are used in lower-priority transfer groups, select the appropriate "BUFMODE" for them (like, SKIP/DISABLED) unless, there is a specific need to use the "SUSPEND" mode.

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MSS#33	*MibSPI RAM ECC is Not Read Correctly in DIAG Mode*
Revision(s) Affected:	AWR294x ES1.0
Description:	A Read operation to the ECC address space of the MibSPI RAM in DIAG mode does not return the correct ECC value for the first 128 buffers, if the Extended Buffer support is implemented, but the Extended Mode is disabled for the particular MibSPI instance.
Workaround(s):	None

MSS#40 ***Any EDMA Transfer That Spans ACCEL_MEM1 +ACCEL_MEM2 Memories of Hardware Accelerator May Result In Data Corruption Without Any Notification Of Error From The SoC***

Revision(s) Affected: AWR294x ES1.0

Description: As per TPTC IP Spec, a Transfer request (TR) is supposed to access a single peripheral end point. ACCEL_MEM0/ACCEL_MEM1 memory banks of HWA are available via single peripheral point and ACCEL_MEM2/ ACCEL_MEM3 memory banks of HWA are available as another peripheral point (different from that of ACCEL_MEM0/ ACCEL_MEM1). Hence if a single TR is used to access a buffer spanning ACCEL_MEM1 and ACCEL_MEM2 memories of the HWA (i.e. a single buffer spanning 2 different peripheral points), the spec is not being adhered to. This errata is explicitly highlighting this spec requirement.

Note

The ACCEL_MEM1 and ACCEL_MEM2 memories are referred to as DSS_HWA_DMA0 and DSS_HWA_DMA1 at the SoC level.

Workaround(s): Split the access into 2 TRs so that a single TR does not span ACCEL_MEM1 +ACCEL_MEM2. The 2 TRs can be chained.

MSS#46	***Hardware Accelerator (HWA) Sniffers as a part of the Measurement Data output (MDO) interface are not operational.***
Revisions Affected	AWR294x ES1.0
Details	Measurement Data Output (MDO) is used to capture the transactions on the bus connected from different interfaces of the AWR294x device and transmit outside over LVDS (4-data lanes). MDO is comprised of a sniffer, FIFO, and an aggregator. The MDO sniffer module is responsible for monitoring the hardware interfaces in the chip and capturing the transactions on the bus which are within the configured addressing region of interest. Hence, the sniffer module, as the name suggests, can sniff a bus interface and transfer contents to the MDO FIFO and aggregator. It can access the data from Radar Sub-System EDMA, L3 memory, DMA, local RAM, hardware accelerator etc. Currently, Hardware accelerator (HWA) sniffers for MDO interface are not operational.
Workaround	The required data to be sent out over the Aurora interface can be transferred out using the Generic DSS MDO FIFO (F2) using an EDMA to sequence the transfers.

MSS#48 ***Measurement Data Output (MDO) software marker inserted at FIFO threshold location other than for Sniffer 0 is not sent out and is bound to get missed.***

Revisions Affected AWR294x ES1.0

Details

Measurement Data Output (MDO) is used to capture the transactions on the bus connected from different interfaces of the AWR294x device and transmit outside over LVDS (4-data lanes). MDO is comprised of a sniffer, FIFO, and an aggregator. The corresponding sniffer module sniffs a bus interface and accumulates data in the FIFO. When a FIFO threshold is reached, the data is sent out to the aggregator as a burst transfer.

An MDO source can also inject a marker indicator along with its data for tracking or other related purpose. Now, if a marker is inserted such that it is a part of the last element of the FIFO threshold location, it is bound to get missed.

This happens only when a sniffer other than *Sniffer 0* is used for transfer.

Workaround

The following two workarounds can be used to ensure the inserted maker is registered without fail :

1. Multiple back to back markers (>1) can be sent out by the user to ensure atleast one of them is registered by the receiver.
2. The same sniffer configurations should be programmed to *Sniffer 0* registers. This way the markers would be sent out and registered by the receiver.
   This workaround is only beneficial where *Sniffer 0* is not in use and is idle for replicating other sniffer configurations.

Note

The above workarounds are only required when using markers in operation. There are no restrictions on the sniffers when markers are not in use.

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MSS#49 ***Issues seen in potential interoperability with receiver supporting only Strict Alignment User Flow Control Stripping during Overflow message transmission in Aurora 64B/66B Protocol.***

Revisions Affected AWR294x ES1.0

Details

Measurement Data Output (MDO) is used to capture the transactions on the bus connected from different interfaces of the AWR294x device and transmit outside over Aurora LVDS Interface (4-data lanes). MDO is comprised of a sniffer, FIFO, and an aggregator. The MDO sniffer module is responsible for monitoring the hardware interfaces in the chip and capturing the transactions on the bus which are within the configured addressing region of interest.

Data loss due to overflow can occur at the sniffer. This overflow information is sent as an interrupt to the CPU and the Aurora Tx IP. A User-Flow-Control (UFC) packet is generated by the Aurora TX IP in case of a data overflow condition in order to notify the user of this error condition. This is an error scenario and is not expected to occur in normal transfer functionality. At this stage, the data integrity is already compromised.

Aurora IP only supports UFC packet generation as per Section 6.6 of Aurora 64B/66B Protocol Specification, i.e. the UFC header block precedes the UFC data blocks. *Strict Alignment User Flow Control Stripping* (refer to Section 6.7 of Aurora 64B/66B Protocol Specification) is currently not supported.

Workaround

For MDO, the input data rate should be less than the output data rate so as to keep the effective data rate well within reasonable limits to avoid any overflow condition altogether.

Note

It is inadvisable for Aurora 64B/66B protocol to use *TOP_AURORA_TX:AURORA_TX_UFC_MSG_REQ* register to send UFC packets without overflow.

ANA#12A	*Second Harmonic (HD2) Present in the Receiver*
Revision(s) Affected:	AWR294xES1.0
Description:	There is a finite isolation between the RF pins/package and the FMCW synthesizer. This can create spurious tones at the synthesizer output and lead to appearance of 2nd order harmonics and inter-modulations of expected IF frequencies at RX ADC output. The amplitude of the 2nd harmonic could as high as -30 dBc, referenced to the power level of the intended tone at the LNA input.
Workaround(s):	No workaround available at this time. However, in many typical radar usecases the HD2 does not affect the system performance due to two reasons: 1. Since the HD2 comes from a coupling to the LO signal, there is an inherent suppression of the HD2 level due to the self-mixing effect (that is, phase noise and phase spur suppression effect at the mixer). 2. In real-life scenarios there is often a double-bounce effect of the radar signal reflected from the target, which leads to a ghost object at twice the distance of the actual object. This effect is often indistinguishable from the effect of HD2 itself.

ANA#32	*High inter-TX gain and phase mismatch drift over temperature*
Revisions Affected	AWR294x ES1.0
Details	TX4/TX1 or TX4/TX2 combination exhibits upto +/-9 degree variation in phase mismatch over the full allowed temperature range.
Workaround	In applications where high gain/phase accuracy is desired between TX channels, a background calibration can be used to correct for mismatch variation over temperature.

ANA#33	***High inter-RX gain and phase mismatch drift over temperature***
Revisions Affected	AWR294x ES1.0
Details	RX4 and RX3 exhibit +/-6 degree phase mismatch variation over the full allowed temperature range with respect to RX1.
Workaround	In applications where high gain/phase accuracy is desired between RX channels, a background calibration can be used to correct for mismatch variation over temperature.

ANA#34	***Low inter-TX isolation between adjacent channels (TX1/TX2 or TX3/TX4)***
Revisions Affected	AWR294x ES1.0
Details	TX1/TX2 and TX3/TX4 pairs exhibit low inter-channel isolation (22dB).
Workaround	No workaround is available. If the isolation is limiting the angular accuracy, zero angle calibration can be extended to multiple angles to calibrate the antenna gain & phase mismatch in order to improve the angular accuracy.

ANA#35	***Low inter-RX isolation between adjacent channels (RX1/RX2 or RX3/RX4)***
Revisions Affected	AWR294x ES1.0
Details	RX1/RX2 and RX3/RX4 pairs exhibit low interchannel isolation (23dB).
Workaround	No workaround is available. If the isolation is limiting the angular accuracy, zero angle calibration can be extended to multiple angles to calibrate the antenna gain & phase mismatch in order to improve the angular accuracy.

ANA#36	*TX4 phase shifter DAC monitor and fault injection are not functional*
Revisions Affected	AWR294x ES1.0
Details	TX4 phase shifter DAC (Digital to Analog Conversion) monitor is not functional due to a design bug in the Silicon. Similarly, the assosicated fault injection mechanism is also not functional on Silicon.
Workaround	No Workaround is available. TX gain/phase mismatch monitor and phase shifter monitor are available as additional diagnostics that can cover the TX-DAC from a safety perspective.

ANA#37	*High RX gain droop across LO frequency*
Revisions Affected	AWR294x ES1.0
Details	RX gain droop is ~6dB across the full operating frequency range of the device. Absolute gain at 81GHz can be ~5dB lower than the programmed gain.
Workaround	Negligible impact on system performance since there is an insignificant impact on noise figure due to the gain droop.

ANA#38	***Return loss on RX pins not meeting the -10dB S11 target***
Revisions Affected	AWR294x ES1.0
Details	Measured input match (S11) at RX input pins on the PCB is ~-4dB at 81GHz.
Workaround	No workaround is available. The noise figure number measured includes the degraded S11 on the Rx ports.

ANA#39	***HPF cutoff frequency 2800kHz configuration can result in incorrect RX IFA gains and filter corner frequencies.***
Revisions Affected	AWR294x ES1.0
Details	The analog IF stages include a second order high pass filter that can be configured to the following -6dB corner frequencies : 300, 350, 700, 1400, 2800 KHz. Out of these, HPF cutoff frequency 2800kHz configuration can result in incorrect RX IFA gains and filter corner frequencies.
Workaround	Use of 2800kHz cutoff configuration is not recommended.

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Revision History

DATE	REVISION	NOTES
November 2021	*	APL Release

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265