Functional Safety Information

ADS8353-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for ADS8353-Q1 (TSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

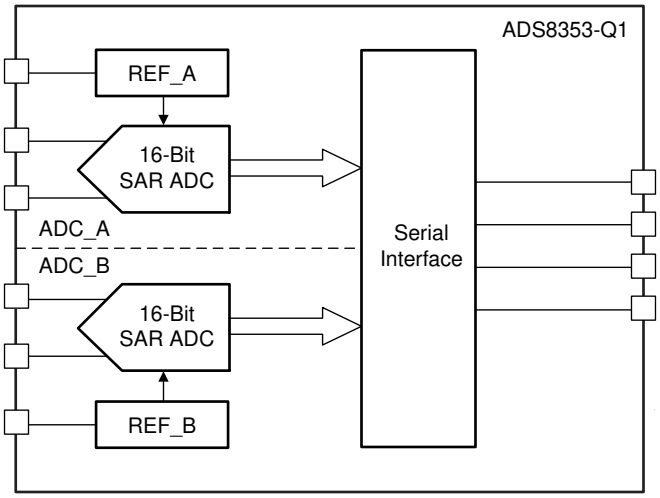

Figure 1-1. Functional Block Diagram

ADS8353-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for ADS8353-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	11
Die FIT Rate	2
Package FIT Rate	9

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 55 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ADS8353-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
ADC_A offset error out of specification	10%
ADC_B offset error out of specification	10%
ADC_A gain error out of specification	10%
ADC_B gain error out of specification	10%
REF_A output out of specification	5%
REF_B output out of specification	5%
10x input leakage current on analog inputs	5%
ADC_A and ADC_B conversions not synchronized	5%
ADC_A or ADC_B output code bit error	20%
Communication error	20%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ADS8353-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the ADS8353-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ADS8353-Q1 data sheet.

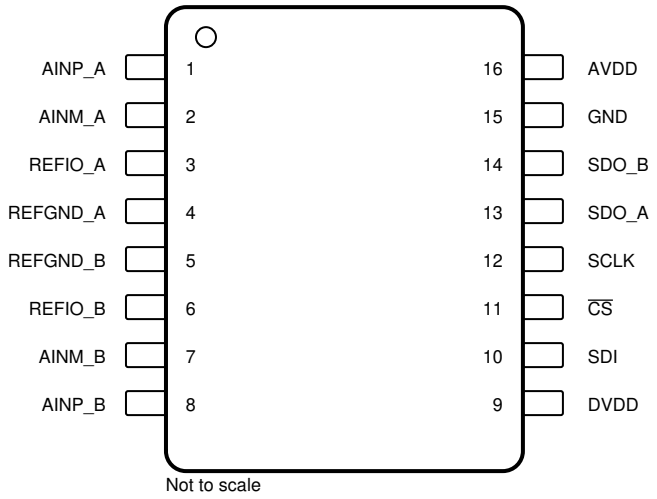

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- AVDD and DVDD use the same supply voltage.
- REFGND_A, REFGND_B and GND use the same GND.
- Short circuit to Power means short to AVDD = DVDD.
- Short circuit to GND means short to REFGND_A = REFGND_B = GND.
- RC filters on every analog input, AINP_x and AINM_x. Series resistors are sized to limit the input currents into the analog inputs to <10mA in all circumstances, e.g. also in case device is unpowered and input signal is applied.
- Device is the only peripheral on the SPI bus.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AINP_A	1	Single-ended configuration: ADC_A conversion result close to 0 V.	B
		Pseudo-differential configuration: ADC_A conversion result close to negative full-scale.	B
AINM_A	2	Single-ended configuration: No effect. Normal operation.	D
		Pseudo-differential configuration: Incorrect ADC_A conversion result. Incorrect voltage on AINM_A.	B
REFIO_A	3	ADC_A conversion result undetermined. ADC_A reference voltage is 0 V (REFGND_A = REFIO_A).	B
REFGND_A	4	No effect. Normal operation.	D
REFGND_B	5	No effect. Normal operation.	D
REFIO_B	6	ADC_B conversion result undetermined. ADC_B reference voltage is 0 V (REFGND_B = REFIO_B).	B
AINM_B	7	Single-ended configuration: Normal operation.	D
		Pseudo-differential configuration: Incorrect ADC_B conversion result. Incorrect voltage on AINM_B.	B
AINP_B	8	Single-ended configuration: ADC_B conversion result close to 0 V.	B
		Pseudo-differential configuration: ADC_B conversion result close to negative full-scale.	B
DVDD	9	Digital interface not powered up. No SPI communication with device possible. Observe that the absolute maximum ratings for all digital pins of the device are met, otherwise device damage may be plausible.	A
SDI	10	SDI stuck low. Normal operation in default power-up configuration. Device configuration cannot be changed.	B
$\overline{CS}$	11	$\overline{CS}$ stuck low. No SPI communication with device possible. Conversions cannot be initiated.	B
SCLK	12	SCLK stuck low. No SPI communication with device possible.	B
SDO_A	13	SDO_A stuck low. ADC_A conversion result or device internal registers cannot be read. Increase in supply current when SDO_A tries to drive high. Device damage plausible if SDO_A drives high for extended period of time.	A
SDO_B	14	32-CLK, dual-SDO mode: SDO_B stuck low. ADC_B conversion results cannot be read. Increase in supply current when SDO_B tries to drive high. Device damage plausible if SDO_B drives high for extended period of time.	A
		32-CLK, single-SDO mode: No effect. Normal operation.	D
GND	15	No effect. Normal operation.	D
AVDD	16	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AINP_A	1	ADC_A conversion result undetermined.	B
AINM_A	2	ADC_A conversion result undetermined.	B
REFIO_A	3	ADC_A reference voltage undetermined. ADC_A conversion result undetermined.	B
REFGND_A	4	Increased gain error for ADC_A. ADC_A reference voltage will connect to ground through internal path in the device. Increased gain error for ADC_A due to reference voltage drop across the internal path in the device.	B
REFGND_B	5	Increased gain error for ADC_B. ADC_B reference voltage will connect to ground through internal path in the device. Increased gain error for ADC_B due to reference voltage drop across the internal path in the device.	B
REFIO_B	6	ADC_B reference voltage undetermined. ADC_B conversion result undetermined.	B
AINM_B	7	ADC_B conversion result undetermined.	B
AINP_B	8	ADC_B conversion result undetermined.	B
DVDD	9	Digital interface not powered up if all external digital pins are held low. No SPI communication with device possible. Digital interface may power up through internal ESD diodes to DVDD if voltages above the device's power-on reset threshold are present on any of the digital pins.	B
SDI	10	State of SDI input undetermined. SPI communication to the device corrupted. Device configuration cannot be changed. Normal operation in default power-up configuration.	B
$\overline{CS}$	11	State of $\overline{CS}$ input undetermined. SPI communication corrupted.	B
SCLK	12	State of SCLK input undetermined. SPI communication corrupted.	B
SDO_A	13	ADC_A conversion result or device internal registers cannot be read.	B
SDO_B	14	32-CLK, dual-SDO mode: ADC_B conversion results cannot be read.	B
		32-CLK, single-SDO mode: No effect. Normal operation.	D
GND	15	Device functionality undetermined. Device may connect to ground internally through alternate pin ESD diode and power up.	B
AVDD	16	Device functionality undetermined. Device unpowered and not functional if all external analog pins are held low. Device may power up through internal ESD diodes to AVDD if voltages above the device's power-on reset threshold are present on any of the analog pins.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
AINP_A	1	AINM_A	Differential ADC_A input voltage is 0 V. ADC_A conversion result close to 0 V.	B
AINM_A	2	REFIO_A	Single-ended configuration: Incorrect voltage on AINM_A. Incorrect ADC_A conversion result.	B
			Pseudo-differential configuration, V_{REF} range: Incorrect ADC_A conversion result.	B
			Pseudo-differential configuration, 2x V_{REF} range: No effect. Normal operation.	D
REFIO_A	3	REFGND_A	ADC_A reference voltage is 0 V (REFGND_A = REFIO_A). ADC_A conversion result undetermined.	B
REFGND_A	4	REFGND_B	No effect. Normal operation.	D
REFGND_B	5	REFIO_B	ADC_B reference voltage is 0 V (REFGND_B = REFIO_B). ADC_B conversion result undetermined.	B
REFIO_B	6	AINM_B	Single-ended configuration: Incorrect voltage on AINM_B. Incorrect ADC_B conversion result.	B
			Pseudo-differential configuration, V_{REF} range: Incorrect ADC_B conversion result.	B
			Pseudo-differential configuration, 2x V_{REF} range: No effect. Normal operation.	D
AINM_B	7	AINP_B	Differential ADC_B input voltage is 0 V. ADC_B conversion result close to 0 V.	B
AINP_B	8	-	Not considered. Corner pin.	-
DVDD	9	SDI	SDI stuck high. Normal operation in default power-up configuration. Device configuration cannot be changed.	B
SDI	10	$\overline{CS}$	SPI communication corrupted. No SPI communication with the device possible.	B
$\overline{CS}$	11	SCLK	SPI communication corrupted. No SPI communication with the device possible.	B
SCLK	12	SDO_A	SPI communication corrupted. Increase in supply current when SCLK tries to drive high while SDO_A tries to drive low and vice versa. Device damage may be plausible.	A
SDO_A	13	SDO_B	SPI communication corrupted. Increase in supply current when SDO_B tries to drive high while SDO_A tries to drive low and vice versa. Device damage may be plausible.	A
SDO_B	14	GND	32-CLK, dual-SDO mode: SDO_B stuck low. ADC_B conversion results cannot be read. Increase in supply current when SDO_B tries to drive high. Device damage plausible if SDO_B drives high for extended period of time.	A
			32-CLK, single-SDO mode: No effect. Normal operation.	D
GND	15	AVDD	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AVDD	16	-	Not considered. Corner pin.	-

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AINP_A	1	ADC_A conversion result close to positive full-scale code.	B
AINM_A	2	Incorrect ADC_A conversion result. Incorrect voltage on AINM_A.	B
REFIO_A	3	Increased gain error because reference to ADC_A is different from the intended REFIO_A voltage.	B
REFGND_A	4	Incorrect ADC_A reference voltage. Incorrect ADC_A conversion result.	B
REFGND_B	5	Incorrect ADC_B reference voltage. Incorrect ADC_B conversion result.	B
REFIO_B	6	Increased gain error because reference to ADC_B is different from the intended REFIO_B voltage.	B
AINM_B	7	Incorrect ADC_B conversion result. Incorrect voltage on AINM_B.	B
AINP_B	8	ADC_B conversion result close to positive full-scale code.	B
DVDD	9	No effect. Normal operation.	D
SDI	10	SDI stuck high. Normal operation in default power-up configuration. Device configuration cannot be changed.	B
$\overline{CS}$	11	$\overline{CS}$ stuck high. No SPI communication with device possible. Conversions cannot be initiated.	B
SCLK	12	SCLK stuck high. No SPI communication with device possible.	B
SDO_A	13	SDO_A stuck high. ADC_A conversion result or device internal registers cannot be read. Increase in supply current when SDO_A tries to drive low. Device damage plausible if SDO_A drives low for extended period of time.	A
SDO_B	14	32-CLK, dual-SDO mode: SDO_B stuck high. ADC_B conversion results cannot be read. Increase in supply current when SDO_B tries to drive low. Device damage plausible if SDO_B drives low for extended period of time.	A
		32-CLK, single-SDO mode: No effect. Normal operation.	D
GND	15	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AVDD	16	No effect. Normal operation.	D

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