INA226-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for INA226-Q1 (VSSOP-10 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

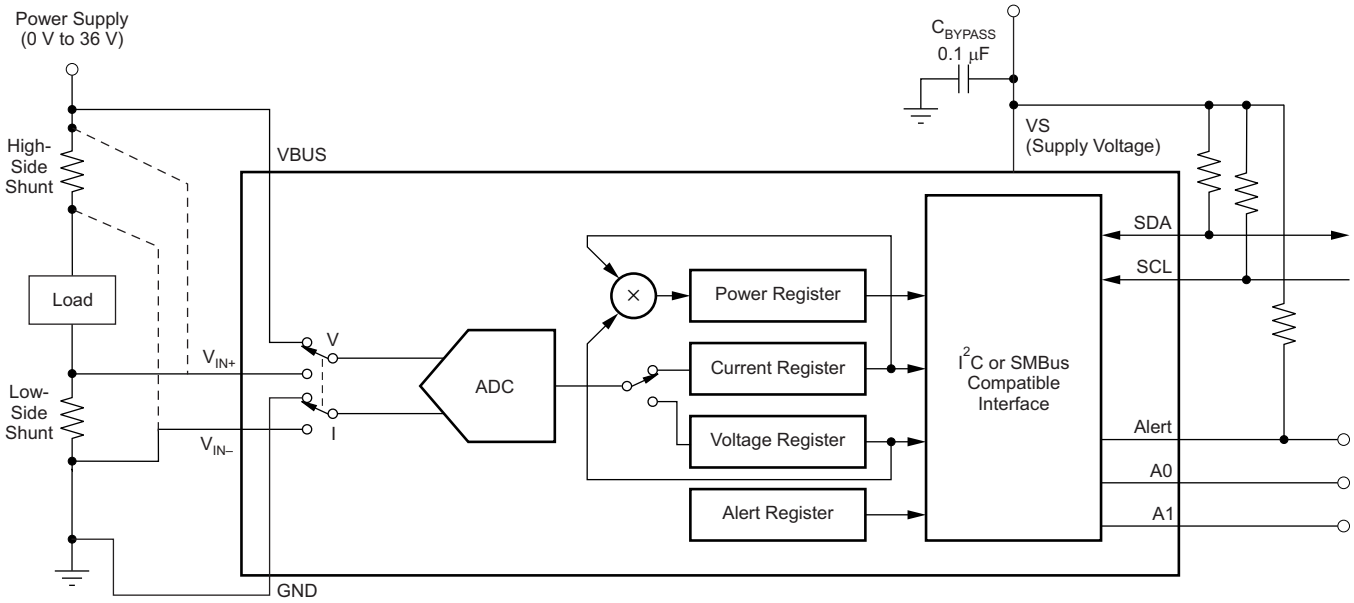

Figure 1. Functional Block Diagram

INA226-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for INA226-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	8
Die FIT Rate	3
Package FIT Rate	5

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA226-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
ADC output bit error	20%
ADC gain out of specification	20%
ADC offset out of specification	20%
Communication error	15%
Register bit error	10%
ADC MUX select error	5%
ALERT - false trip or failure to trip	5%
Pin to pin short, any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA226-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin open-circuited (see Table 6)
- Pin short-circuited to an adjacent pin (see Table 7)
- Pin short-circuited to VS (see Table 8)

Table 5 through Table 8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 2 shows the INA226-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the INA226-Q1 datasheet.

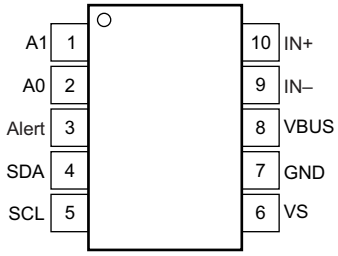

Figure 2. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 2.7 V to 5.5 V
- V_{BUS} = 12 V
- Device is the only slave on the I^2C bus

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A1	1	Power supply shorted to GND if A1 initially connected to VS. Slave address will change if A1 was not initially grounded.	B
A0	2	Power supply shorted to GND if A0 initially connected to VS. Slave address will change if A0 was not initially grounded.	B
ALERT	3	Alert pin cannot be pulled high and thus alerts cannot be detected by host.	C
SDA	4	Will halt the digital communication.	B
SCL	5	Will halt the digital communication.	B
VS	6	Power supply shorted to GND and device turned off.	B
GND	7	Normal operation.	D
VBUS	8	Cannot measure bus voltage. A short from the bus supply to GND will occur. High current will flow from bus supply through VBUS trace and to GND. Shunt/trace/bus voltage source could be damaged.	B
IN-	9	Corrupts (saturates or shorts) the input sense voltage unless IN- is already connected to GND. If high-side application, then bus voltage source is shorted to GND and potentially damaged due to high-current. If low-side and IN+ is initially connected to bus GND, then sense voltage becomes zero.	B. Only D if low-side sensing positive V_{SENSE}.
IN+	10	Corrupts (saturate or shorts) the input sense voltage unless IN+ is already connected to GND. If high-side application, then bus voltage source is shorted to GND and potentially damaged due to high-current. If low-side and IN- is initially connected to bus GND, then sense voltage becomes zero.	B. Only D if low-side sensing negative V_{SENSE}.

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A1	1	Changes the device's slave address if A1 not already floating.	C
A0	2	Changes the device's slave address if A0 not already floating.	C
ALERT	3	ALERT cannot be pulled high and alerts cannot be detected by host.	C
SDA	4	Will halt digital communication.	B
SCL	5	Will halt digital communication.	B
VS	6	No power to the device. Device may be partially biased through inputs. No damage to the device.	B
GND	7	No power to the device.	B
VBUS	8	Cannot measure the bus voltage and thus cannot calculate power.	C
IN-	9	Cannot measure sense voltage.	B
IN+	10	Cannot measure sense voltage.	B

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
A1	1	2 - A0	Can change the device's slave address if A1 is not already same as A0.	C
A0	2	3 - ALERT	Can halt the alert response if A0 is tied to GND, or change slave address if ALERT is pulled high and A0 is initially floating	C
ALERT	3	4 - SDA	Will halt digital communication as long as ALERT pin is active LOW. ALERT can be pulled low by SDA.	B
SDA	4	5 - SCL	Will halt digital communication.	B
SCL	5	6 - VS	Will short out the SCL pull-up resistor and halt digital communication.	B
VS	6	7 - GND	Power supply shorted to GND and device turned off.	B
GND	7	8 - VBUS	Cannot measure bus voltage. A short from the bus supply to GND will occur. High current will flow from bus supply through VBUS trace and to GND. Shunt/trace/bus voltage source could be damaged.	B
VBUS	8	9 - IN-	This could create a short in parallel with the shunt resistor, which would affect sense voltage. Could potentially cause the short/trace connecting VBUS to IN- to burn up from high bus currents.	B
IN-	9	10 - IN+	This would short out the shunt resistance and make input voltage 0-V. Could potentially cause the short/trace connecting IN+ to IN- to burn up from high bus currents.	B
IN+	10	1 - A1	A1 is a digital input pin and can be damaged if shorted to voltage greater than 6 V. For high-side application, shorting IN+ and A1 can damage pin if IN+ common-mode voltage is greater than 6 V. For a low-side application, this will change slave address if A1 not already connected to GND.	A

Table 8. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A1	1	Changes the device's slave address if A1 not already tied to VS.	C
A0	2	Changes the device's slave address if A0 not already tied to VS.	C
ALERT	3	Will short out the ALERT pull-up resistor. If ALERT was to activate (active LOW), then only the internal transistor's resistance would limit the I_{OL} current into ALERT. According to Absolute Maximum Ratings, if I_{OL} > 10 mA (which is likely with no pull-up resistance), then this could damage the internal transistor/device. This increase in IOL current could also increase the V_{OL} (low-level output voltage) of ALERT pin as well during an alert event.	A
SDA	4	Will short out the SDA pull-up resistor and halt digital communication. If SDA is driven low by INA226-Q1 (slave), then device damage could occur if I_{OL} > 10 mA, which is likely with no pull-up resistance. This increase in I_{OL} current would likely also increase the V_{OL} (low-level output voltage) of SDA.	A
SCL	5	Will short out the SCL pull-up resistor and halt digital communication.	B
VS	6	Normal operation.	D
GND	7	Power supply shorted to GND and device turned off.	B
VBUS	8	Bus voltage source shorted to VS rail. if VS is driven to voltage > 6V, will damage the INA226-Q1.	A
IN-	9	For high-side applications, this would short bus source to VS rail. If VS is driven to voltage > 6 V, then this could damage INA226-Q1. For low-side applications, this won't cause device damage, but might cause the VS supply to short to GND causing a sharp rise in current through the shunt and/or device to turn off.	A
IN+	10	For high-side applications, this would short bus source to VS rail. If VS is driven to voltage > 6 V, then this could damage INA226-Q1. For low-side applications, this won't cause device damage, but might cause the VS supply to short to GND causing a sharp rise in current through the shunt and/or device to turn off.	A

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2020) to A Revision	Page
• Changed to latest report format, including FIT Rate, FMD, and Pin FMA	1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265