INA186-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for INA186-Q1 (DCK-6 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

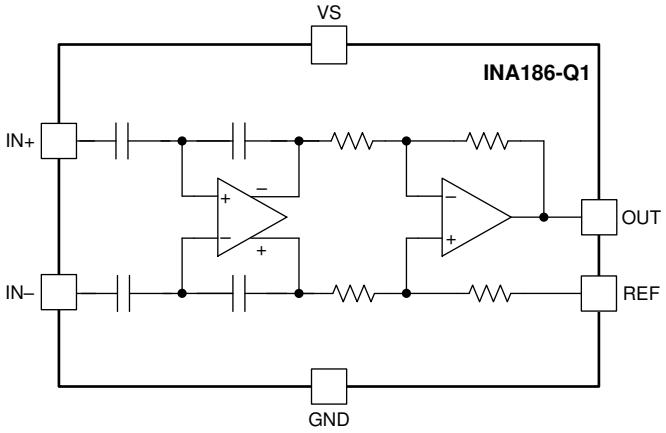

Figure 1. Functional Block Diagram

INA186-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for INA186-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 25 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	CMOS Op amp, comparators, voltage monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA186-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT open (Hi-Z)	10%
OUT to GND	20%
OUT to VS	15%
OUT functional, not in specification	50%
Pin to pin short, any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA186-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin open-circuited (see Table 6)
- Pin short-circuited to an adjacent pin (see Table 7)
- Pin short-circuited to VS (see Table 8)

Table 5 through Table 8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 2 shows the INA186-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the INA186-Q1 datasheet.

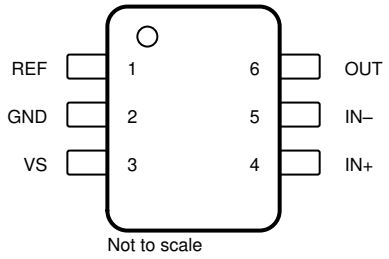

Figure 2. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 1.8 V to 5.0 V
- V_{IN+} = 12 V
- $V_{REF} = V_S / 2$

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
REF	1	Normal operation if REF pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF=GND by design; C otherwise
GND	2	Normal operation.	D
VS	3	Power supply shorted to GND.	B
IN+	4	In high-side configuration, a short from the bus supply to GND will occur.	B
IN-	5	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
OUT	6	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, which could cause die junction temperature to exceed 150°C.	B

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
REF	1	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
GND	2	When GND is floating, output will be incorrect as it is no longer referenced to GND.	B
VS	3	No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.	B
IN+	4	Shunt resistor is not connected to amplifier. IN+ pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN-	5	Shunt resistor is not connected to amplifier. IN- pin may float to an unknown value. Output will go to an unknown value not to exceed Vs or GND.	B
OUT	6	Output can be left open. There is no effect on the IC, but the output will not be measured.	C

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
REF	1	2 - GND	Normal operation if REF pin is at GND potential by design, otherwise the system measurement will be incorrect.	D if REF=GND by design; C otherwise
GND	2	3 - VS	Power supply shorted to GND.	B
VS	3	4 - IN+	In high-side configuration, VS may be subjected to high voltage bus supply. In low side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN+	4	5 - IN-	Inputs shorted together, so no sense voltage applied. Output will track REF voltage.	B
IN-	5	6 - OUT	In high-side configuration, OUT pin may be subjected to high voltage bus supply. In low side configuration, OUT is shorted to GND, device will not be damaged, but functionality will be affected.	A for high-side; B for low-side
OUT	6	1 - REF	Output will be pulled to REF voltage and output current may be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B

Table 8. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
REF	1	Normal operation if REF pin is at VS potential by design; otherwise the system measurement will be incorrect.	D if REF=VS by design; C otherwise
GND	2	Power supply shorted to GND.	B
VS	3	Normal operation.	D
IN+	4	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN-	5	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
OUT	6	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B

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