Application Report

OPA2365-Q1
Functional Safety FIT Rate and Pin FMA

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1 Overview

This document contains information for OPA2365-Q1 (SOIC-8 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Pin failure mode analysis (Pin FMA)

OPA2365-Q1 shows the device functional block diagram for reference.

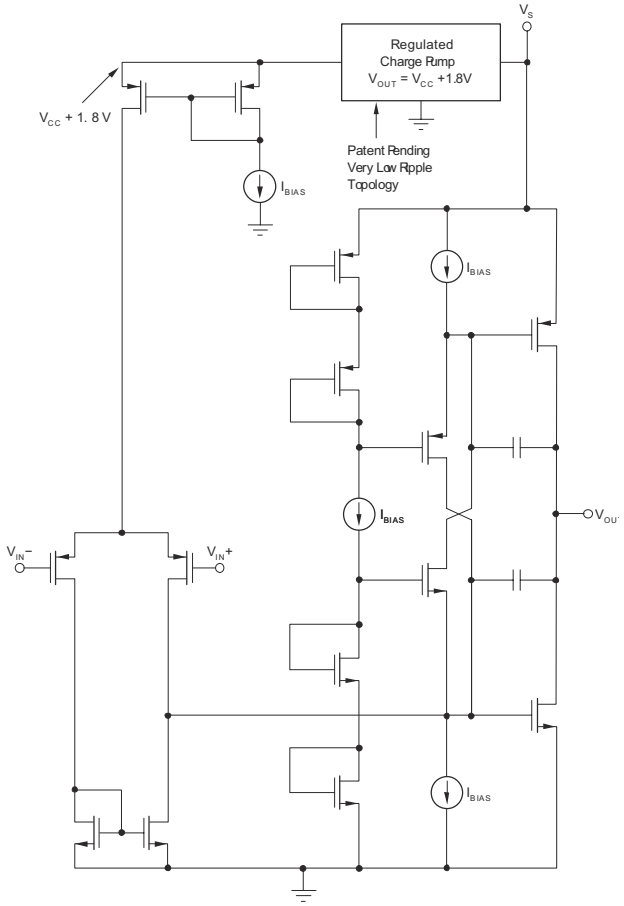

Figure 1-1. Functional Block Diagram

OPA2365-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for OPA2365-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	10
Die FIT Rate	3
Package FIT Rate	7

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 120 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Bipolar Op Amp, Comparators, Voltage Monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the OPA2365-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 3-2)
- Pin open-circuited (see Table 3-3)
- Pin short-circuited to an adjacent pin (see Table 3-4)
- Pin short-circuited to V+ (see Table 3-5)

Table 3-2 through Table 3-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 3-1.

Table 3-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 3-1 shows the OPA2365-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the OPA2365-Q1 data sheet.

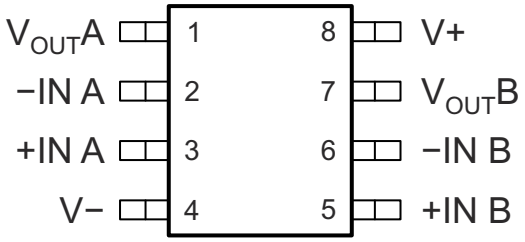

Figure 3-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Total supply voltage of 5 V with V+ connected to 5V and V- connected to ground
- Input and output pins biased to 2.5 V reference point
- Device is configured with feedback network in gain greater than or equal to 1 V/V

Table 3-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1	VOUTA	May cause device to overheat.	B
2	-IN A	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
3	+IN A	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
4	V-	Normal operation, unless dual supply voltage was intended.	D
5	+IN B	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
6	-IN B	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
7	VOUTB	May cause device to overheat.	B
8	V+	Diodes from input to V+ may turn on due to input signal and cause electrical overstress (EOS).	A

Table 3-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1	VOUTA	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
2	-IN A	Floating input, circuit will likely not function as expected.	C
3	+IN A	Floating input, circuit will likely not function as expected.	C
4	V-	Lowest voltage pin will try to power the device's V- pin.	B
5	+IN B	Floating input, circuit will likely not function as expected.	C
6	-IN B	Floating input, circuit will likely not function as expected.	C
7	VOUTB	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
8	V+	Highest voltage output pin will try to power internal V+	B

Table 3-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
1	VOUTA	-IN A	Channel 1 configured in unity gain	C
2	-IN A	+IN A	No damage to device. Application circuit will not work.	C
3	+IN A	V-	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
4	V-	+IN B	Input at V- (GND) is valid input, however, desired application result is unlikely. Pins are not adjacent to each other.	C
5	+IN B	-IN B	No damage to device. Application circuit will not work	C
6	-IN B	VOUTB	Channel 1 configured in unity gain	C
7	VOUTB	V+	May cause device to overheat.	B
8	V+	VOUTA	May cause device to overheat. Pins are not adjacent to each other.	B

Table 3-5. Pin FMA for Device Pins Short-Circuited to VS+

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1	VOUTA	May cause device to overheat.	B
2	-IN A	Input at V+ is a valid input, however, desired application result is unlikely.	C
3	+IN A	Input at V+ is a valid input, however, desired application result is unlikely.	C
4	V-	Diodes from input to V- may turn on due to input signal and cause electrical overstress (EOS).	A
5	+IN B	Input at V+ is a valid input, however, desired application result is unlikely.	C
6	-IN B	Input at V+ (GND) is a valid input, however, desired application result is unlikely.	C
7	VOUTB	May cause device to overheat.	B
8	V+	Normal Operation.	D

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