Functional Safety Information

INA333-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for INA333-Q1 (VSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

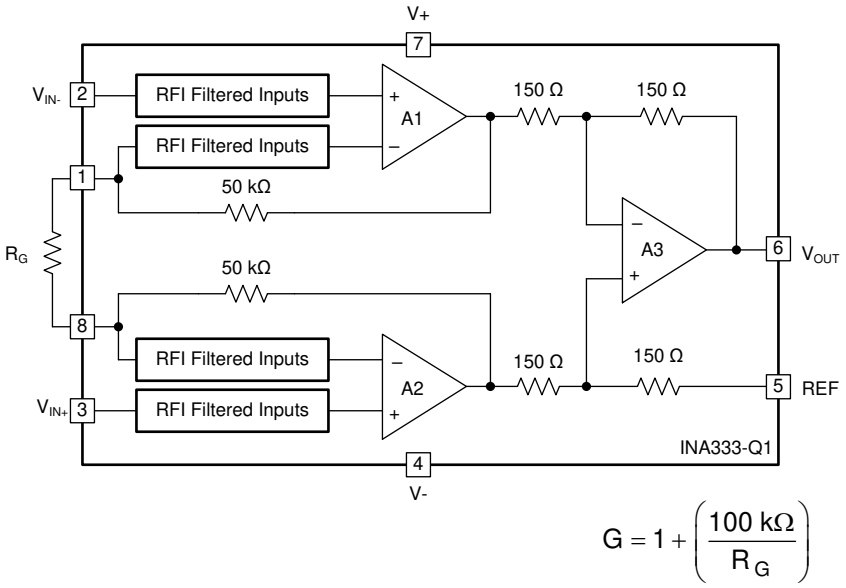

Figure 1-1. Functional Block Diagram

INA333-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for INA333-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	2
Package FIT Rate	3

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 28 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA333-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	20%
Output saturated high	25%
Output saturated low	25%
Output functional, out of specification voltage or timing	30%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA333-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the INA333-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA333-Q1 data sheet.

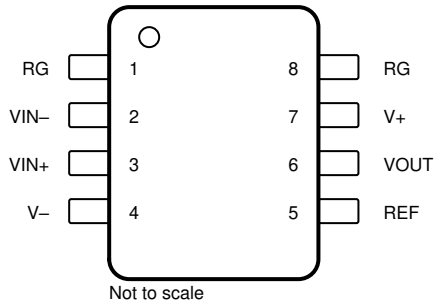

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- 'Short circuit to Power' means short to V+
- 'Short circuit to GND or Ground' means short to V–
- V+ is equivalent to VCC and V– equivalent to VEE

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RG	1	The device does not receive negative feedback internally causing a loss of functionality.	B
VIN–	2	Inverting pin is shorted to supply, likely resulting in a device output voltage between the negative and positive rails.	B
VIN+	3	Noninverting pin is shorted to supply, likely resulting in a device output voltage between the negative and positive rails.	C
REF	5	Depending on the circuit configuration, the output most likely moves to the negative supply.	B
VOUT	6	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the VOUT voltage ultimately forced to the V– voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A
V+	7	INA supplies are shorted together, leaving the V+ pin at some voltage between the V+ and V– sources (depending on the source impedance).	A
RG	8	The device does not receive negative feedback internally causing a loss of functionality.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RG	1	Gain is set to 1 based on gain equation: G = 1 + (100 kΩ / RG).	B
VIN–	2	Inverting pin of the INA is left floating. The VIN– pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes, likely resulting in a device output voltage between the negative and positive rails.	B
VIN+	3	Noninverting pin of the INA is left floating. The VIN+ pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes, likely resulting in a device output voltage between the negative and positive rails.	B
V–	4	Negative supply is left floating. The INA ceases to function because no current can source or sink to the device.	A
REF	5	Loss of functionality due to floating DC bias of output amplifier potentially causing shift in output voltage.	B
VOUT	6	Loss of device ability for VOUT to drive the application.	A
RG	8	Gain is set to 1 based on gain equation: G = 1 + (100 kΩ / RG)	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
RG	1	2	The device does not receive negative feedback internally causing a loss of functionality.	B
VIN–	2	3	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
VIN+	3	4	Noninverting pin is tied to the negative rail. Depending on the circuit configuration, the device output voltage will likely land between the negative and positive rails	C
V–	4	5	Depending on the circuit configuration, the output most likely moves to the negative supply.	B
REF	5	6	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the VOUT voltage ultimately forced to the REF voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A
VOUT	6	7	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the VOUT voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A
V+	7	8	The device does not receive negative feedback internally causing a loss of functionality.	B
RG	8	1	Gain is not set and device loses functionality. Prolonged exposure to these conditions will not cause device damage.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RG	1	The device does not receive negative feedback internally causing a loss of functionality.	B
VIN–	2	Inverting pin is shorted to supply, likely resulting in a device output voltage between the negative and positive rails.	B
VIN+	3	Noninverting pin is shorted to supply, likely resulting in a device output voltage between the negative and positive rails.	B
V–	4	INA supplies are shorted together, leaving the V– pin at some voltage between the V– and V+ sources (depending on the source impedance).	A
REf	5	Depending on the circuit configuration, the output most likely moves to the positive supply.	B
VOUT	6	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the VOUT voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A
RG	8	The device does not receive negative feedback internally causing a loss of functionality.	B

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