Functional Safety Information

TLV733P-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TLV733P-Q1 (WSON-6 and SOT-23-5 packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

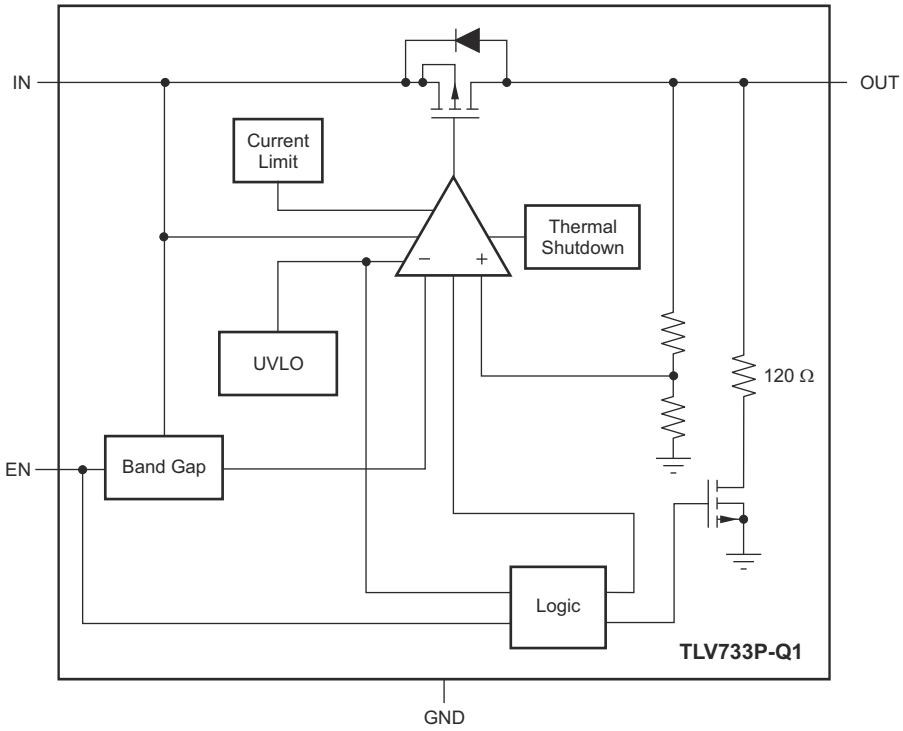

Figure 1-1. Functional Block Diagram

TLV733P-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 WSON-6 Package

This section provides Functional Safety Failure In Time (FIT) rates for the WSON-6 package of TLV733P-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 125 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power Amplifier and Regulator ≤ 1 Watt (LDO)	40 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 SOT-23-5 Package

This section provides Functional Safety Failure In Time (FIT) rates for the SOT-23-5 package of TLV733P-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	5
Package FIT Rate	2

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 125 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power Amplifier and Regulator ≤ 1 Watt (LDO)	40 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLV733P-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No OUTPUT (output low)	50%
OUTPUT High (following input)	10%
OUTPUT not in specification	35%
Short circuit, any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLV733P-Q1 (WSON-6 and SOT-23-5 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (seeTable 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to V_{IN} (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_J = -40°C to +150°C
- T_A = -40°C to +125°C
- V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater)
- I_{OUT} = 1 mA
- V_{EN} = V_{IN}
- C_{IN} = C_{OUT} = 1 µF

4.1 WSON-6 Package

Figure 4-1 shows the TLV733P-Q1 pin diagram for the WSON-6 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TLV733P-Q1 data sheet.

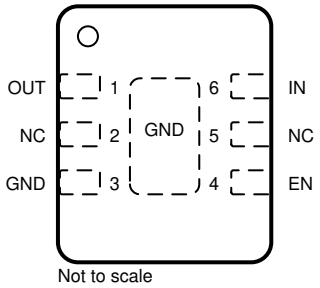

Figure 4-1. Pin Diagram (WSON-6) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output voltage will be near/at ground. Device is in current limit. It may cycle in and out of thermal shutdown depending on power dissipation.	B
NC	2	Normal operation.	D
GND	3	Normal operation.	D
EN	4	LDO will not start up due to EN being grounded.	B
NC	5	Normal operation.	D
IN	6	Output voltage will be near/at ground.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	No impact to the LDO, but components downstream will not be powered.	D
NC	2	Normal operation.	D
GND	3	GND is floating. Output voltage will be incorrect as it is no longer referenced to GND.	B
EN	4	EN pin voltage will float as the LDO contains no internal pullup/pulldown. LDO is in unknown state.	B
NC	5	Normal operation.	D
IN	6	No input to LDO. Input and output will float to an unknown voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	2 - NC	Normal operation.	D
NC	2	3 - GND	Normal operation.	D
GND	3	4 - EN	LDO will not start up due to EN being grounded.	B
EN	4	5 - NC	Normal operation.	D
NC	5	6 - IN	Normal operation.	D
IN	6	1 - OUT	No output voltage regulation. Output voltage is the same as input voltage.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{IN}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	No output voltage regulation. Output voltage is the same as input voltage.	B
NC	2	Normal operation.	D
GND	3	Output voltage will be near/at ground.	B
EN	4	LDO will startup/shutdown when V_{IN} is above EN threshold.	D if $V_{IN} = V_{EN}$ by design, B otherwise
NC	5	Normal operation.	D
IN	6	Normal operation.	D

4.2 SOT-23-5 Package

Figure 4-2 shows the TLV733P-Q1 pin diagram for the SOT-23-5 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TLV733P-Q1 data sheet.

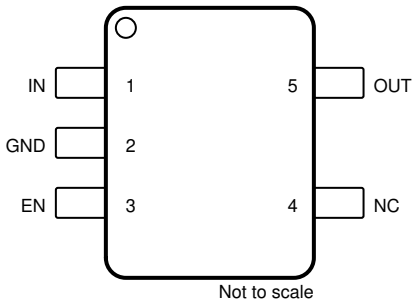

Figure 4-2. Pin Diagram (SOT-23-5 Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	Output voltage will be near/at ground.	B
GND	2	Normal operation.	D
EN	3	LDO will not start up due to EN being grounded.	B
NC	4	Normal operation.	D
OUT	5	Output voltage will be near/at ground. Device is in current limit. It may cycle in and out of thermal shutdown depending on power dissipation.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	No input to LDO. Input and output will float to an unknown voltage.	B
GND	2	GND is floating. Output voltage will be incorrect as it is no longer referenced to GND.	B
EN	3	EN pin voltage will float as LDO contains no internal pullup/pulldown. LDO is in unknown state.	B
NC	4	Normal operation.	D
OUT	5	No impact to the LDO, but components downstream will not be powered.	D

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	2 - GND	Output voltage will be near/at ground.	B
GND	2	3 - EN	LDO will not start up due to EN being grounded.	B
EN	3	4 - NC	Normal operation.	D
NC	4	5 - OUT	Normal operation.	D
OUT	5	1 - IN	No output voltage regulation. Output voltage is the same as input voltage.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to V_{IN}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	Normal operation.	D
GND	2	Output voltage will be near/at ground.	B
EN	3	LDO will startup/shutdown when V_{IN} is above EN threshold.	D if $V_{IN} = V_{EN}$ by design, B otherwise
NC	4	Normal operation.	D
OUT	5	No output voltage regulation. Output voltage is the same as input voltage.	B

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265