Functional Safety Information

TPS1HB50-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS1HB50-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

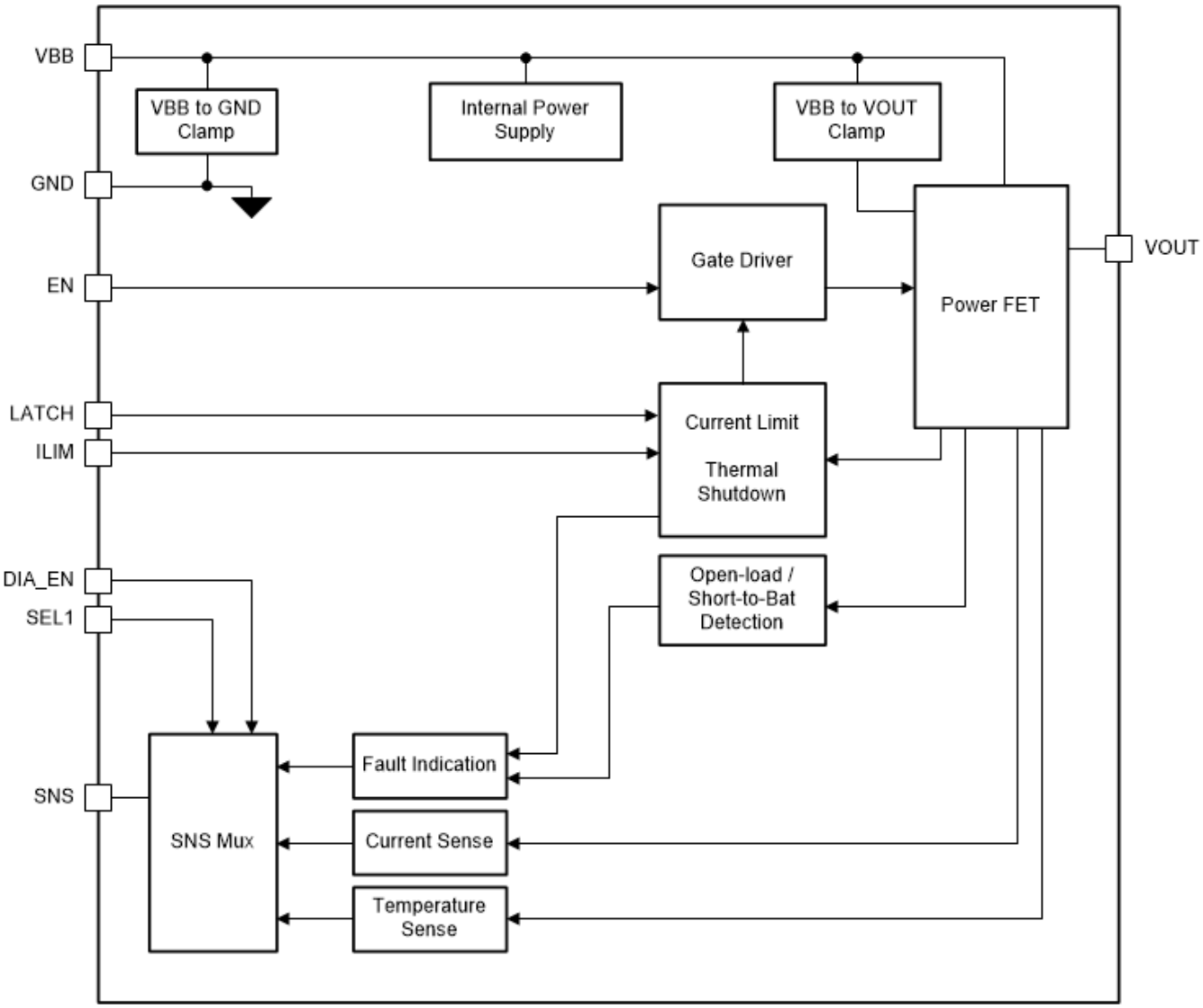

Figure 1-1. Functional Block Diagram

TPS1HB50-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS1HB50-Q1 based on industry-wide used reliability standard:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	22
Die FIT Rate	12
Package FIT Rate	10

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 750 mW
- Climate type: World-wide Table 8 IEC TR 62380
- Package factor (lambda 3): Table 17b IEC TR 62380
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS1HB50-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (HiZ)	20%
VOUT stuck on (VBB)	10%
VOUT functional, not in specification voltage or timing	45%
Diagnostics not in specification	10%
Protect functions fails to trip	10%
Pin to Pin short any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS1HB50-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS1HB50-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS1HB50-Q1 data sheet.

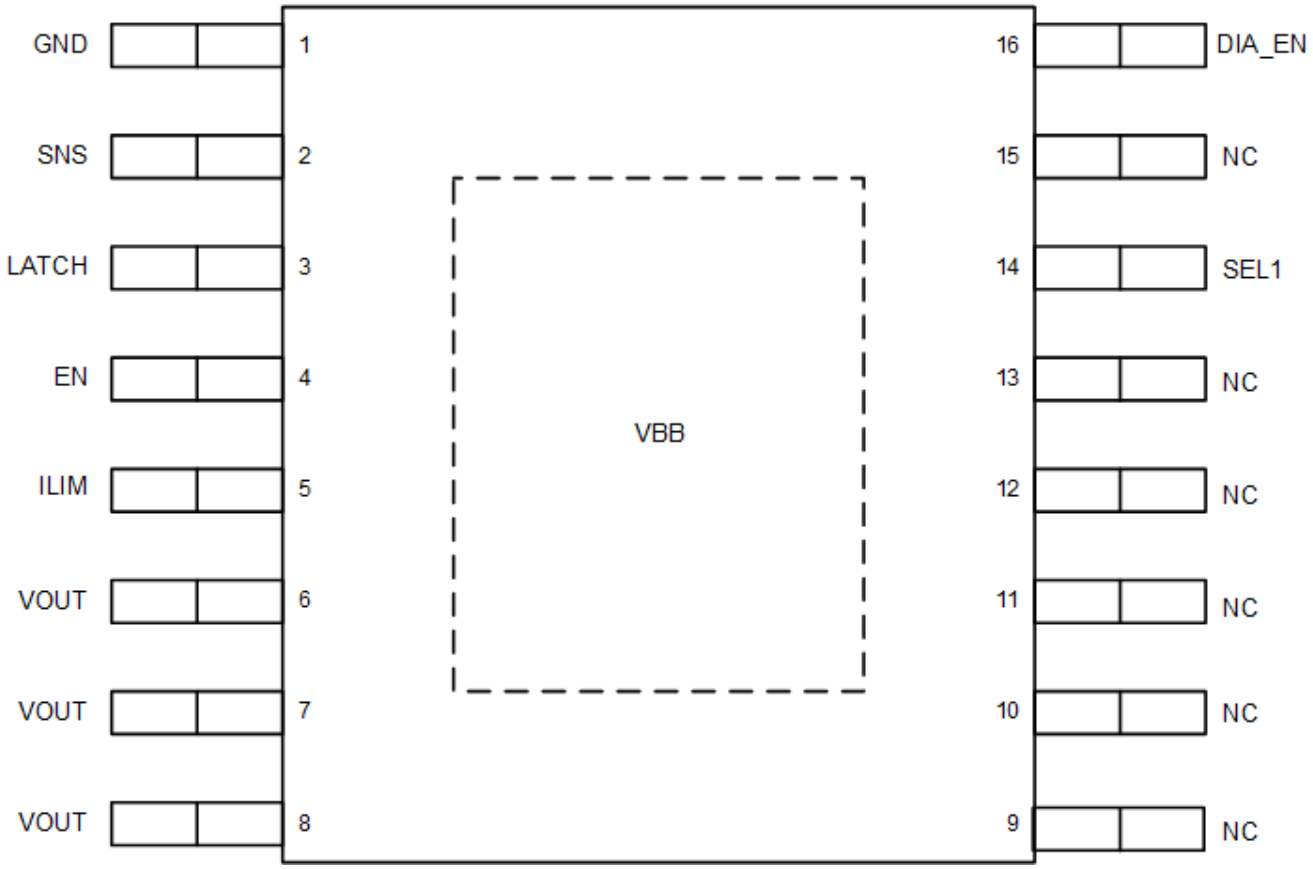

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Follows data sheet recommendation for operating conditions, external component selection and PCB layout

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Resistor/diode network will be bypassed if present.	B
SNS	2	SNS current diagnostic not available.	B
LATCH	3	Normal operation. With device in auto-retry mode.	B
EN	4	Normal operation with output off (FET turned off).	B
ILIM	5	Current limit defaults to internal limit	B
VOUT	6,7,8	Short to GND protection kicks in to protect the device.	B
NC	9,10,11,12,13,15	No effect.	D
SEL	14	Normal operation with diagnostics corresponding to SEL=LOW.	B
DIAG_EN	16	Normal operation with diagnostics function disabled.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	The output is off with the FET turned off.	B
SNS	2	SNS current diagnostic not available.	B
LATCH	3	Normal operation with device in auto-retry mode. Internal pull=down resistor will pull pin to GND.	B
EN	4	Normal operation with output off (FET turned off). Internal pull-down resistor will pull pin to GND.	B
ILIM	5	Current limit defaults to internal limit	B
VOUT	6,7,8	Output off. Open load detection will be triggered in off-state while in diagnostics state.	B
NC	9,10,11,12,13,15	No effect.	D
SEL	14	Normal operation with diagnostics corresponding to SEL=LOW. Internal pull-down resistor will pull pin to GND.	B
DIAG_EN	16	Normal operation with diagnostics function disabled. Internal pull-down resistor will pull pin to GND.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	2 (SNS)	SNS current diagnostic not available.	B
SNS	2	3 (LATCH)	Depends on pin voltage. Sense output may not be correct. Latch function may be enabled if pin voltage > VIH; latch function may be disabled if pin voltage < VIL.	B
LATCH	3	4 (EN)	Device behavior depends on pin voltage. Latch function may be enabled if pin voltage > VIH; Latch function may be disabled if pin voltage < VIL.	B
EN	4	5 (/FLT)	Channel may be enabled if pin voltage > VIH; channel may be disabled if pin voltage < VIL. Fault pin will not work as intended.	B
ILIM	5	6 (VOUT)	Current limit defaults to internal limit.	B
NC	9,10,11,12,13	14 (SEL)	No effect.	D
SEL	14	15 (NC)	No effect.	D
NC	15	16 (DIAG_EN)	No effect.	D
DIAG_EN	16	15 (NC)	No effect.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Supply power will be bypassed and device will not turn on.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SNS	2	If pin voltage exceeds the pin data sheet range, it may cause device damage due to voltage breakdown on ESD circuit.	A
LATCH	3	If pin voltage exceeds the pin data sheet range, it may cause device damage due to voltage breakdown on ESD circuit. Device behavior depends on supply voltage.	A
EN	4	If pin voltage exceeds the pin data sheet range, it may cause device damage due to voltage breakdown on ESD circuit.	A
ILIM	5	Current limit defaults to internal limit.	B
VOUT	6,7,8	Output stuck on to supply. Open load detection will be triggered in off-state in diagnostics state.	C
NC	9,10,11,12,13,15	No effect.	D
SEL	14	If pin voltage exceeds the pin data sheet range, it may cause device damage due to voltage breakdown on ESD circuit.	A
DIAG_EN	16	If pin voltage exceeds the pin data sheet range, it may cause device damage due to voltage breakdown on ESD circuit.	A

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