Functional Safety Information

UCC23511-Q1, UCC23513-Q1, UCC23313-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for UCC23511-Q1, UCC23513-Q1, UCC23313-Q1 (Streched SO-6 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

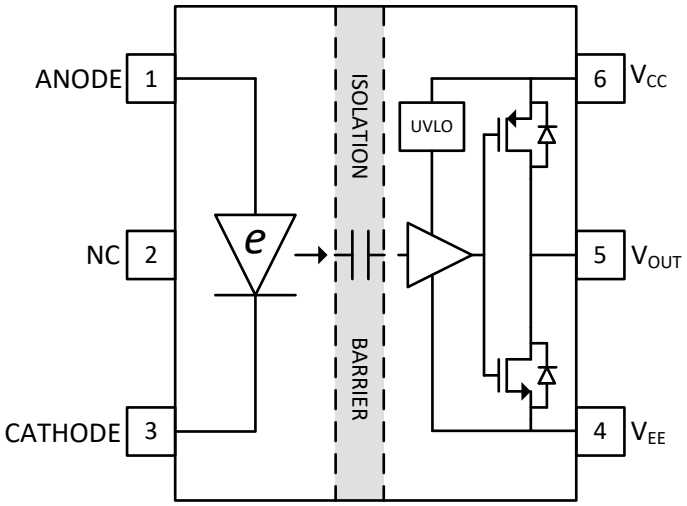

Figure 1-1. Functional Block Diagram

UCC23511-Q1, UCC23513-Q1, UCC23313-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for UCC23511-Q1, UCC23513-Q1, UCC23313-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (50mW, 150mW)	16,19
Die FIT Rate (50mW, 150mW)	3,5
Package FIT Rate (50mW, 150mW)	13,14

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50mW, 150mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC23511-Q1, UCC23513-Q1, UCC23313-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT stuck high	23%
VOUT stuck low	39%
VOUT unknown (low or high)	38%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the UCC23511-Q1, UCC23513-Q1, UCC23313-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the UCC23511-Q1, UCC23513-Q1, UCC23313-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC23511-Q1, UCC23513-Q1, UCC23313-Q1 data sheet.

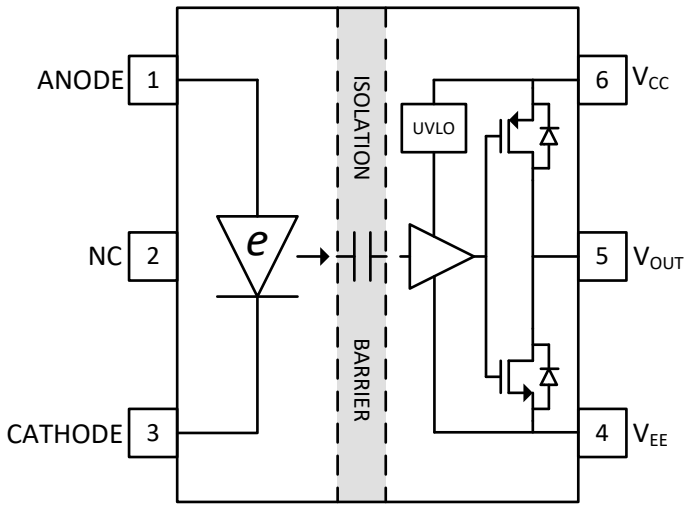

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin short case No.1 to 6 and 3 to 4 are out of scope.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ANODE	1	VOUT state = L (low state).	B
NC (No connect)	2	No impact	D
CATHODE	3	Possible incorrect VOUT state. The external controller cannot control CATHODE current.	B
VEE	4	Shorting to VEE itself. No effect.	D
VOUT	5	VOUT state = L. Possible damge to device.	A
VCC	6	VOUT state = L with reduced pulled-low strength.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ANODE	1	VOUT state = L (low state). VOUT does not repond to the external controller command.	B
NC (No connect)	2	No impact.	D
CATHODE	3	VOUT state = L.VOUT does not repond to the external controller command.	B
VEE	4	VOUT state = H (high state) with reduced pulled-high drive strength. VOUT does not repond to the external controller command.	B
VOUT	5	VOUT is diconnected from the system.	B
VCC	6	VOUT state = L with reduced pulled-low strength.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
ANODE	1	NC	No impact.	D
NC (No connect)	2	CATHODE	No impact.	D
CATHODE	3	Not Applicable	Not Applicable	Not Applicable
VEE	4	VOUT	VOUT state = L. Possible damge to device.	A
VOUT	5	VCC	VOUT state = H. Possible damge to device.	A
VCC	6	Not Applicable	Not Applicable	Not Applicable

Table 4-5. Pin FMA for Device Pins Short-Circuited to 5v supply for Pin No.1,2,and 3,and VCC for Pin No. 4,5 and 6.

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
ANODE	1	The external controller can't command ANODE to CATHODE current via ANODE pin.	B
NC (No connect)	2	No impact.	D
CATHODE	3	VOUT state = L. VOUT does not repond to the external controller command.	B
VEE	4	VOUT state = L with reduced pulled-low drive strength	B
VOUT	5	VOUT state = H. Possible damge to device.	A
VCC	6	Shorting to VCC itself. No effect.	D

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265