Functional Safety Information

DRV8899-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for DRV8899-Q1 to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

DRV8899-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

Figure 1-1 shows the functional block diagram for the DRV8899-Q1 as a reference.

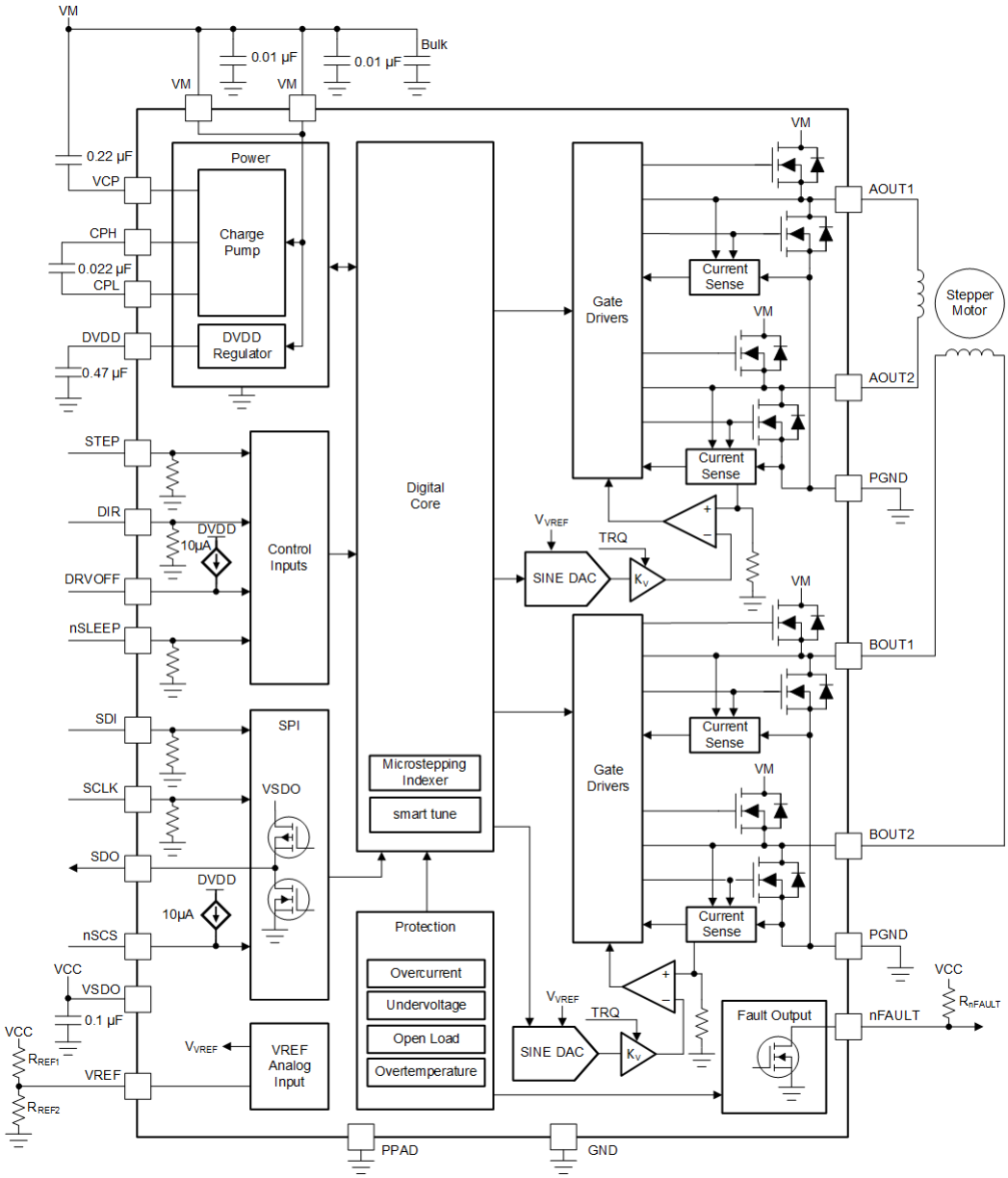

Figure 1-1. DRV8899-Q1 Block Diagram

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for DRV8899-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11.
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2.

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	21
Die FIT Rate	9
Package FIT Rate	12

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: **1 W**
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Lambda ref FIT	Theta vj
5	**CMOS/BICMOS ASICs Analog & Mixed =<50V supply**	**60 FIT**	**70°C**

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for DRV8899-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
xOUTx is stuck LOW when commanded OFF	8%
xOUTx is stuck OFF when commanded LOW	12%
xOUTx ON resistance too high when commanded LOW	8%
Low side slew rate too fast or too slow	3%
xOUTx is stuck HIGH when commanded OFF	9%
xOUTx is stuck OFF when commanded HIGH	13%
xOUTx ON resistance too high when commanded HIGH	9%
High side slew rate too fast or too slow	3%
Dead time is too short	4%
Incorrect communication or fault indication	14%
Current regulation incorrect	17%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the DRV8899-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the package pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the datasheet.

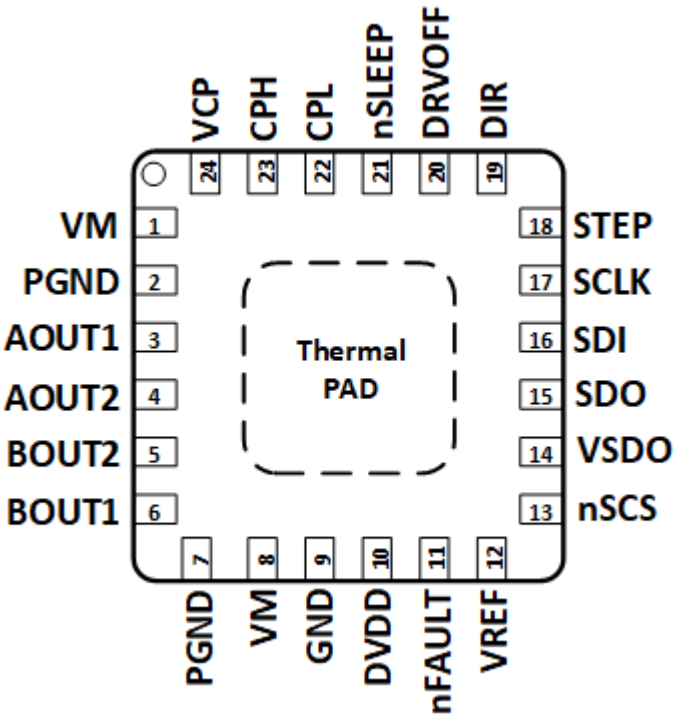

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used with external components consistent with the values described in the external component table of the datasheet.

Table 4-2. QFN Package - Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VM	1	Device will not power up	B

Table 4-2. QFN Package - Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	2	Intended Operation	D
AOUT1	3	Device will signal OCP fault	B
AOUT2	4	Device will signal OCP fault	B
BOUT2	5	Device will signal OCP fault	B
BOUT1	6	Device will signal OCP fault	B
PGND	7	Intended Operation	D
VM	8	Device will signal OCP fault	B
GND	9	Intended Operation	D
DVDD	10	Device external digital power supply stuck low. Device non-operational.	B
nFAULT	11	Device will always be signaling fault	B
VREF	12	Current regulation will be lost	B
nSCS	13	SPI read write functions will be non-functional	B
VSDO	14	SPI read function will be non-functional	B
SDO	15	SPI read function will be non-functional	B
SDI	16	SPI read write functions will be non-functional	B
SCLK	17	SPI read write functions will be non-functional	B
STEP	18	STEP input capability will be lost	B
DIR	19	Direction change capability will be lost	B
DRVOFF	20	Driver control will be lost	B
nSLEEP	21	Device will be in sleep state with OUTx Hi-Z	B
CPL	22	Device charge pump non-operational. Device CPUV fault.	A
CPH	23	Device charge pump non-operational. Device CPUV fault.	A
VCP	24	Device charge pump non-operational. Device CPUV fault.	A

Table 4-3. QFN Package - Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VM	1	Device will not power up	B
PGND	2	Device will not power up	B
AOUT1	3	Device will not be able to drive the load properly	B
AOUT2	4	Device will not be able to drive the load properly	B
BOUT2	5	Device will not be able to drive the load properly	B
BOUT1	6	Device will not be able to drive the load properly	B
PGND	7	Device will not power up	B
VM	8	Device will not power up	B
GND	9	Device will not power up	B
DVDD	10	Device external digital power supply missing. Device non-operational.	B
nFAULT	11	Fault signaling will be lost	B
VREF	12	Current regulation will be lost	B

Table 4-3. QFN Package - Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
nSCS	13	SPI read write functions will be non-functional	B
VSDO	14	SPI read function will be non-functional	B
SDO	15	SPI read function will be non-functional	B
SDI	16	SPI read write functions will be non-functional	B
SCLK	17	SPI read write functions will be non-functional	B
STEP	18	Driver control will be lost	B
DIR	19	Driver control will be lost	B
DRVOFF	20	Driver control will be lost	B
nSLEEP	21	Device will be in sleep state	B
CPL	22	Device charge pump non-operational. Device CPUV fault.	B
CPH	23	Device charge pump non-operational. Device CPUV fault.	B
VCP	24	Device charge pump non-operational. Device CPUV fault.	B

Table 4-4. QFN Package - Pin FMA for Device Pins Shorted to Adjacent Pin

Pin Name	Pin No.	Shorted to Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VM	1	2	Device will not power up	B
PGND	2	3	Device will signal OCP fault	B
AOUT1	3	4	Device will signal OCP fault	B
AOUT2	4	5	Device will signal OCP fault	B
BOUT2	5	6	Device will signal OCP fault	B
BOUT1	6	7	Device will signal OCP fault	B
PGND	7	8	Device will not power up	B
VM	8	9	Device will not power up	B
GND	9	10	Device external digital power supply stuck low. Device non-operational.	B
DVDD	10	11	Device will reset whenever nFAULT is asserted low	B
nFAULT	11	12	Current regulation and fault signalling will be lost	B
VREF	12	13	Current regulation and SPI read write functions will be non-functional	B
nSCS	13	14	SPI read write functions will be non-functional	B
VSDO	14	15	SPI read write functions will be non-functional	B
SDO	15	16	SPI read write functions will be non-functional	B
SDI	16	17	SPI read write functions will be non-functional	B
SCLK	17	18	SPI read write functions and GPIO step input will be non-functional	B
STEP	18	19	STEP input and direction change capabilities will be lost	B
DIR	19	20	Direction change and OUTx control will be lost	B
DRVOFF	20	21	Driver control will be lost	B
nSLEEP	21	22	Device charge pump non-operational. Device CPUV fault.	A
CPL	22	23	Device charge pump non-operational. Device CPUV fault.	A

Table 4-4. QFN Package - Pin FMA for Device Pins Shorted to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CPH	23	24	Device charge pump non-operational. Device CPUV fault.	A
VCP	24	1	Device charge pump non-operational. Device CPUV fault.	B

Table 4-5. QFN Package - Pin FMA for Device Pins Shorted to VM (High Voltage Supply)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VM	1	Intended Operation	D
PGND	2	Device will not power up	B
AOUT1	3	Device will signal OCP fault	B
'AOUT2	4	Device will signal OCP fault	B
BOUT2	5	Device will signal OCP fault	B
BOUT1	6	Device will signal OCP fault	B
PGND	7	Device will not power up	B
VM	8	Intended Operation	D
GND	9	Device will not power up	B
DVDD	10	Low voltage pin max voltage violated.	A
nFAULT	11	Low voltage pin max voltage violated.	A
VREF	12	Low voltage pin max voltage violated.	A
nSCS	13	Low voltage pin max voltage violated.	A
VSDO	14	Low voltage pin max voltage violated.	A
SDO	15	Low voltage pin max voltage violated.	A
SDI	16	Low voltage pin max voltage violated.	A
SCLK	17	Low voltage pin max voltage violated.	A
STEP	18	Low voltage pin max voltage violated.	A
DIR	19	Low voltage pin max voltage violated.	A
DRVOFF	20	Low voltage pin max voltage violated.	A
nSLEEP	21	Driver control will be lost	B
CPL	22	Device charge pump non-operational. Device CPUV fault.	A
CPH	23	Device charge pump non-operational. Device CPUV fault.	A
VCP	24	Device charge pump non-operational. Device CPUV fault.	B

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