Functional Safety Information

UCC27211A-Q1 UCC27212A-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for UCC27211A-Q1 UCC27212A-Q1 (SOIC package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Functional Block Diagram shows the device functional block diagram for reference.

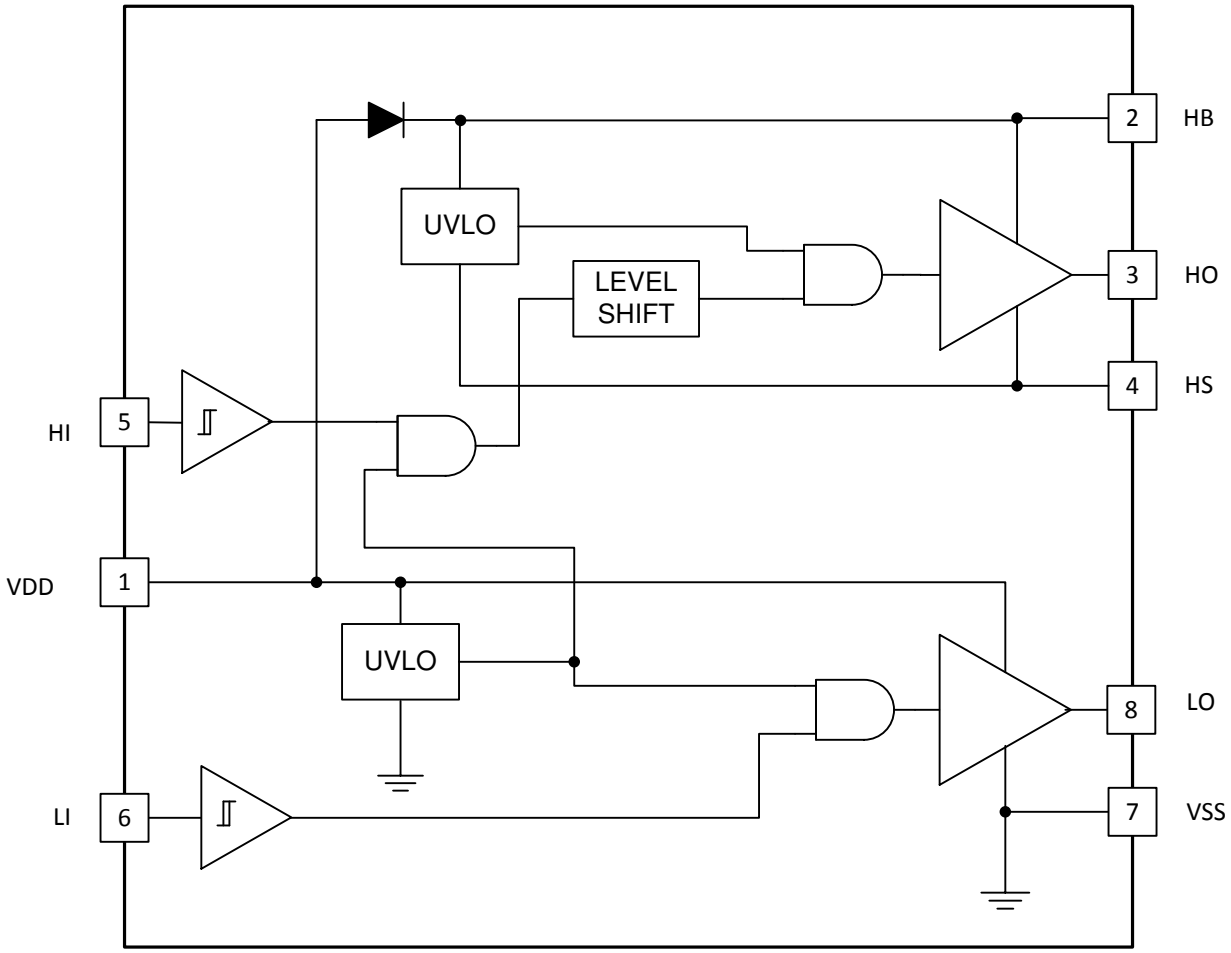

Figure 1-1. Functional Block Diagram

UCC27211A-Q1 UCC27212A-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for UCC27211A-Q1 UCC27212A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (Power dissipation=50, 500 mA)	10,12
Die FIT Rate (Power dissipation=50, 500 mA)	3,4
Package FIT Rate (Power dissipation=50, 500 mA)	7,8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50, 500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC27211A-Q1 UCC27212A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
HO stuck low	16.3%
HO stuck high	16.3%
HO unkown or level is outside of specified level	16.3%
LO stuck low	16.3%
LO stuck high	16.3%
LO unkown or level is outside of specified level	16.3%
High side UVLO not functioning	1%
Low side UVLO not functioning	1%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the UCC27211A-Q1 UCC27212A-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the UCC27211A-Q1 UCC27212A-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC27211A-Q1 UCC27212A-Q1 data sheet.

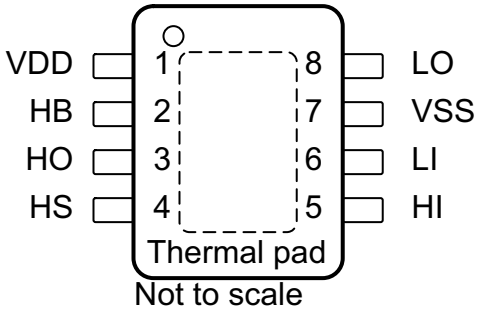

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin #1 short to Pin #8 and Pin #4 short to Pin #5 are not considered.
- Short-Circuited to supply case is analyzed for short to VDD.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Device power up not possible. Device positive supply short to ground.	B
HB	2	Possible boostrap diode damage. HO output is stuck low.	A
HO	3	Possible damage to HO output driver. HO output is stuck low.	A
HS	4	HO level is stuck low or ground level. High side power FET can't pull up HO node.	B
HI	5	HO is stuck low.	B
LI	6	LO is stuck low.	B
VSS	7	No effect. Short to same potential.	D
LO	8	LO is stuck low. Possible LO output driver damage.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Device power up not possible. Device positive supply is open.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
HB	2	High side UVLO is detected. HO is stuck low.	B
HO	3	Power FET gate is disconnected from HO.	D
HS	4	HO output level is unknown.	B
HI	5	HO is stuck low.	B
LI	6	LO is stuck low.	B
VSS	7	No ground connection to the device. LO and HO potentially pulled up to VDD level.	
LO	8	Power FET gate is disconnected from HO.	

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	HB	High side UVLO is detected. HO is stuck low	B
HB	2	HO	Possible damage to boostrap diode and HO output stage.	A
HO	3	HS	Possible damage to boostrap diode and HO output stage.	A
HI	5	LI	HO and LO states depend on the driving source of LI and HI.	B
LI	6	VSS	LO is stuck low.	B
VSS	7	LO	LO is stuck low. Possible damage to LO output driver.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No effect. Short to same potential.	D
HB	2	High side UVLO is detected. HO is stuck low	B
HO	3	HO is stcuk high at VDD level. Possible damgae to HO driver.	A
HS	4	HO is stcuk high at VDD level. Possible damgae to HO driver.	A
HI	5	HO is stuck high.	B
LI	6	LO is stuck high.	B
VSS	7	Device power up not possible. Device positive supply short to ground.	B
LO	8	LO is stcuk high at VDD level. Possible damgae to LO driver.	A

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