Functional Safety Information

TPSM53602

Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TPSM53602 (B3QFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

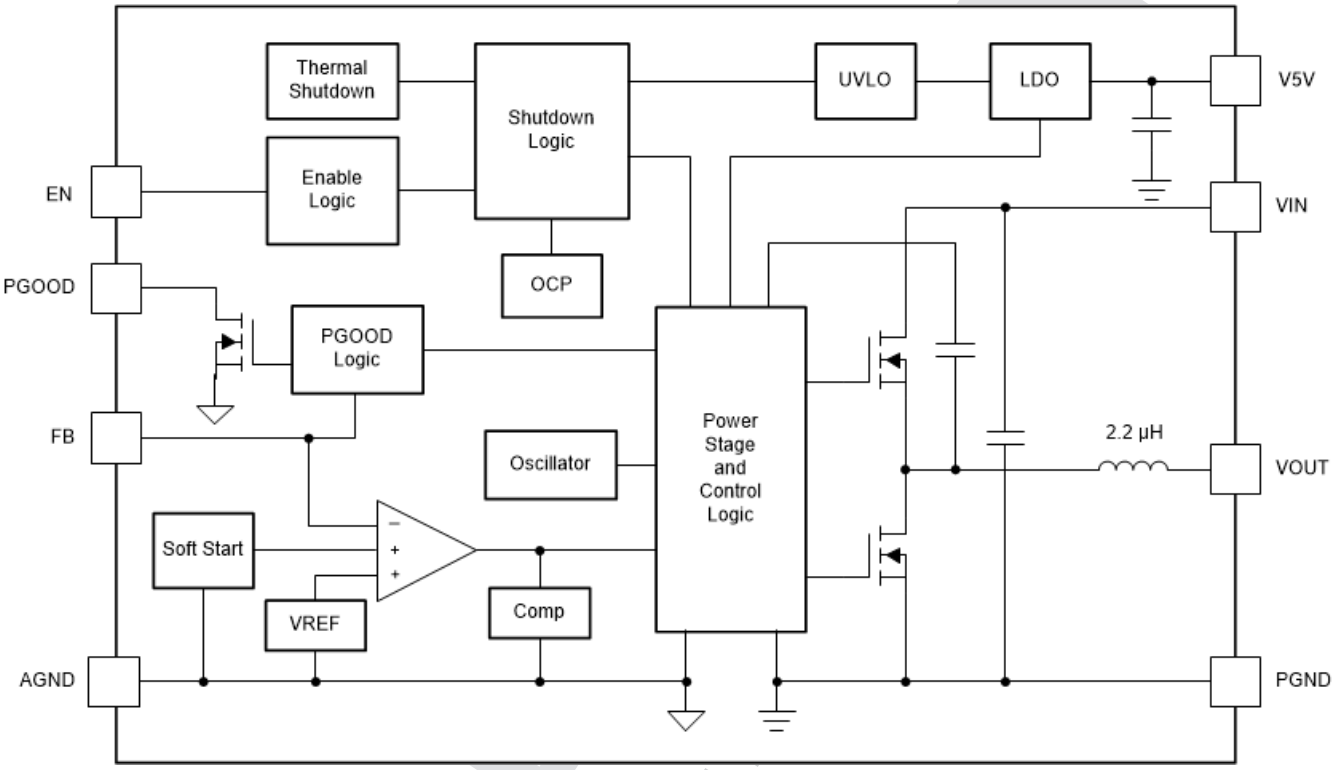

Figure 1-1. Functional Block Diagram

TPSM53602 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPSM53602 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	22
Die FIT Rate	4
Package FIT Rate	9
Passives FIT Rate	9

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 555 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPSM53602 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No Output Voltage	60%
Output not in specification - voltage or timing	25%
Gate driver stuck on	5%
Power Good - False trip or fails to trip	5%
Short circuit any two pins	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPSM53602. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPSM53602 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPSM53602 data sheet.

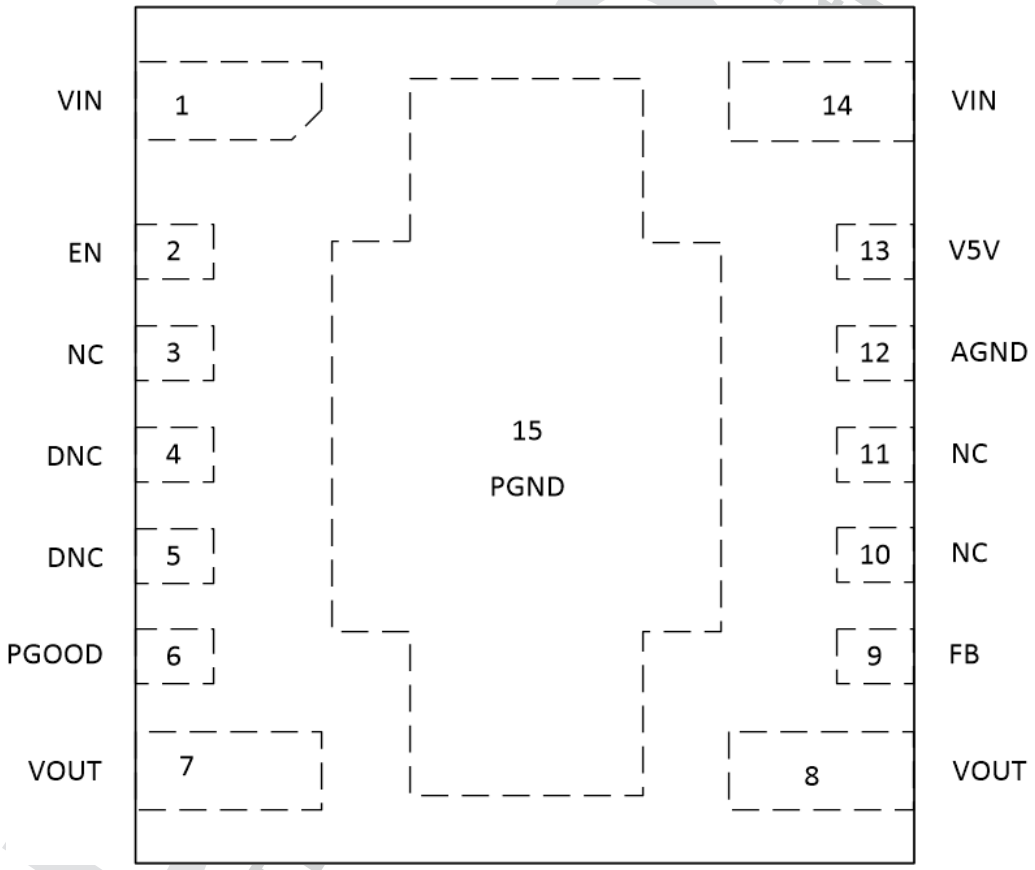

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the TPSM53602 data sheet is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1, 14	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current can damage device.	A
EN	2	Loss of ENABLE functionality. Device will remain in Shutdown mode.	B
NC	3, 10, 11	Not connected to any circuitry within the module; no effect	D
DNC	4, 5	Possible damage to internal circuits	A
PGOOD	6	This is a valid connection for PGOOD output. PGOOD functionality will be lost. Damage to customer components connected to PGOOD input can occur.	B
VOUT	7, 8	Loss of output voltage	B
FB	9	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage (VIN) level. Possible damage to customer load, output stage components can occur, or both. No effect on device.	B
AGND	12	No effect	D
V5V	13	Fault mode will shut down device.	B
PGND	15	No effect	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1, 14	With both pins open: loss of output voltage. With one pin open: possible device damage.	A
EN	2	Loss of enable functionality. Erratic operation; probable loss of regulation	B
NC	3, 10, 11	Not connected to any circuitry within the module; no effect	D
DNC	4, 5	No effect	D
PGOOD	6	This is a valid connection for the PGOOD output. PGOOD functionality will be lost.	B
VOUT	7, 8	Loss of output voltage	B
FB	9	Loss of output volage regulation. Output voltage can rise or fall outside of intended regulation window.	B
AGND	12	Loss of output voltage regulation. Possible damage to internal circuits	A
V5V	13	This is a valid connection for V5V pin.	D
PGND	15	Erratic operation; probable loss of regulation. Possible device damage	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	EN	This is a valid input for VIN. Enable functionality will be lost; the device will remain on.	B
EN	2	NC	Loss of enable functionallity. Probable loss of regulation	B
NC	3	DNC	NC pin is not connected to any circuitry within the module; no effect	D
DNC	4	DNC	Possible damage to internal circuits	A
DNC	5	PGOOD	Possible damage to internal circuits	A
PGOOD	6	VOUT	Possible damge to internal circuits	A
VOUT	7	PGND	Loss of output voltage	B
VOUT	8	FB	Erratic operation; probable loss of regulation. Damage to internal circuits will occur for VOUT > 5.5 V.	A
FB	9	NC	NC pin not connected to any circuitry within the module; no effect	D
NC	10	NC	Neither pin connected to any circuitry within the module; no effect	D
NC	11	AGND	NC pin not connected to any circuitry within the module; no effect	D
AGND	12	V5V	Fault mode will shut down device.	B
V5V	13	VIN	Damage to internal circuits for VIN > 5.5 V	A
VIN	14	PGND	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current can damage device.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1, 14	No effect.	D
EN	2	No damage to device. Loss of enable functionality.	B
NC	3, 10, 11	No effect.	C
DNC	4, 5	Possible damage to internal circuits.	A
PGOOD	6	Damage to internal circuits.	A
VOUT	7, 8	The output voltage will rise to nearly the level of VIN. Customer load will be damaged. Possible damage to device.	A
FB	9	Damage to internal circuits will occur for VIN > 5.5 V.	A
AGND	12	Possible damage to internal circuits or package.	A
V5V	13	Damage to internal circuits for VIN > 5.5 V.	A
PGND	15	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A

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