Functional Safety Information

TPSM33625
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPSM33625 (QFN-HR package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

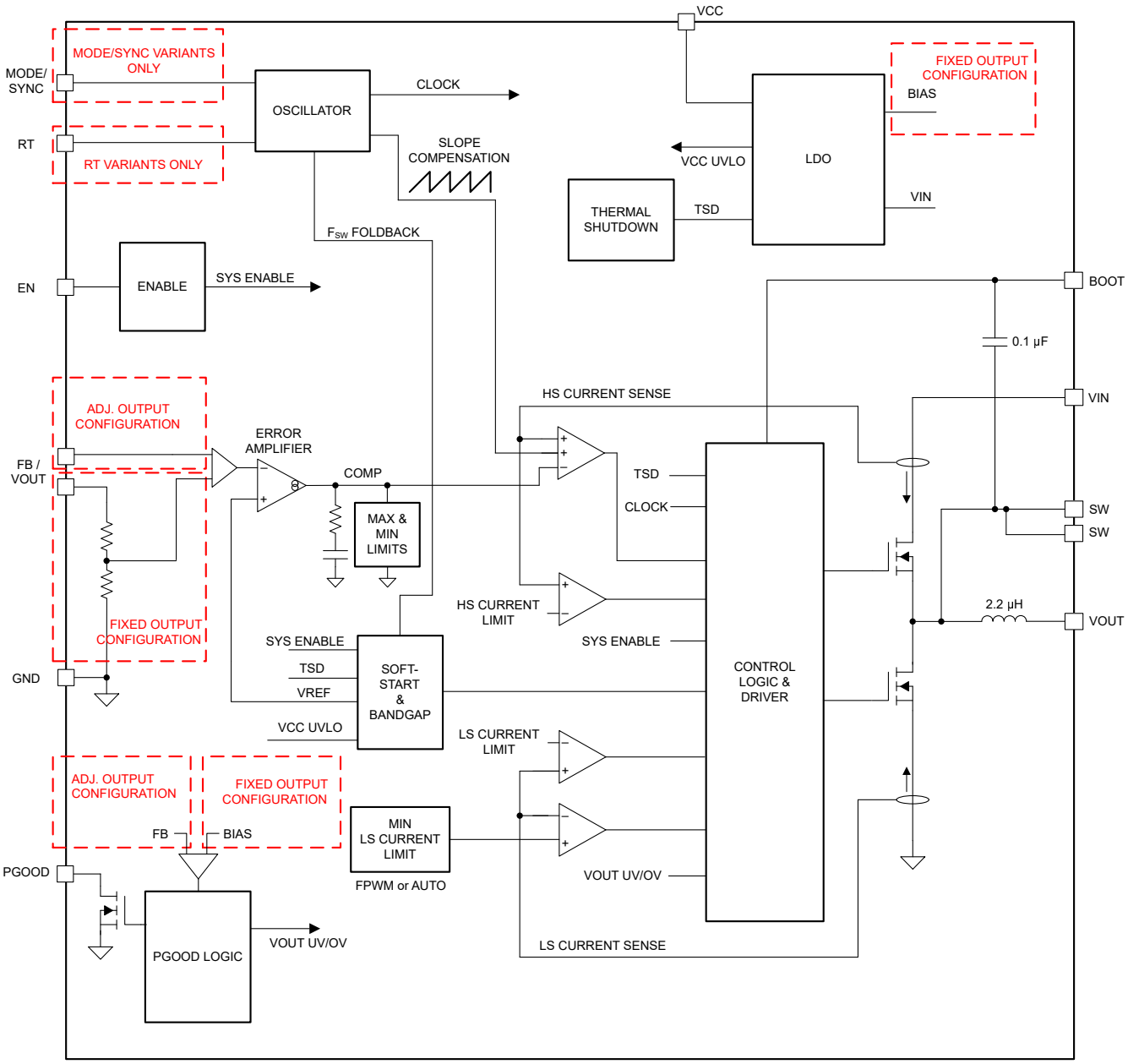

Figure 1-1. Functional Block Diagram

The TPSM33625 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPSM33625 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	30
Die FIT rate	6
Package FIT rate	24

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed = < 50-V supply	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPSM33625 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	60
Output not in specification-voltage or timing	30
PG false trip or fails to trip	5
Short circuit any two pins	5

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPSM33625. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPSM33625 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPSM33625 data sheet.

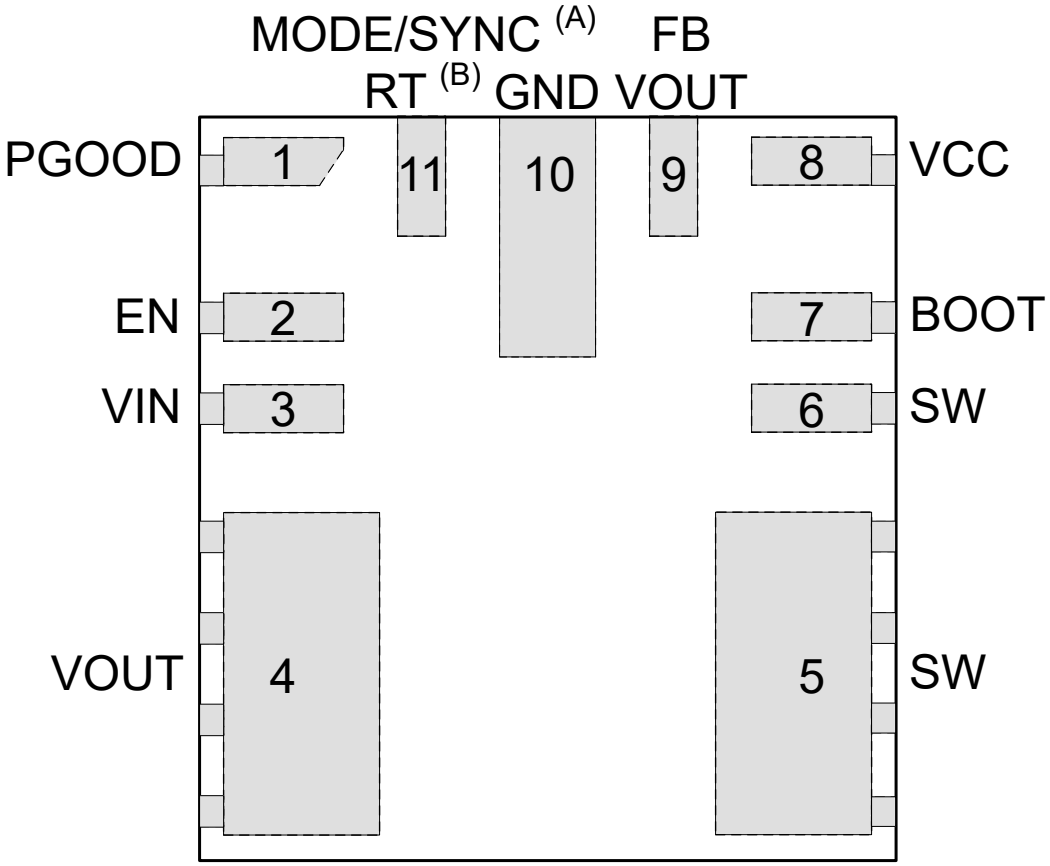

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The product data sheet application circuit is followed.

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RT	11	Switching Frequency is 2.2 MHz	D
PGOOD	1	When not in use, can be left open, grounded.	D
EN/UVLO	2	VOUT = 0 V, part is disabled	B
VIN	3	VOUT = 0 V	B
SW	5 and 6	Device damage.	A
BOOT	7	VOUT = 0, HS does not turn on	B
VCC	8	VOUT = 0 V	B
FB	9	VOUT = 0 V	B
GND	10	VOUT normal	D
VOUT	4	Goes in to hiccup, short-circuit operation	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RT	11	If its RT part, frequency is not defined. If it is a MODE/SYNC part, then part can go back and forth between FPWM/PFM. Part is up, part functional.	C
PGOOD	1	When not in use, can be left open, grounded.	D
EN/UVLO	2	Pin cannot be left floating	B
VIN	3	VOUT = 0 V	B
SW	5 and 6	Normal operation	D
BOOT	7	Normal operation	D
VCC	8	VCC output is unstable, can increase above 5.5 V	A
FB	9	VOUT = 0 V. Do not float this pin.	C
GND	10	Vout can be abnormal, as reference voltage is not fixed	C
VOUT	4	Normal operation	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
RT	11	PGOOD	If PGOOD is high, and < 5.5V Fsw = 1 MHz; If PGOOD is low, Fsw = 2.2 MHz .PGOOD absmax being 20 V, RT ESD damages if PG goes to 20 V.	A
PGOOD	1	EN/UVLO	If EN > 20 V, it damages devices connected to PGOOD pin.	A
EN/UVLO	2	VIN	VOUT normal	D
VIN	3	SW	If VIN > 16 V, damage occurs	A
SW	5 and 6	BOOT	VOUT = 0 V, HS does not turn on, no Cboot	B
BOOT	7	VCC	Damage occurs, break VCC pin	A
VCC	8	FB	Can be nonfunctional, no damage occurs	B
FB	9	GND	VOUT = 0 V (for fixed option), switches at max duty cycle for ADJ option	B
GND	10	RT	VOUT normal if RT/MODE/SYNC pin is low, otherwise not functional.	D
Vout	4	SW	Damage occurs	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RT	11	If Vin > 5.5 V, damage occurs. If Vin < 5.5 V, switching frequency is 1 MHz	A
PGOOD	1	If VIN > 20 V, it damages PGOOD	A

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Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN/UVLO	2	VOUT normal	D
VIN	3	VOUT normal	D
SW	5 and 6	Device damage	A
BOOT	7	Damage occurs, BOOT ESD clamp is damaged	A
VCC	8	If Vin > 5.5, damage occurs	A
FB	9	If VIN > 20 V, damage occurs	A
GND	10	VOUT = 0 V	A
VOUT	4	Damage occurs if VIN > 16 V	A

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