Functional Safety Information

OPA2197-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for OPA2197-Q1 (VSSOP-8 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

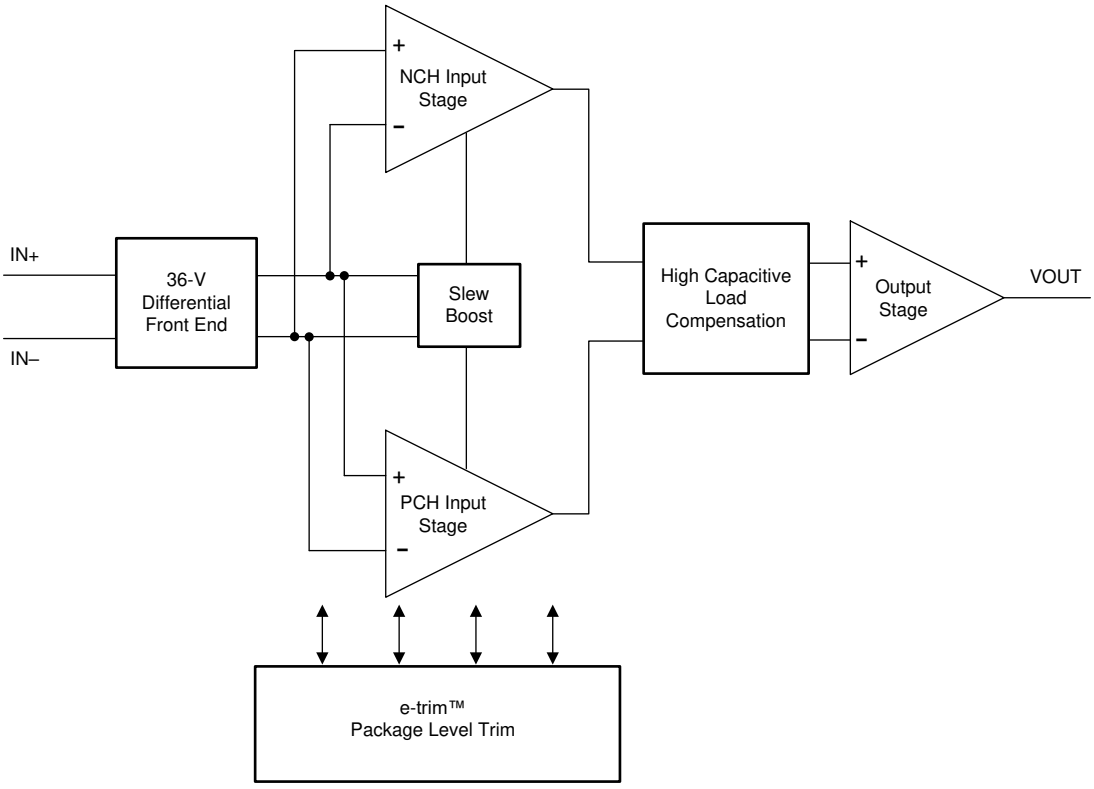

Figure 1-1. Functional Block Diagram

OPA2197-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for OPA2197-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	3
Package FIT Rate	3

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 54 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for OPA2197-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	20%
Output saturated high	25%
Output saturated low	25%
Output functional, out of specification voltage or timing	30%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the OPA2197-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the OPA2197-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the OPA2197-Q1 data sheet.

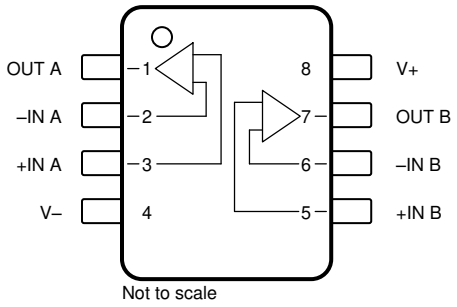

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- 'Short circuit to Power' means short to V+.
- 'Short circuit to GND or Ground' means short to V–.
- V+ is equivalent to VCC and V– equivalent to VEE.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT A	1	Depending on the circuit configuration, the device is likely to be forced into a short–circuit condition with the OUT A voltage ultimately forced to the V– voltage. Prolonged exposure to short–circuit conditions could result in long–term reliability issues.	A
-IN A	2	The device does not receive negative feedback. Depending on the circuit configuration, the output most likely moves to the negative supply.	B
+IN A	3	Device common–mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common–mode condition.	C
+IN B	5	Device common–mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common–mode condition.	C
-IN B	6	The device does not receive negative feedback. Depending on the circuit configuration, the output most likely moves to the negative supply.	B
OUT B	7	Depending on the circuit configuration, the device is likely to be forced into a short–circuit condition with the OUT B voltage ultimately forced to the V– voltage. Prolonged exposure to short–circuit conditions could result in long–term reliability issues.	A
V+	8	Op–amp supplies are shorted together, leaving the V+ pin at some voltage between the V+ and V– sources (depending on the source impedance).	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT A	1	No negative feedback or ability for OUT A to drive the application.	B
-IN A	2	Inverting pin of the op amp is left floating. Negative feedback is not provided to the device, likely resulting in the device output moving between the positive and negative rails. The –IN A pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
+IN A	3	Device common–mode is disconnected. The op amp is not provided with common–mode bias, and the device output likely ends up at the positive or negative rail. The +IN A pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
V-	4	Negative supply is left floating. The op amp ceases to function because no current can source or sink to the device.	B
+IN B	5	Device common–mode is disconnected. The op amp is not provided with common–mode bias, and the device output likely ends up at the positive or negative rail. The +IN B pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
-IN B	6	Inverting pin of the op amp is left floating. Negative feedback is not provided to the device, likely resulting in the device output moving between the positive and negative rails. The –IN B pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
OUT B	7	No negative feedback or ability for OUT B to drive the application.	B
V+	8	Positive supply is left floating. The op amp ceases to function because no current can source or sink to the device.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT A	1	2	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application might not function as intended.	B
–IN A	2	3	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
+IN A	3	4	Device common–mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common–mode condition.	C
V-	4	5	Device common–mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common–mode condition.	C
+IN B	5	6	Both inputs are tied together. Depending on the offset of the device, the output voltage likely moves to near midsupply.	D
-IN B	6	7	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application might not function as intended.	B
OUT B	7	8	Depending on the circuit configuration, the device is likely to be forced into a short–circuit condition with the OUT B voltage ultimately forced to the V+ voltage. Prolonged exposure to short–circuit conditions could result in long–term reliability issues.	A
V+	8	1	Depending on the circuit configuration, the device is likely to be forced into a short–circuit condition with the V+ voltage ultimately forced to the OUT A voltage. Prolonged exposure to short–circuit conditions could result in long–term reliability issues.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT A	1	Depending on the circuit configuration, the device is likely to be forced into a short–circuit condition with the OUT A voltage ultimately forced to the V+ voltage. Prolonged exposure to short–circuit conditions could result in long–term reliability issues.	A
-IN A	2	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output most likely moves to the negative supply.	B
+IN A	3	Depending on the circuit configuration, the application is likely not to function because device common–mode voltage is connected to +IN A.	B
V-	4	Op–amp supplies are shorted together, leaving the V– pin at some voltage between the V– and V+ sources (depending on the source impedance).	A
+IN B	5	Depending on the circuit configuration, the application is likely not to function because device common–mode voltage is connected to +IN B.	B
-IN B	6	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output most likely moves to the negative supply.	B
OUT B	7	Depending on the circuit configuration, the device is likely to be forced into a short–circuit condition with the OUT B voltage ultimately forced to the V+ voltage. Prolonged exposure to short–circuit conditions could result in long–term reliability issues.	A

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