Functional Safety Information

LM5185-Q1 and LM25185-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the LM5185-Q1 and LM25185-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

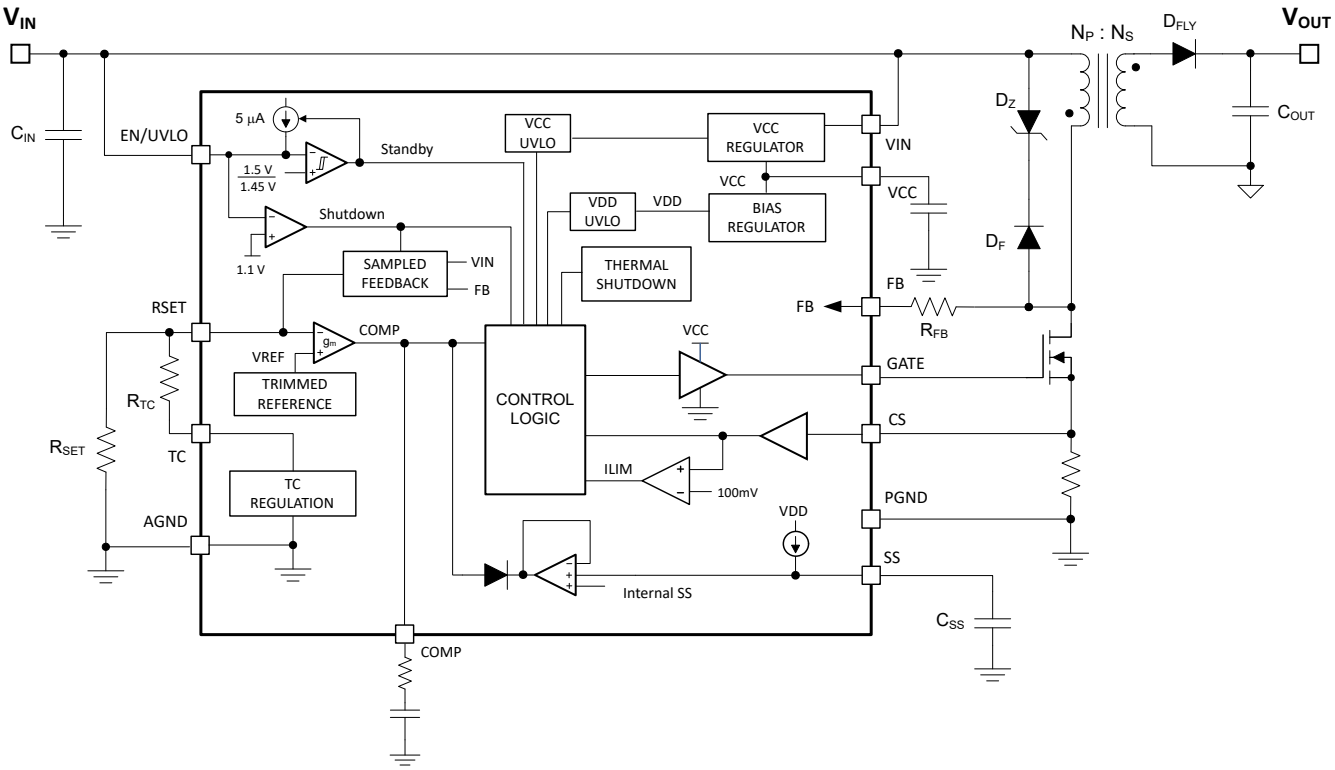

Figure 1-1. Functional Block Diagram

The LM5185-Q1, LM25185-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LM5185-Q1 and LM25185-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	17
Die FIT rate	8
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 700 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM5185-Q1 and LM25185-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	25%
Output not in specification – voltage or timing	45%
Gate driver stuck on	10%
EN/UVLO false trip or fails to trip	15%
Short circuit to any two pins	5%

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM5185-Q1 and LM25185-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM5185-Q1 and LM25185-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM5185-Q1 and LM25185-Q1 data sheets.

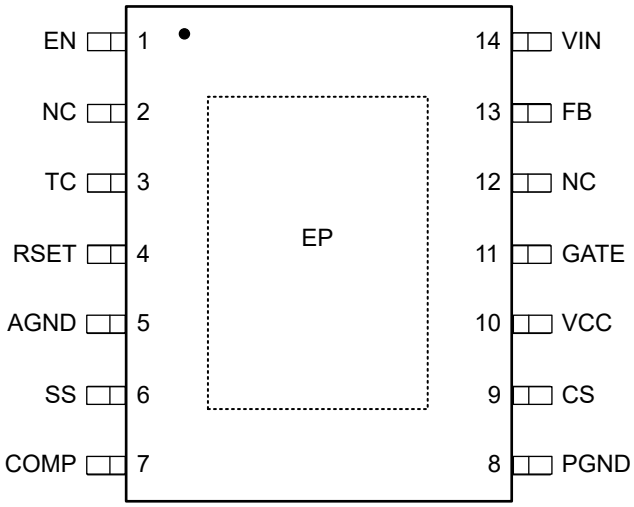

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the Recommended Operating Conditions and the Absolute Maximum Ratings found in the LM5185-Q1 and LM25185-Q1 data sheets.
- Application circuit as shown in the Application and Implementation section found in the LM5185-Q1 and LM25185-Q1 data sheets.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	VOUT = 0 V. Shutdown operation.	B
NC	2	Normal operation.	D
TC	3	Temperature compensation disabled; VOUT will be slightly higher than the target due to RTC|| RSET.	C
RSET	4	120 µs switching, delivering a power of ½ × L × I_pk^2 × fsw to the output.	B
AGND	5	Normal operation.	D
SS	6	If short during start-up, delivering a power of ½ × L × I_pk_min^2 × fsw_min (minimum load) to the output. If short during steady-state, normal operation.	B
COMP	7	Delivering a power of ½ × L × I_pk_min^2 × fsw_min (minimum load) to the output.	B
PGND	8	Normal operation.	D
CS	9	Forced maximum Ton of 32 us. Potentially damage the FET and VOUT = 0 V.	A
VCC	10	VOUT = 0 V.	B
GATE	11	VOUT = 0 V. Potential damage to VCC and GATE.	A
NC	12	Normal operation.	D
FB	13	VOUT = 0 V. Damage the internal VIN to FB diode.	A
VIN	14	VOUT = 0 V.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	Shutdown or normal operation since EN is high impedance	B
NC	2	Normal operation.	D
TC	3	VOUT regulating. Temperature compensation disabled.	C
RSET	4	Delivering a power of ½ × L × I_pk_min^2 × fsw_min (minimum load) to the output.	B
AGND	5	Floating ground. Vout = 0 V.	B
SS	6	VOUT regulating. Internal SS.	C
COMP	7	Loss of loop compensation and the output voltage can oscillate.	B
PGND	8	Floating ground. Vout = 0 V. External FET can be damaged.	B
CS	9	VOUT = 0 V. CS is pulled up internally. Device enters hiccup.	B
VCC	10	High ripple on VCC pin that can trigger VCC UVLO.	B
GATE	11	VOUT = 0 V.	B
NC	12	Normal operation.	D
FB	13	120 µs switching, delivering a power of 1/2× L × I_pk^2 × fsw to the output.	B
VIN	14	VOUT = 0 V.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	Normal operation.	D
NC	2	Normal operation.	D
TC	3	120 µs switching, delivering a power to the output (the power can be ½ × L × I_pk^2 × fsw, ½ × L × I_pk_min^2 × fsw, or between); TC disabled.	B
RSET	4	120 µs switching, delivering a power of ½ × L × I_pk^2 × fsw to the output.	B
AGND	5	If short during start-up, delivering a power of ½ × L × I_pk_min^2 × fsw_min (minimum load) to the output. If short during steady-state, normal operation.	B
SS	6	VOUT is a little higher than regulation target. Compensation network is changed and output voltage can oscillate.	B
COMP	7	Corner pin not considered.	NA
PGND	8	Forced maximum Ton of 32 us. Potentially damage the FET and VOUT = 0 V.	A
CS	9	VOUT = 0 V. Damage CS pin.	A
VCC	10	VOUT = 0 V. Damage the gate driver.	A
GATE	11	Normal operation.	D
NC	12	Normal operation.	D
FB	13	VOUT = 0 V.	B
VIN	14	Corner pin not considered.	NA

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	VOUT regulating. Always in active mode.	C
NC	2	Normal operation.	D
TC	3	Potentially damage TC pin if VIN > 5 V.	A
RSET	4	Damage RSET pin.	A
AGND	5	VOUT = 0 V.	B
SS	6	Potentially damage SS pin if VIN > 5 V.	A
COMP	7	Potentially damage COMP pin if VIN > 5 V.	A
PGND	8	VOUT = 0 V.	B
CS	9	Damage CS pin.	A
VCC	10	Potentially damage VCC pin if VIN > 15 V. Otherwise Vout regulating with gate drive voltage = VIN.	A
GATE	11	Potentially damage GATE and VCC pin.	A
NC	12	Normal operation.	D
FB	13	VOUT = 0 V.	B
VIN	14	Normal operation.	D

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265