Functional Safety Information

DRV8242-Q1 H-Bridge Driver Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for DRV8242-Q1 to aid in a functional safety system design. This document covers all the device package and interface variants as listed below:

1. HW variant in VQFN-RHL package
2. SPI "S" variant in VQFN-RHL package
3. SPI "P" variant in VQFN-RHL package

Note

The DRV8242-Q1 HW (H) and SPI (P) variants are preview only, pre-production status.

Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA) for all the package and interface variants

Figure 1-1 shows the functional block diagram for the HW device variant reference.

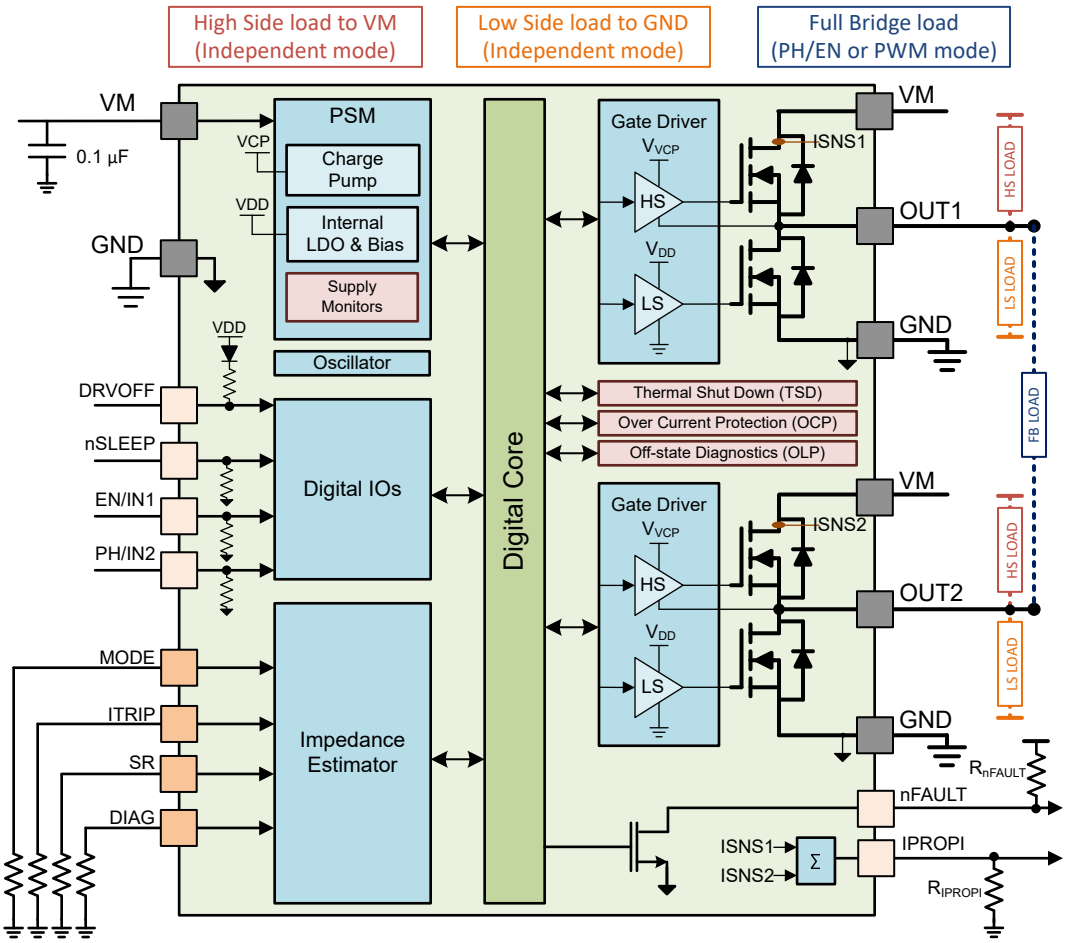

Figure 1-1. Functional Block Diagram for HW Variant

Figure 1-2 shows the functional block diagram for the SPI "S" device variant for reference.

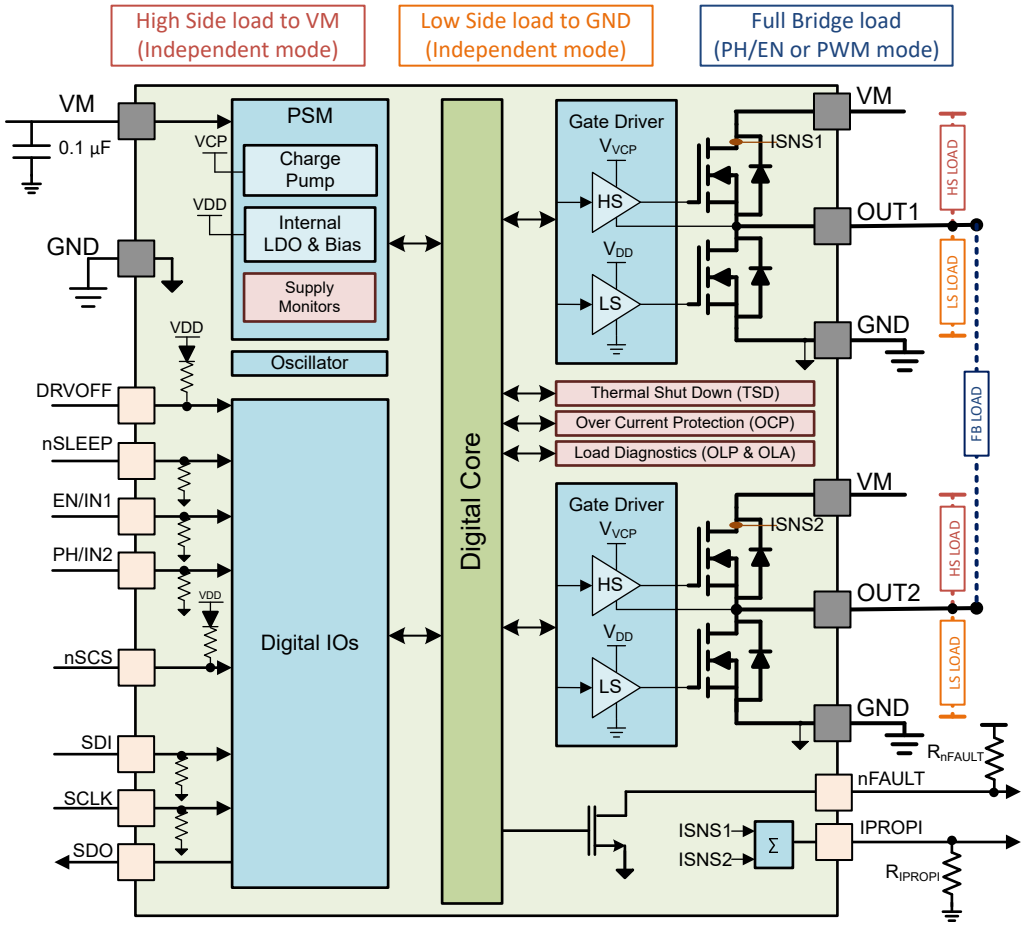

Figure 1-2. Functional Block Diagram for SPI S Variant

Figure 1-3 shows the functional block diagram for the SPI "P" device variant for reference.

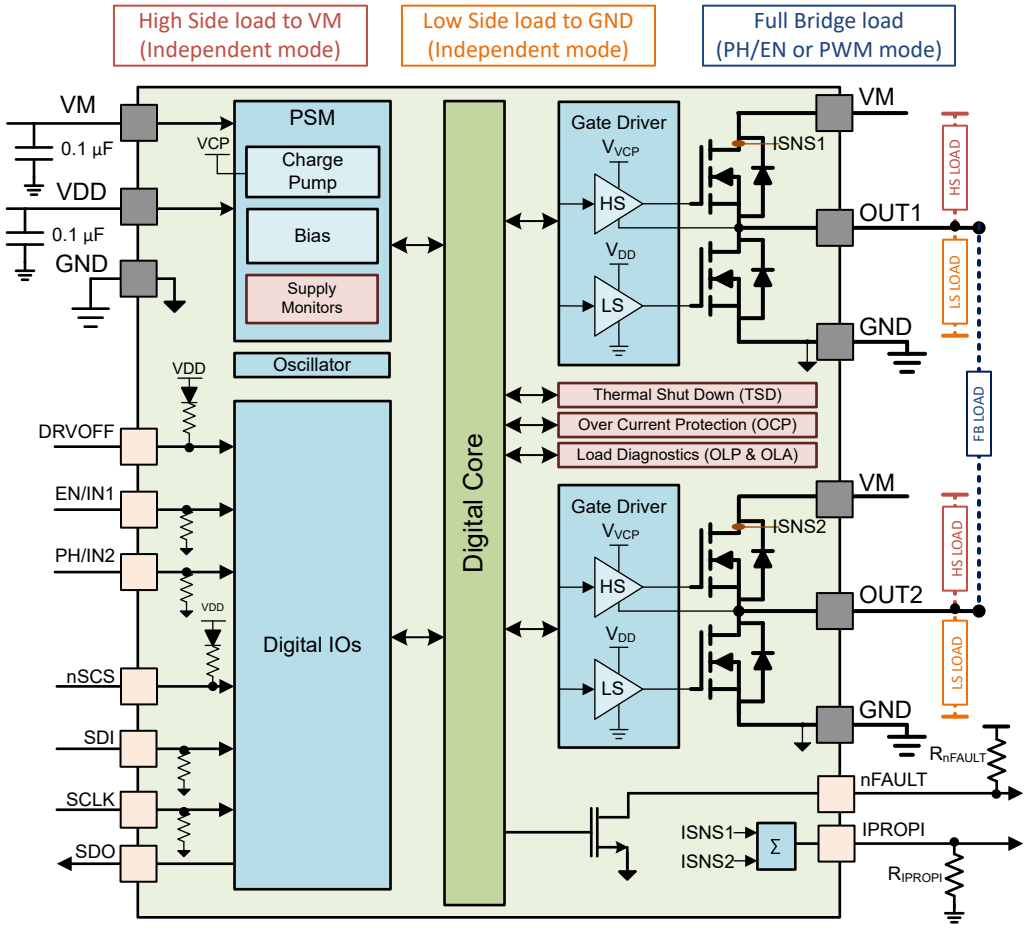

Figure 1-3. Functional Block Diagram for SPI P Variant

DRV8242-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for DRV8242-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)		
	HW Variant in VQFN-RHL Package	SPI "S" Variant in VQFN-RHL Package	SPI "P" Variant in VQFN-RHL Package
Total Component FIT Rate	**20**	**20**	**20**
Die FIT Rate	**10**	**10**	**10**
Package FIT Rate	**10**	**10**	**10**

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1150 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS,BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for DRV8242-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output is stuck LOW when commanded OFF (GND short)	14%(2)
Output is stuck HIGH when commanded OFF (VM short)	14%(2)
Output is stuck OFF when commanded LOW (Open)	8%(2)
Output is stuck OFF when commanded HIGH (Open)	8%(2)
Output ON resistance too high when commanded LOW	12%(2)
Output ON resistance too high when commanded HIGH	18%(2)
Low side slew rate too fast or too slow (high-side recirculation)	5%(2)
High side slew rate too fast or too slow (low-side recirculation)	5%(2)
Dead-time is too short	1%(2)
Current sense feedback incorrect	3%
ITRIP current regulation incorrect	3%
Incorrect communication (SPI variant)/ configuration interpretation (HW variant)	4%(1)
Incorrect input interpretation (nSLEEP, DRVOFF, EN/IN1, PH/IN2)	4%(1)
Incorrect nFAULT assertion	1%

(1) 1% for each pin function
(2) 50% for OUT1, 50% for OUT2

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) of the pins for each of the device variants of DRV8242-Q1 as listed below.

1. SPI "S" variant in VQFN-RHL package
2. SPI "P" variant in VQFN-RHL package
3. HW variant in VQFN-RHL package

The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground
- Pin open-circuited
- Pin short-circuited to an adjacent pin
- Pin short-circuited to supply

The analysis also indicates how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

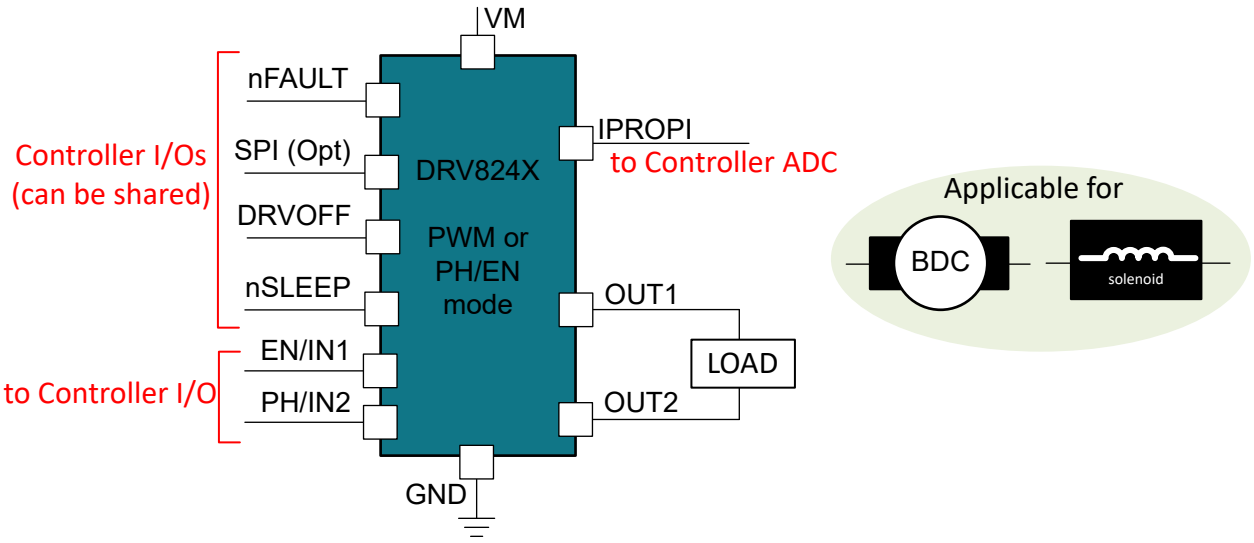

Figure 4-1. DRV824x-Q1 in Full Bridge Mode

- Test conditions:
  - V_{VM} = 13.5 V, $T_{Ambient}$ = 25°C, SPI "P" variant: V_{VDD} = 5 V
- SPI "S" variant:
  - DRVOFF, EN/IN1 pins controlled by controller, PH/IN2 pin tied low
  - IPROPI pin monitored by controller, nFAULT pin monitoring optional
  - Configurations: PH/EN mode, SPI_IN unlocked with
    - DRVOFF_SEL = 1'b0 (Pin and register control for redundant shutoff)
    - EN_IN1_SEL = 1'b1 (Pin only control for PWM)
    - PH_IN2_SEL = 1'b0 (Register only control for direction)
- HW variant:
- – nSLEEP, DRVOFF, EN/IN1, PH/IN2 pins controlled by controller
  - nFAULT and IPROPI pins monitored by controller
  - Configuration: PWM mode

4.1 HW Variant in VQFN-RHL Package

Figure 4-2 shows the pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the DRV8242-Q1 data sheet.

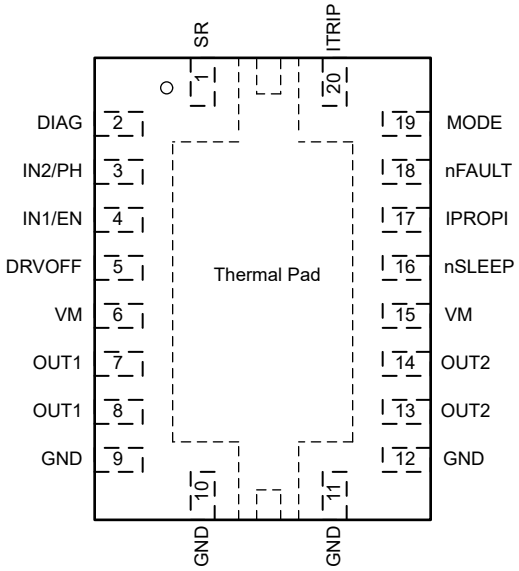

Figure 4-2. HW Variant

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
1	SR	Wrong SR configuration possible, EM performance may be affected.	B
2	DIAG	Wrong load and fault response configuration possible.	B
3	IN2/PH	Normal function as register bit is used for direction control.	D
4	IN1/EN	Load will be in re-circulation (braking). No risk of spin direction reversal.	B
5	DRVOFF	Pin based shutoff function is lost.	B
6, 15	VM	Device is powered off with driver Hi-Z.	B
7, 8	OUT1	If OUT1 is commanded to be pulled high, short is detected and outputs are Hi-Z.	B
9-12	GND	Normal function.	D
13, 14	OUT2	If OUT2 is commanded to be pulled high, short is detected and outputs are Hi-Z.	B
16	nSLEEP	Device will be in SLEEP state and outputs are Hi-Z.	B
17	IPROPI	IPROPI feedback is lost. ITRIP regulation, if enabled, is also lost.	B
18	nFAULT	False fault signalling possible. Device will continue to operate as commanded.	B
19	MODE	Wrong MODE configuration possible.	B
20	ITRIP	Incorrect ITRIP level for current regulation possible.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
1	SR	Wrong SR configuration possible, EM performance may be affected.	B
2	DIAG	Wrong load and fault response configuration possible.	B
3	IN2/PH	Normal function as register bit is used for direction control.	D
4	IN1/EN	Load will be in re-circulation (braking). No risk of spin direction reversal.	B
5	DRVOFF	Pin based shutoff is triggered and outputs are Hi-Z.	B
6, 15	VM	Device is powered off with driver Hi-Z.	B
7, 8	OUT1	Load drive capability is lost.	B
9-12	GND	Device is powered off with driver Hi-Z.	B
13, 14	OUT2	Load drive capability is lost.	B
16	nSLEEP	Device will be in SLEEP state and outputs are Hi-Z.	B
17	IPROPI	IPROPI feedback is lost. Load will be forced to recirculate if ITRIP regulation is enabled.	B
18	nFAULT	False fault signaling possible. Device will continue to operate as commanded.	B
19	MODE	Normal function.	B
20	ITRIP	Incorrect ITRIP level for current regulation possible.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Short between pins		Description of Potential Failure Effect(s)	Failure Effect Class
nFAULT	MODE	False fault signaling possible. MODE setting is not affected.	B
IPROPI	nFAULT	False fault signaling possible. IPROPI feedback is inaccurate. ITRIP regulation levels, if enabled, will be lower.	B
nSLEEP	IPROPI	IPROPI feedback is inaccurate. ITRIP regulation levels, if enabled, will be lower.	B
VM	nSLEEP	SLEEP functionality is lost.	B
OUT2	VM	If OUT2 is commanded to be pulled low, short is detected and outputs are Hi-Z.	B
GND	OUT2	If OUT2 is commanded to be pulled high, short is detected and outputs are Hi-Z.	B
OUT1	GND	If OUT1 is commanded to be pulled high, short is detected and outputs are Hi-Z.	B
VM	OUT1	If OUT1 is commanded to be pulled low, short is detected and outputs are Hi-Z	B
DRVOFF	VM	Outputs are Hi-Z.	B
EN/IN1	DRVOFF	Outputs are either Hi-Z or load is in re-circulation state.	B
PH/IN2	EN/IN1	External PWM control is lost. Internal ITRIP regulation is OK. No risk of spin direction reversal.	D
DIAG	PH/IN2	Normal function as register bit is used for direction control.	D
SR	DIAG	Wrong configuration - EM performance may be affected. Load and fault response may be incorrect.	B
ITRIP	SR	Wrong configuration - EM performance may be affected. Incorrect ITRIP level for current regulation possible.	B
MODE	ITRIP	Wrong configuration possible- Both MODE and ITRIP settings are affected.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VM

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
1	SR	Device damage possible.	A
2	DIAG	Device damage possible.	A
3	IN2/PH	Device damage possible.	A
4	IN1/EN	Device damage possible.	A
5	DRVOFF	Outputs are Hi-Z.	B
6, 15	VM	Normal function.	D
7, 8	OUT1	If OUT1 is commanded to be pulled low, short is detected and outputs are Hi-Z.	B
9-12	GND	Device is powered off with driver Hi-Z.	B
13, 14	OUT2	If OUT2 is commanded to be pulled low, short is detected and outputs are Hi-Z.	B
16	nSLEEP	SLEEP functionality is lost.	B
17	IPROPI	Device damage possible.	A
18	nFAULT	Device damage possible.	A
19	MODE	Device damage possible.	A
20	ITRIP	Device damage possible.	A

4.2 SPI "S" and"P" Variant in VQFN-RHL Package

Figure 4-3 shows the pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the DRV8242-Q1 data sheet.

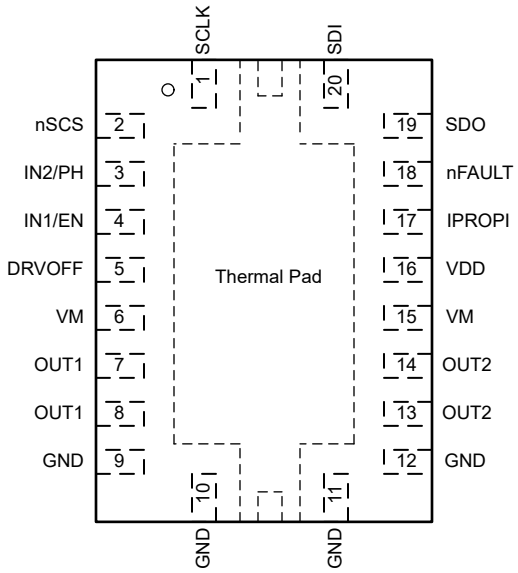

Figure 4-3. SPI "P" Variant

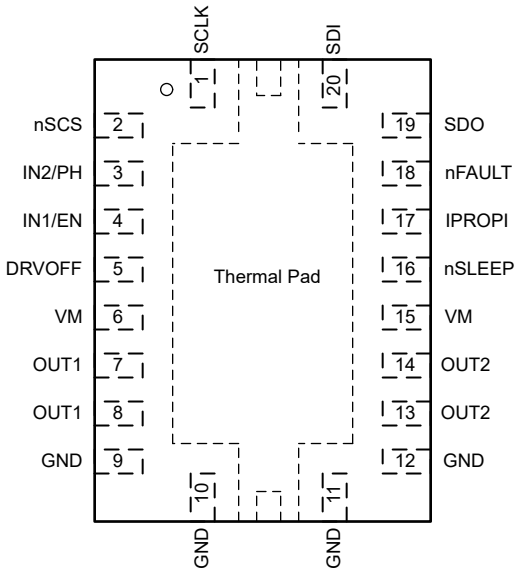

Figure 4-4. SPI "S" variant

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
1	SCLK	SPI communication is lost.	B
2	nSCS	SPI communication is lost.	B
3	IN2/PH	Normal function as register bit is used for direction control.	D
4	IN1/EN	Load will be in re-circulation (braking). No risk of spin direction reversal.	B
5	DRVOFF	Pin based shutoff function is lost.	B
6, 15	VM	Device is powered off with driver Hi-Z.	B
7, 8	OUT1	If OUT1 is commanded to be pulled high, short is detected and outputs are Hi-Z.	B
9-12	GND	Normal function.	D
13, 14	OUT2	If OUT2 is commanded to be pulled high, short is detected and outputs are Hi-Z.	B
16	nSLEEP/VDD	Device will be in SLEEP state and outputs are Hi-Z.	B
17	IPROPI	IPROPI feedback is lost. ITRIP regulation, if enabled, is also lost.	B
18	nFAULT	False fault signalling possible. Device will continue to operate as commanded.	B
19	SDO	SPI communication is lost.	B
20	SDI	SPI communication is lost.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
1	SCLK	SPI communication is lost.	B
2	nSCS	SPI communication is lost.	B
3	PH/IN2	Normal function as register bit is used for direction control.	D
4	EN/IN1	Load will be in re-circulation (braking). No risk of spin direction reversal.	B
5	DRVOFF	Pin based shutoff is triggered and outputs are Hi-Z.	B
6, 15	VM	Device is powered off with driver Hi-Z.	B
7, 8	OUT1	Load drive capability is lost.	B
9, 10, 11, 12	GND	Device is powered off with driver Hi-Z.	B
13, 14	OUT2	Load drive capability is lost.	B
16	nSLEEP	Both "S" & "P" variants: Device will be in SLEEP state and outputs are Hi-Z.	B
	VDD		
17	IPROPI	IPROPI feedback is lost. Load will be forced to recirculate if ITRIP regulation is enabled.	B
18	nFAULT	False fault signaling possible. Device will continue to operate as commanded.	B
19	SDO	SPI communication is lost.	B
20	SDI	SPI communication is lost.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Short between pins		Description of Potential Failure Effect(s)	Failure Effect Class
SCLK	SDI	SPI communication is lost.	B
nSCS	SCLK	SPI communication is lost.	B
PH/IN2	nSCS	Normal function as register bit is used for direction control.	D
EN/IN1	PH/IN2	External PWM control is lost. Internal ITRIP regulation is OK. No risk of spin direction reversal.	D
DRVOFF	EN/IN1	Outputs are either Hi-Z or load is in re-circulation state.	B
VM	DRVOFF	Outputs are Hi-Z.	B
OUT1	VM	If OUT1 is commanded to be pulled low, short is detected and outputs are Hi-Z	B
GND	OUT1	If OUT1 is commanded to be pulled high, short is detected and outputs are Hi-Z.	B
OUT2	GND	If OUT2 is commanded to be pulled high, short is detected and outputs are Hi-Z.	B
VM	OUT2	If OUT2 is commanded to be pulled low, short is detected and outputs are Hi-Z.	B
nSLEEP	**VM**	"S" variant: SLEEP functionality is lost	B
VDD		**"P" variant: Device damage possible. Device behavior can not be guaranteed.**	**A**
IPROPI	nSLEEP	"S" variant: IPROPI feedback is inaccurate. ITRIP regulation levels, if enabled, will be lower.	B
	VDD	"P" variant: IPROPI feedback is inaccurate. Outputs are Hi-Z if ITRIP regulation is enabled.	
nFAULT	IPROPI	False fault signaling possible. IPROPI feedback is inaccurate. ITRIP regulation levels, if enabled, will be lower.	B
SDO	nFAULT	False fault signaling possible. SPI communication will be affected during fault assertion.	B
SDI	SDO	SPI communication is lost.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply VM

Pin		Description of Potential Failure Effect(s)	Failure Effect Class
No.	Name		
1	SCLK	Device damage possible.	A
2	nSCS	Device damage possible.	A
3	PH/IN2	Device damage possible.	A
4	EN/IN1	Device damage possible.	A
5	DRVOFF	Outputs are Hi-Z.	B
6, 15	VM	Normal function.	D
7, 8	OUT1	If OUT1 is commanded to be pulled low, short is detected and outputs are Hi-Z.	B
9, 10, 11, 12	GND	Device is powered off with driver Hi-Z.	B
13, 14	OUT2	If OUT2 is commanded to be pulled low, short is detected and outputs are Hi-Z.	B
16	nSLEEP	"S" variant: SLEEP functionality is lost.	B
	VDD	"P" variant: Device damage possible.	A
17	IPROPI	Device damage possible.	A
18	nFAULT	Device damage possible.	A
19	SDO	Device damage possible.	A
20	SDI	Device damage possible.	A

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