Functional Safety Information

TLVM365R15, TLVM365R1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TLVM365R15 and TLVM365R1 (RDN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

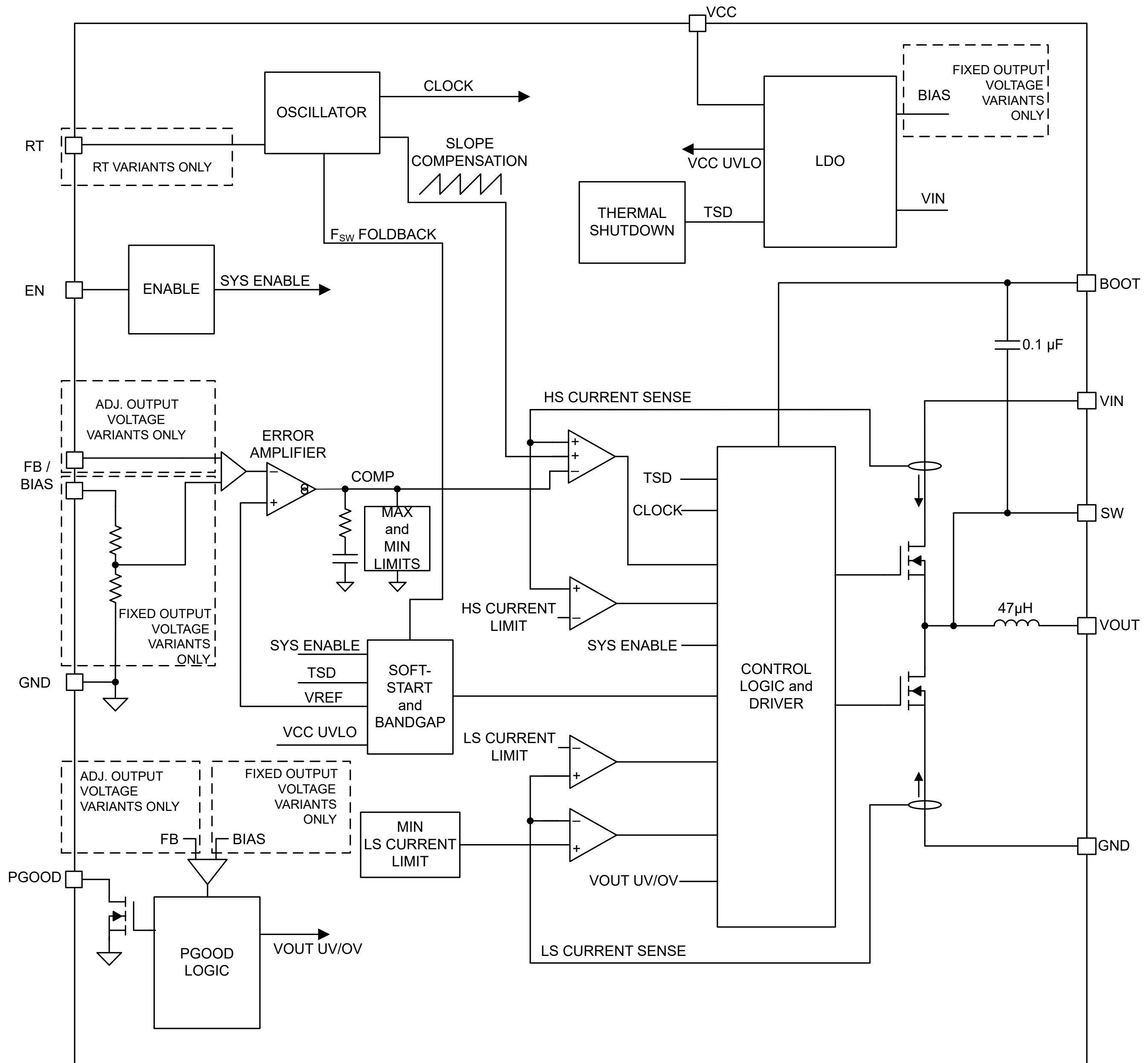

Figure 1-1. Functional Block Diagram

TLVM365R15 and TLVM365R1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 TLVM365R15

This section provides Functional Safety Failure In Time (FIT) rates for TLVM365R15 and TLVM365R1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	27
Die FIT Rate	4
Package FIT Rate	23

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 195 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/ BICMOS ASICs Analog & Mixed HV > 50-V supply	30 FIT	75°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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2.2 TLVM365R1

This section provides Functional Safety Failure In Time (FIT) rates for TLVM365R15 and TLVM365R1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	25
Die FIT Rate	3
Package FIT Rate	22

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 140 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/ BICMOS ASICs Analog & Mixed HV > 50-V supply	30 FIT	75°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLVM365R15 and TLVM365R1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No Output Voltage	60%
Output not in specification - voltage or timing	30%
Power Good - False Trip or Failure to Trip	5%
Short Circuit any two pins	5%

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLVM365R15 and TLVM365R1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

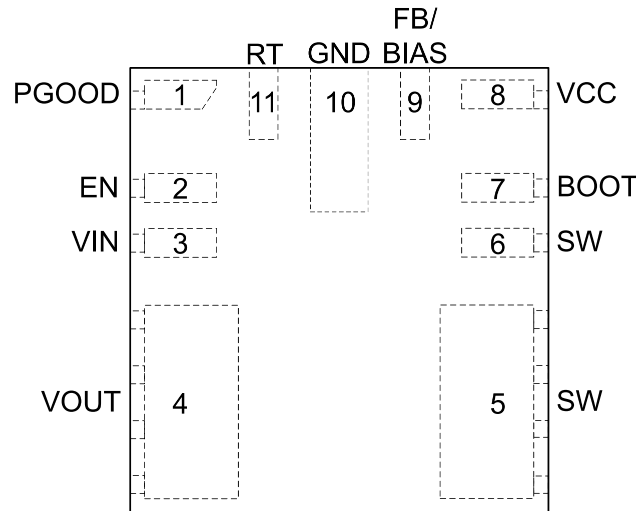
- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TLVM365R15 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TLVM365R15 data sheet.



1. Pin 1 trimmed and factory-set for externally adjustable switching frequency RT variants only.
2. Pin 9 trimmed and factory-set for fixed output voltage or adjustable output voltage. See the *data sheet* for more details.

Figure 4-1. Pin Diagram

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGOOD	1	When not in use, this pin can be left open or grounded. However, PGOOD is no longer reliably relays Power-Good information to devices connected to this pin.	B
EN	2	VOUT = 0 V, device is disabled.	B
VIN	3	VOUT = 0 V.	B
VOUT	4	Goes into hiccup, short-circuit operation.	B
SW	5, 6	Damage occurs.	A
BOOT	7	VOUT = 0 V, HS FET does not turn on.	B
VCC	8	VOUT = 0 V.	B
FB/BIAS	9	VOUT = 0 V.	B
GND	10	Normal operation.	D
RT	11	For RT, the switching frequency is set to 2.2 MHz.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGOOD	1	When not in use, this pin can be left open or grounded. However, PGOOD is no longer reliably relays Power-Good information to devices connected to this pin.	B
EN	2	VOUT behavior is not defined. VOUT may be 0 V, but it also may be up. Do not float this pin. Device can no longer reliably be enabled or disabled by other devices connected to this pin.	B
VIN	3	VOUT = 0 V.	B
VOUT	4	VOUT = 0 V.	B
SW	5, 6	Normal operation.	D
BOOT	7	Normal operation.	D
VCC	8	VCC output is unstable, can increase above 5.5 V	A
FB/BIAS	9	VOUT = 0 V. Do not float this pin.	B
GND	10	VOUT can be abnormal, as reference voltage is not fixed.	B
RT	11	If it is RT device, then frequency is not defined. VOUT is up, but only partially functional.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
PGOOD	1	EN	If EN > 20 V, it damages devices connected to the PGOOD pin.	A
EN	2	VIN	VOUT normal (enable is on, all other blocks work). However, the device can no longer be disabled.	B
VIN	3	VOUT	If VIN >16 V, damage occurs.	A
VOUT	4	SW	Damage occurs.	A
SW	6	BOOT	VOUT = 0 V, HS does not turn on, no Cboot.	B
BOOT	7	VCC	Damage occurs to VCC LDO. The VCC LDO could no longer supply voltage to internal control circuits.	A
VCC	8	FB	Can be partially nonfunctional, no damage occurs.	B
FB/BIAS	9	GND	VOUT = 0 V (for fixed option) switches at maximum duty cycle for ADJ option.	B
GND	10	RT or MODE	For RT, Switching Frequency is set to 2.2 MHz. For MODE/SYNC the device goes into PFM mode.	B

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
RT	11	PGOOD	If PGOOD is high and < 5.5 V, then Fsw = 1 MHz. If PGOOD is low, then Fsw = 2.2 MHz for RT. PGOOD absmax being 20 V, RT ESD damages if PG goes to 20 V.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGOOD	1	If VIN > 20 V, it damages PGOOD. PGOOD is no longer reliably relays Power-Good information to devices connected to this pin.	A
EN	2	VOUT normal (enable is on, all other blocks work). However, the device can no longer be disabled.	B
VIN	3	Normal operation.	D
VOUT	4	Damage occurs, if VIN > 16 V.	A
SW	5, 6	Damage occurs.	A
BOOT	7	Damage occurs, the BOOT ESD clamp is damaged.	A
VCC	8	If Vin > 5.5 V, damage occurs.	A
FB/BIAS	9	If VIN > 20 V, damage occurs.	A
GND	10	VOUT = 0 V.	A
RT	11	If Vin > 5.5 V, damage occurs. If Vin < 5.5 V, switching frequency is 1 MHz.	A

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