Functional Safety Information

TPS3808E-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TPS3808E-Q1 (DYY package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

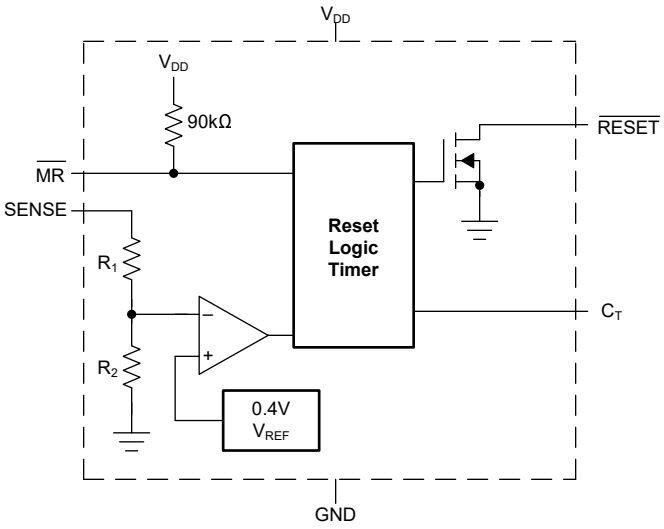

Figure 1-1. Functional Block Diagram

TPS3808E-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS3808E-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	3
Package FIT Rate	3

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 60mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS3808E-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
RESET / fails to trip	22%
RESET / false trip	40%
RESET / trip outside specification (voltage or time)	22%
RESET / delay outside specification	16%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS3808E-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Table 4-1 shows the TPS3808E-Q1 pin diagram. For a detailed description of the device pins please refer to *TPS3760-Q1* in the *Pin Configuration and Functions* section of the data sheet.

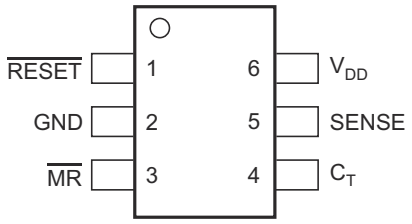

Figure 4-1. Pin Diagram DYY Package 14-Pin SOT-23

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- At $V_{DD\ (MIN)} \leq VDD \leq V_{DD\ (MAX)}$
- $\overline{MR}$ = Open, C_T = Open,
- Output reset Pullup Resistor (R_{PULLUP}) = 10kΩ, Output reset pullup voltage (V_{PULLUP} = 3.5V
- Sense is monitoring VDD
- Typical values are at T_A = 25°C, V_{DD} = 3.5V, C_{VDD}=0.1µF, and V_{IT} = 3.3V unless stated otherwise.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
$\overline{\text{RESET}}$	1	Forces RESET to be held low.	B
GND	2	No damage to device. No impact to functionality.	D
$\overline{\text{MR}}$	3	RESET will be asserted.	B
CT	4	RESET is latched low if an undervoltage condition occurs.	B
SENSE	5	RESET will be asserted.	B
VDD	6	VDD short to GND, Device has no power for normal operation	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
$\overline{\text{RESET}}$	1	Reset functionality will be lost since it's not being pulled up to VDD.	B
GND	2	Device is unpowered.	B
$\overline{\text{MR}}$	3	Normal operation.	D
CT	4	Normal operation.	D
SENSE	5	No damage to the device. Reset is asserted.	B
VDD	6	Device is unpowered.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

PIN NAME	PIN NO.	SHORTED TO	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
$\overline{\text{RESET}}$	1	GND	Forces RESET to be held low.	B
GND	2	/MR	RESET will be asserted.	B
$\overline{\text{MR}}$	3	CT	RESET is latched low if an undervoltage condition occurs.	B
CT	4	SENSE	RESET is latched low if an undervoltage condition occurs.	B
SENSE	5	VDD	Normal operation.	D
VDD	6	/RESET	Large current can flow into RESET when in error condition. This can cause permanent damage.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
$\overline{\text{RESET}}$	1	Large current can flow into RESET when in error condition. This can cause permanent damage.	A
GND	2	Device has no power for normal operation	B
$\overline{\text{MR}}$	3	Normal operation.	D
CT	4	RESET is latched low if an undervoltage condition occurs.	B
SENSE	5	Normal operation.	D
VDD	6	Normal operation.	D

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