*Functional Safety Information*

# *LM67640-Q1, LM67660-Q1 and LM67680-Q1 Functional Safety FIT Rate, FMD and Pin FMA*

## Table of Contents


**1 Overview** ..... 2
**2 Functional Safety Failure In Time (FIT) Rates** ..... 3
**3 Failure Mode Distribution (FMD)** ..... 4
**4 Pin Failure Mode Analysis (Pin FMA)** ..... 5
**5 Revision History** ..... 9


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# 1 Overview

This document contains information for the LM676X0-Q1 (WQFN-FCRLF, 26-pin package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

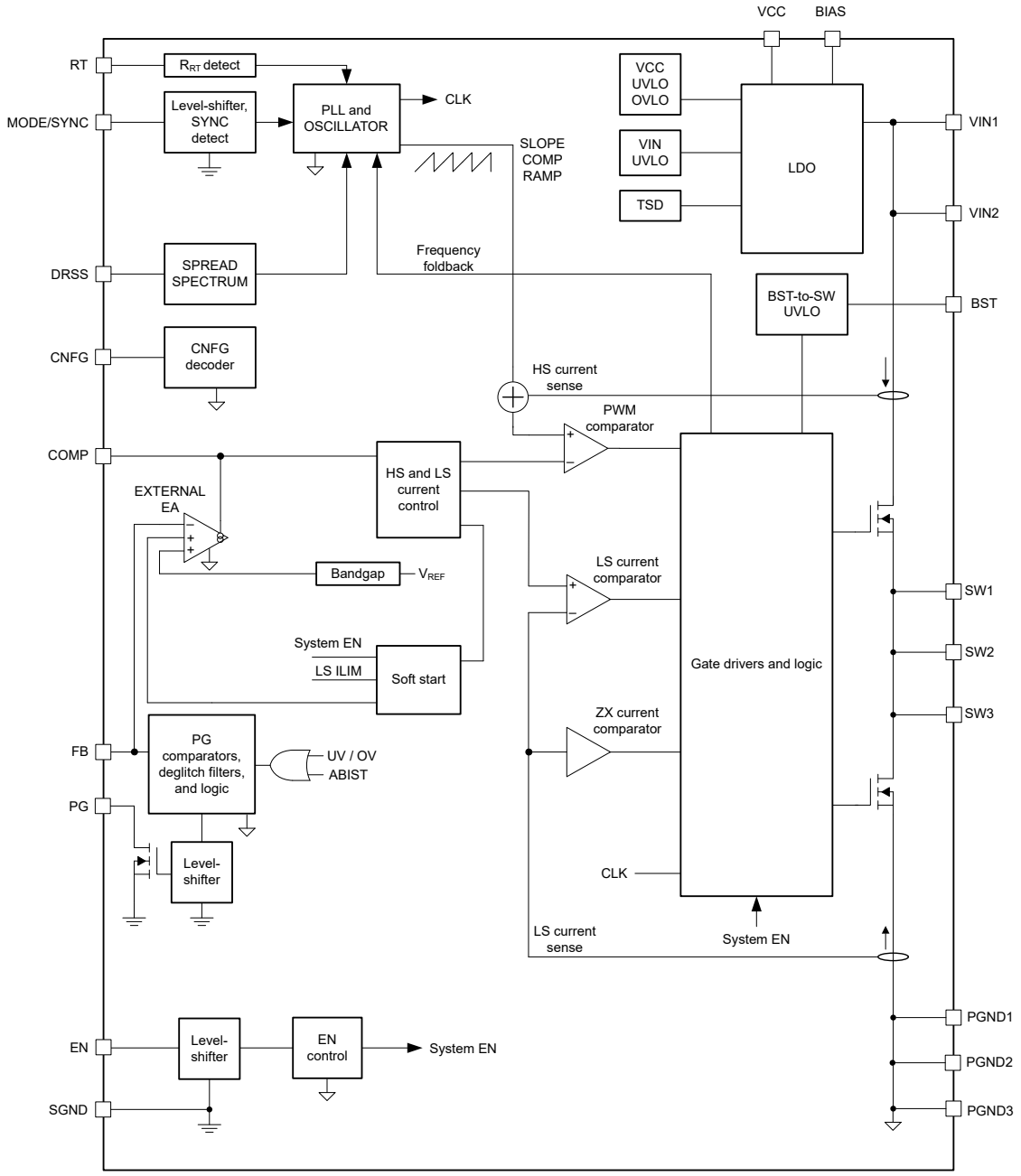


**Figure 1-1. Functional Block Diagram**

LM676X0-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.



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## 2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LM676X0-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) | | |
|---|---|---|---|
| | LM67680-Q1 | LM67660-Q1 | LM67640-Q1 |
| Total component FIT rate | 27 | 20 | 17 |
| Die FIT rate | 12 | 6 | 4 |
| Package FIT rate | 15 | 14 | 13 |

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation for LM67680-Q1: 2.8W
- Power dissipation for LM67660-Q1: 1.5W
- Power dissipation for LM67640-Q1: 0.7W
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS, BICMOS<br>ASICs analog and mixed HV > 50V supply | 25 FIT | 55°C |

The reference FIT rate and reference virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.


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# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM676X0-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| No output voltage | 50 |
| Output voltage not in specification | 40 |
| Power FET stuck on | 5 |
| PG false trip, fails to trip | 5 |



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# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM676X0-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality. |
| B | No device damage, but loss of functionality. |
| C | No device damage, but performance degradation. |
| D | No device damage, no impact to functionality or performance. |

Figure 4-1 shows the LM676X0-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM676X0-Q1 datasheet.

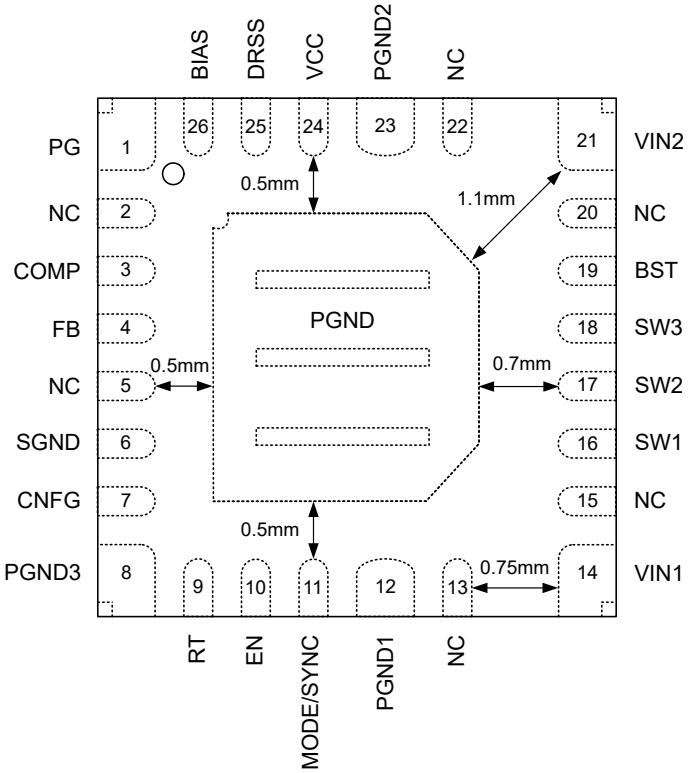


**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The application circuit is configured according to the LM676X0-Q1 datasheet.


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**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (SGND)**

| Pin Name | Pin No | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| PG | 1 | There is a loss of power good functionality. | B |
| NC | 2 | The device operates as normal. | D |
| | 5 | | |
| | 13 | | |
| | 15 | | |
| | 20 | | |
| | 22 | | |
| COMP | 3 | The device is damaged if $\|V_{PGND}\|$ > 5.5V. | A |
| FB | 4 | The device is damaged if $\|V_{PGND}\|$ > 5.5V. | A |
| SGND | 6 | The device operates as normal. | D |
| CNFG | 7 | The device is damaged if $\|V_{PGND}\|$ > 5.5V. | A |
| PGND1, PGND2, PGND3 | 8 | There is a loss of regulation. $V_{OUT}$ = 0V. | B |
| | 12 | | |
| | 23 | | |
| RT | 9 | When fixed at 400kHz, there is a loss of regulation. $V_{OUT}$ = 0V. | B |
| | | When fixed at 2.2MHz, the device is damaged if $\|V_{PGND}\|$ > 5.5V. | A |
| | | When the frequency is adjustable, the performance of the device degrades. The switching frequency is undetermined. | C |
| EN | 10 | The device disables. $V_{OUT}$ = 0V. | B |
| MODE/SYNC | 11 | When in AUTO mode, the device operates as normal. | D |
| | | When in FPWM mode, there is a loss of regulation. $V_{OUT}$ = 0V. | B |
| | | When in external SYNC, there is a loss of synchronization. The performance of the device degrades. The device operates in AUTO mode. | C |
| VIN1, VIN2 | 14 | $V_{OUT}$ = 0V | B |
| | 21 | | |
| SW1, SW2, SW3 | 16 | The device is damaged. | A |
| | 17 | | |
| | 18 | | |
| BST | 19 | There is a loss of regulation. $V_{OUT}$ = 0V. | B |
| VCC | 24 | The device is damaged if $\|V_{PGND}\|$ > 5.5V. | A |
| DRSS | 25 | The DRSS selection is undetermined. The performance of EMI degrades. | C |
| BIAS | 26 | When the BIAS pin is tied to PGND, there is a loss of regulation. $V_{OUT}$ = 0V. | B |
| | | When the BIAS pin is tied to SGND, the device operates as normal. | D |



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**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| PG | 1 | There is a loss of power good functionality. | B |
| NC | 2 | The device operates as normal. | D |
| | 5 | | |
| | 13 | | |
| | 15 | | |
| | 20 | | |
| | 22 | | |
| COMP | 3 | There is a loss of regulation. | B |
| FB | 4 | When $V_{OUT}$ is adjustable, there is a loss of regulation. | B |
| SGND | 6 | The performance degradation of the device is dependent on the conditions of the application. | C |
| CNFG | 7 | There is a loss of regulation. $V_{OUT}$ = 0V. | B |
| PGND1, PGND2, PGND3 | 8 | The performance of the device degrades. | C |
| | 12 | | |
| | 23 | | |
| RT | 9 | When fixed at 400kHz, there is a loss of regulation. The device switches at 2.2MHz. | C |
| | | When fixed at 2.2MHz, the device operates as normal. | C |
| | | When the frequency is adjustable, the performance of the device degrades. The device switches at 2.2MHz. | C |
| EN | 10 | The device disables. $V_{OUT}$ = 0V. | B |
| MODE/SYNC | 11 | When in AUTO mode, the device operates as normal. | D |
| | | When in FPWM mode, the performance of the device degrades. The device operates in AUTO mode. | C |
| | | When in external SYNC, there is a loss of synchronization. The performance of the device degrades. The device operates in AUTO mode. | C |
| VIN1, VIN2 | 14 | The performance degradation of the device is dependent on the conditions of the application. | C |
| | 21 | | |
| SW1, SW2, SW3 | 16 | The performance degradation of the device is dependent on the conditions of the application. | C |
| | 17 | | |
| | 18 | | |
| BST | 19 | There is a loss of regulation. $V_{OUT}$ = 0V. | B |
| VCC | 24 | The LDO operation is unstable, there is a loss of regulation. | B |
| DRSS | 25 | The DRSS pin is enabled and slew rate control is enabled. The device operates as normal. | D |
| BIAS | 26 | When the BIAS pin is tied to $V_{OUT}$, the performance of the device degrades. There is a higher no-load $I_Q$. | C |
| | | When the BIAS pin is tied to SGND, the device operates as normal. | D |


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**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Adjacent Pin | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| PG | NC | The device operates as normal. | D |
| NC | COMP | The device operates as normal. | D |
| COMP | FB | There is a loss of regulation. There is an overvoltage condition. | B |
| FB | NC | The device operates as normal. | D |
| NC | SGND | The device operates as normal. | D |
| SGND | CNFG | The device is damaged if SGND to CNFG > 5.5V. | A |
| CNFG | PGND3 | There is a loss of regulation. $V_{OUT}$ = 0V. | B |
| PGND3 | RT | When the RT pin is tied to GND, the device operates as normal. | D |
| | | When the RT pin is tied to VCC, there is a loss of regulation. $V_{OUT}$ = 0V. | B |
| | | When the RT pin is pulled to GND with a resistor, the performance of the device degrades. | C |
| RT | EN | When the RT pin is tied to GND and the EN pin is tied to VIN, there is a loss of regulation. $V_{OUT}$ = 0. | B |
| | | When the RT pin is tied to VCC and the EN pin tied to VIN, the device is damaged. | A |
| | | When the RT pin is pulled to GND with a resistor and the EN pin is tied to VIN, the performance of the device degrades. | C |
| EN | MODE/ SYNC | When the MODE/SYNC pin is tied to GND and the EN pin is tied to VIN, the device is damaged if EN > 5.5V. | A |
| MODE/SYNC | PGND1 | When in AUTO mode, the device operates as normal. | D |
| | | When in FPWM mode, there is a loss of regulation. $V_{OUT}$ = 0V. | |
| | | When in external SYNC, there is a loss of synchronization. The performance of the device degrades. The device operates in AUTO mode. | |
| PGND1 | NC | The device operates as normal. | D |
| NC | VIN1 | The device operates as normal. | D |
| VIN1 | NC | The device operates as normal. | D |
| NC | SW1 | The device operates as normal. | D |
| SW1 | SW2 | The device operates as normal. | D |
| SW2 | SW3 | The device operates as normal. | D |
| SW3 | BST | The device operates as normal. | B |
| BST | NC | The device operates as normal. | D |
| NC | VIN2 | The device operates as normal. | D |
| VIN2 | NC | The device operates as normal. | D |
| NC | PGND2 | The device operates as normal. | D |
| PGND2 | VCC | There is a loss of regulation. $V_{OUT}$ = 0V. | B |
| VCC | DRSS | When the DRSS pin is tied to VCC, the device operates as normal. | D |
| | | When the DRSS pin is tied to PGND, there is a loss of regulation. $V_{OUT}$ = 0V. | B |
| | | When the DRSS pin is pulled to PGND with a resistor, the performance of the device degrades. | C |
| DRSS | BIAS | When the DRSS pin is tied to PGND and the BIAS pin is tied to GND, the device operates as normal. | D |
| | | When the DRSS pin is tied to VCC and the BIAS pin is tied to GND, there is a loss of regulation. $V_{OUT}$ = 0V. | B |
| | | When the DRSS pin is pulled to PGND with a resistor and the BIAS pin is tied to GND, the performance of the device degrades. | C |
| | | When the DRSS pin is tied to PGND and the BIAS pin is tied to $V_{OUT}$, there is a loss of regulation. | B |
| | | When the DRSS pin is tied to VCC and the BIAS pin is tied to $V_{OUT}$ (<5V), the device operates as normal. | D |
| | | When the DRSS pin is tied to VCC and the BIAS pin is tied to $V_{OUT}$ (>5V), the device is damaged. | A |
| | | When the DRSS pin is pulled to GND with a resistor and the BIAS pin is tied to $V_{OUT}$, the performance of the device degrades. | C |


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**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

| Pin Name | Adjacent Pin | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| BIAS | NC | The device operates as normal. | D |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply ($V_{IN}$)**

| Pin Name | Pin No | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| PG | 1 | The device is damaged if $V_{IN}$ > 5.5V. | A |
| NC | 2 | The device operates as normal. | D |
| | 5 | | |
| | 13 | | |
| | 15 | | |
| | 20 | | |
| | 22 | | |
| COMP | 3 | The device is damaged if $V_{IN}$ > 5.5V. | A |
| FB | 4 | The device is damaged if $V_{IN}$ > 5.5V. | A |
| SGND | 6 | There is a loss of regulation. $V_{OUT}$ = 0V. | B |
| CNFG | 7 | The device is damaged if $V_{IN}$ > 5.5V. | A |
| PGND1, PGND2, PGND3 | 8 | There is a loss of regulation. $V_{OUT}$ = 0V. | B |
| | 12 | | |
| | 23 | | |
| RT | 9 | The performance of the device degrades. The switching frequency is undefined. | C |
| EN | 10 | The device operates as normal. | D |
| MODE/SYNC | 11 | The device is damaged if $V_{IN}$ > 5.5V. | A |
| VIN1, VIN2 | 14 | The device operates as normal. | D |
| | 21 | | |
| SW1, SW2, SW3 | 16 | The device is damaged. | A |
| | 17 | | |
| | 18 | | |
| BST | 19 | The device is damaged. | A |
| VCC | 24 | The device is damaged if $V_{IN}$ > 5.5V. | A |
| DRSS | 25 | The device is damaged if $V_{IN}$ > 40V. | A |
| BIAS | 26 | The device is damaged if $V_{IN}$ > 40V. | A |

# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| December 2025 | * | Initial Release |


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Last updated 10/2025