Application Report

Functional Safety Manual for TCAN1144-Q1 and TCAN1146-Q1

ABSTRACT

Table A-2 summarizes the functional safety mechanisms present in hardware or recommend for implementation in software or at the system level as described in Section 7. Table A-1 describes each column in Table A-2 and gives examples of what content could appear in each cell.

Table A-1. Legend of Functional Safety Mechanisms

Functional Safety Mechanism	Description
TI Safety Mechanism Unique Identifier	A unique identifier assigned to this safety mechanism for easier tracking.
Safety Mechanism Name	The full name of this safety mechanism.
Safety Mechanism Category	**Safety Mechanism** - This test provides coverage for faults on the primary function. It may also provide coverage on another safety mechanism. **Test for Safety Mechanism** - This test provides coverage for faults of a safety mechanism only. It does not provide coverage on the primary function. **Fault Avoidance** - This is typically a feature used to improve the effectiveness of a related safety mechanism.
Safety Mechanism Type	Can be either hardware, software, a combination of both hardware and software, or system. See Section 8.2 for more details.
Safety Mechanism Operation Interval	The timing behavior of the safety mechanism with respect to the test interval defined for a functional safety requirement / functional safety goal. Can be either continuous, or on-demand. **Continuous** - the safety mechanism constantly monitors the hardware-under-test for a failure condition. **Periodic or On-Demand** - the safety mechanism is executed periodically, when demanded by the application. This includes Built-In Self-Tests that are executed one time per drive cycle or once every few hours.
Test Execution Time	Time period required for the safety mechanism to complete, not including error reporting time. Note: Certain parameters are not set until there is a concrete implementation in a specific component. When component specific information is required, the component data sheet should be referenced. Note: For software-driven tests, the majority contribution of the Test Execution Time is often software implementation-dependent.
Action on Detected Fault	The response that this safety mechanism takes when an error is detected. Note: For software-driven tests, the Action on Detected Fault may depend on software implementation.
Time to Report	Typical time required for safety mechanism to indicate a detected fault to the system Note: For software-driven tests, the majority contribution of the Time to Report is often software implementation-dependent

Table A-2. Summary of Functional Safety Mechanisms

TI Safety Mechanism Unique Identifier	Safety Mechanism Name	Safety Mechanism Category	Safety Mechanism Type	Safety Mechanism Operation Interval	Test Execution Time	Action on Detected Fault	Time to Report
SM-1	CAN bus fault	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous - In normal mode	150 ns	interrupt bits in registers 8'h50[7], 8'h50[3] and register 8'h54[6:0] and indicates an CAN Bus fault	50 ns

Table A-2. Summary of Functional Safety Mechanisms (continued)

TI Safety Mechanism Unique Identifier	Safety Mechanism Name	Safety Mechanism Category	Safety Mechanism Type	Safety Mechanism Operation Interval	Test Execution Time	Action on Detected Fault	Time to Report
SM-2	Thermal shutdown; TSD	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous - all modes except for sleep	4.4 µs	[turn off the CAN transceiver and set the interrupt bit registers 8'h50[7], 8'h50[5] and 8'h52[1] indicating junction temperature exceeded and enters fail-safe mode or TSD protected mode	1.1 µs
SM-3	CAN bus short circuit limiter, I_{OS}	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous - all modes except for sleep	NA	Limits the current throught the CANH and CANL pins.	NA
SM-4	CAN TXD pin dominant state timeout; t_{TXD_DTO}	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous - In normal mode	3.5 ms	the device will turn off the CAN transceiver and indicate the the fault at 8'h50[7], 8'h50[6] and 8'h51[0]	1.1 µs
SM-5	VCC undervoltage; UV_{CC}	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous - all modes except for sleep	330 ms	Device enters programmed mode, sleep or fail-safe mode, sets interrupt registers 8'h50[7], 8'h50[5] and 8'h52[2] and indicates UVCC condition	1.1 µs
SM-6	VSUP supply undervoltage; UV_{SUP}	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous - all modes except for sleep	2.2 µs	Device enters programmed mode, sleep or fail-safe mode, sets interrupt registers 8'h50[7], 8'h50[5] and 8'h52[4] and indicates UVSUP condition	1.1 µs
SM-7	VIO supply undervoltage; UV_{IO}	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous - all modes except for sleep	330 ms	Device enters programmed mode, UVIO protected or fail-safe mode, sets interrupt registers 8'h50[7], 8'h50[5] and 8'h52[3] and indicates UVIO condition back to MCU with nINT pin	1.1 µs
SM-8	Timout, Window or Q&A watchdog error - Normal mode	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous	Programmable	Increments WD error counter and if exceeded programmed value will enter programmed mode, restart or fail-safe mode, set WD interrupt and indicate back to MCU with nINT pin	1.1 µs
SM-9	SPI communication error; SPIERR	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous	50 ns after rising edge of nCS	The device shall monitor MCU SPI communication utilizing clock count check and if there are too many or not enough clock signals the MCU write to the device will be blocked and 8'h50[7], 8'h50[4] and 8'h53[7]	1.1 µs
SM-10	Scratchpad write/read	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous when VIO is present and is MCU initiated	SPI clock rate dependent as a write plus data followed by a read and data required	Using the TCAN114x scratchpad, 8'h0F[7:0], by the processor makes it possible to write and read back data to determine SPI communication is valid	NA

Table A-2. Summary of Functional Safety Mechanisms (continued)

TI Safety Mechanism Unique Identifier	Safety Mechanism Name	Safety Mechanism Category	Safety Mechanism Type	Safety Mechanism Operation Interval	Test Execution Time	Action on Detected Fault	Time to Report
SM-11	Sleep Wake Error Timer; $t_{INACTIVE}$	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous	5 min	If $t_{INACTIVE}$ times out and fail-safe mode (FSM) is enabled, the device will enter FSM and will indicate the fault at 8'h50[7], 8'h50[4] and 8'h53[5]. If not enabled, the device will enter sleep mode.	1.1 µs
SM-12	Internal memory CRC; CRC_EEPROM	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Periodic - Exiting fail-safe and sleep modes	425 µs	The device will attempt to load and CRC check the EEPROM up to eight times and if fail it will indicate the the fault at 8'h50[7], 8'h50[4] and 8'h53[0]	1.1 µs
SM-13	SCLK internal pull-up to VIO	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous	NA	Avoids floating pin	NA
SM-14	SDI internal pull-up to VIO	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous	NA	Avoids floating pin	NA
SM-15	nCS internal pull-up to VIO	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous	NA	Avoids floating pin	NA
SM-16	TXD internal pull-up to VIO	Safety Mechanism	Component Hardware Functional Safety Mechanisms	Continuous	NA	Avoids floating pin	NA
SM-17	CAN protocol	Safety Mechanism	System Functional Safety Mechanism	Periodic	NA	CAN protocol has several mechanism that will make sure the data provided is correct, like CRC. If incorrect the processor will disregard the CAN packets	NA

1 TCAN1144-Q1 and TCAN1146-Q1 Functional Safety Manual

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2 Trademarks

All trademarks are the property of their respective owners.

3 Introduction

This document is a functional safety manual for the Texas Instruments TCAN1144-Q1 and TCAN1146-Q1 component. The specific orderable part numbers supported by this functional safety manual are as follows:

- TCAN1144DQ1, TCAN1144DMTQ1 and TCAN1144DYYQ1
- TCAN1146DQ1, TCAN1146DMTQ1 and TCAN1146DYYQ1

This functional safety manual provides information needed by system developers to help in the creation of a functional safety system using a TCAN1144-Q1 or TCAN1146-Q1 component. This document includes:

- An overview of the component architecture
- The details of architecture partitions and recommended functional safety mechanisms

The following information is documented in the *[Functional Safety Analysis Report]* and is not repeated in this document:

- Summary of failure rates (FIT) of the component
- Summary of functional safety metrics of the hardware component for targeted standards (for example IEC 61508, ISO 26262, and so forth)
- Quantitative functional safety analysis (also known as FMEDA, Failure Modes, Effects, and Diagnostics Analysis) with detail of the different parts of the component, allowing for customized application of functional safety mechanisms
- Assumptions used in the calculation of functional safety metrics

The user of this document should have a general familiarity with the TCAN1144-Q1 and TCAN1146-Q1 components. For more information, refer to the data sheet. This document is intended to be used in conjunction with the pertinent data sheets, technical reference manuals, and other component documentation.

For information that is beyond the scope of the listed deliverables, contact your TI sales representative or go to http://www.ti.com.

4 TCAN114x-Q1 Hardware Component Functional Safety Capability

This section summarizes the component functional safety capability.

This hardware component:

- Was not developed according to the requirements of any functional safety standard.
- FIT rates and failure mode distributions are provided as part of the Functional Safety Analysis Report for customers to calculate random fault integrity metrics.
- Recommendations are provided in this Functional Safety Manual for external safety mechanisms that may provide coverage for component failure modes.
- TI recommends that this component is integrated into the system through the strategy of "evaluation of hardware element" (ISO 26262-8:2018 clause 13).

5 Development Process for Management of Systematic Faults

For functional safety development, it is necessary to manage both systematic and random faults. Texas Instruments follows a new-product development process for all of its components which helps to decrease the probability of systematic failures. This new-product development process is described in Section 5.1.

5.1 TI New-Product Development Process

Texas Instruments has been developing components for automotive and industrial markets since 1996. Automotive markets have strong requirements regarding quality management and product reliability. The TI new-product development process features many elements necessary to manage systematic faults. Additionally, the documentation and reports for these components can be used to assist with compliance to a wide range of standards for customer's end applications including automotive and industrial systems (e.g ISO 26262-4, IEC 61508-2).

This component was developed using TI's new product development process which has been certified as compliant to ISO 9001 / IATF 16949 as assessed by Bureau Veritas (BV).

The standard development process breaks development into phases:

- Assess
- Plan
- Create
- Validate

Figure 5-1 shows the standard process.

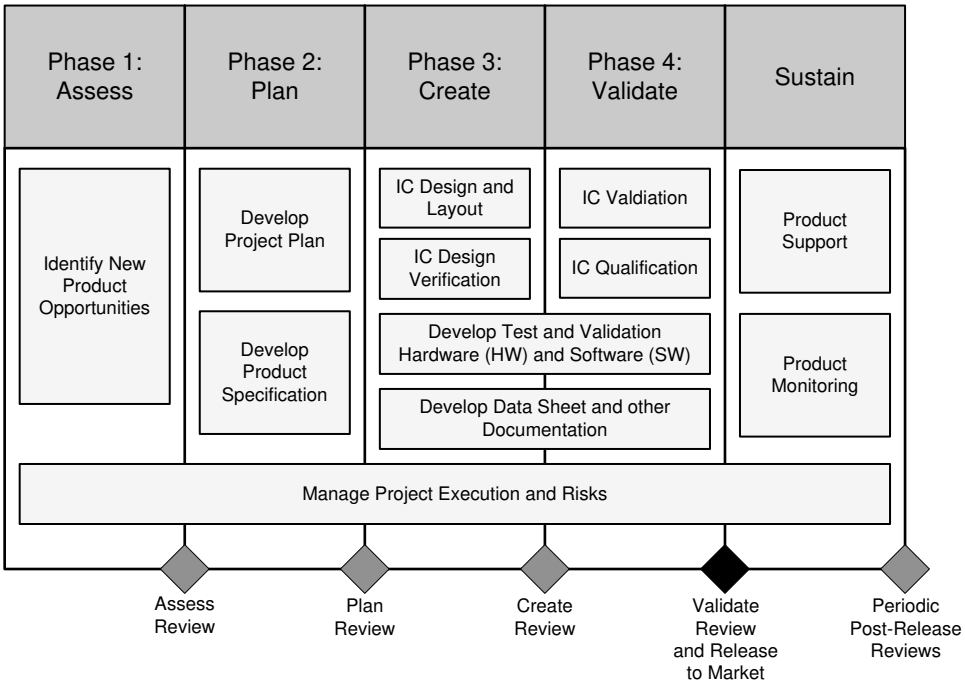

Figure 5-1. TI New-Product Development Process

6 TCAN1144-Q1 and TCAN1146-Q1 Component Overview

The TCAN1144-Q1 and TCAN1146-Q1 are enhanced high-speed CAN FD transceivers supporting data rates up to 5 Mbps. These devices are configured using serial peripheral interface (SPI) in order to use all the features available. The devices support 1.8 V to 5 V processors by applying the appropriate voltage to the VIO pin, allowing lower voltage processors to be utilized. The family of devices are register compatible enabling the system designer the flexibility to implement the features needed with minimal if any hardware and software changes.

The TCAN1144-Q1 and TCAN1146-Q1 are full featured devices supporting watchdog and advanced bus diagnostics. For ease of debug, the advanced bus fault diagnostics and communication feature can be used to pinpoint bus faults when used with other devices supporting this feature. The inhibit (INH) pin can be used to enable node power. If inhibit (INH) pin function is not required, the pin can be configured as a limp home function for when a watchdog error takes place.

The TCAN1146-Q1 supports selective wake, also known as partial networking, used in systems containing nodes that can be placed into sleep mode and reducing overall power of the system. The transceiver and selective wake function meets the specifications of the ISO11898-2:2016 standard.

Table 6-1. Device Comparison Table

Device Number	Selective Wake	Watchdog	Bus Fault Diagnostics	LIMP Home Capable
TCAN1144-Q1		X	X	X
TCAN1146-Q1	X	X	X	X

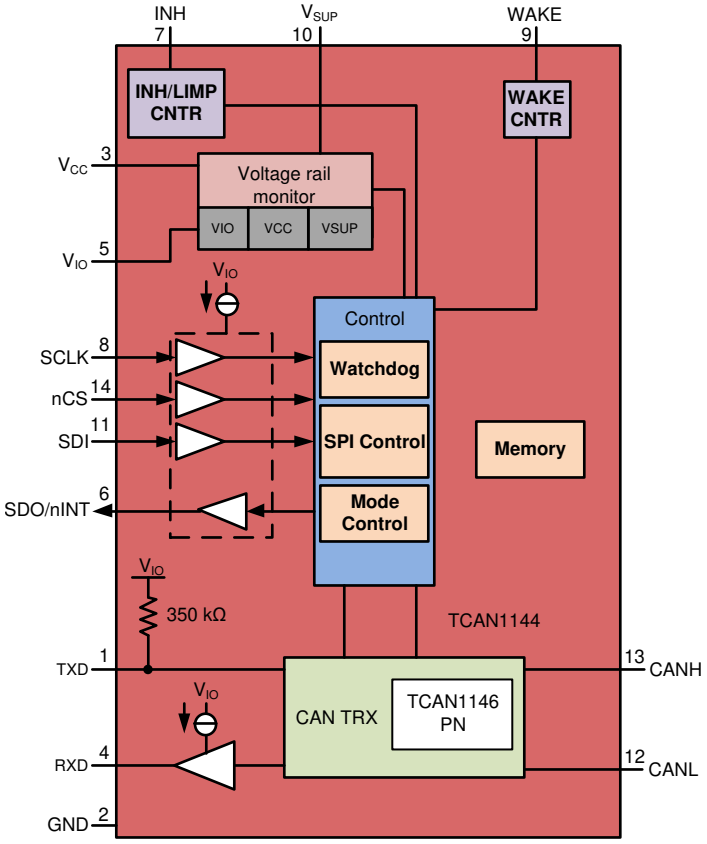

Figure 6-1. TCAN1144-Q1 and TCAN1146-Q1 Block Diagram

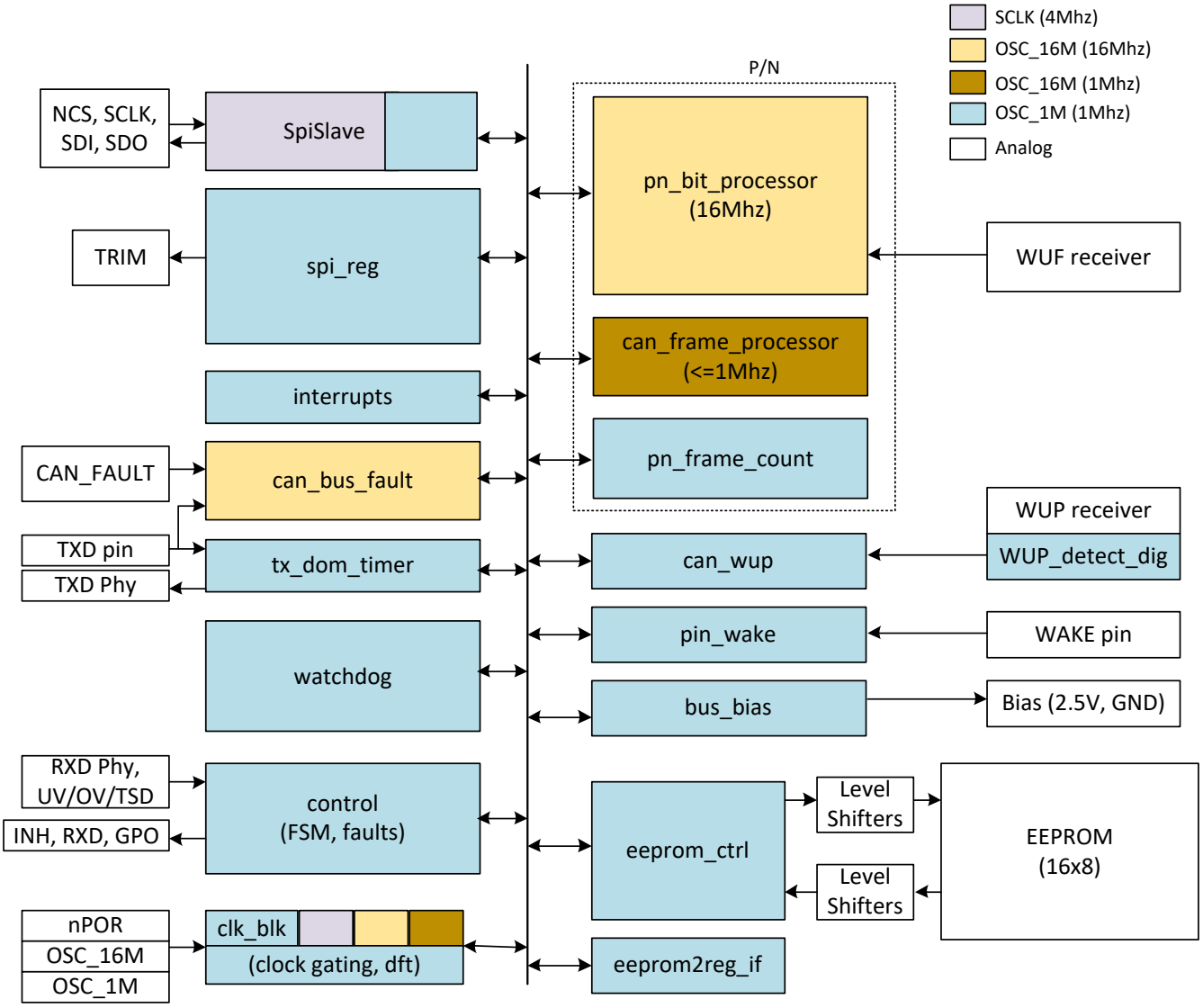

Figure 6-2. Digital Core Block Diagram and Clock Tree

6.1 Targeted Applications

The TCAN1144-Q1 and TCAN1146-Q1 components are targeted at general-purpose automotive applications that can support system level functional safety based upon quality managed criteria. This is called Safety Element out of Context (SEooC) development according to ISO 26262-10. In this case, the development is done based on assumptions on the conditions of the semiconductor component usage, and then the assumptions are verified at the system level. This method is also used to meet the related requirements of IEC 61508 at the semiconductor level. This section describes some of the target applications for this component, the component safety concept, and then describes the assumptions about the systems (also know as Assumptions of Use or AoU) that were made in performing the safety analysis.

Example target applications include, but are not limited to, the following:

- General purpose applications containing a processor and external power.

Figure 6-3 shows a generic block diagram for a general purpose system. This diagram is only an example and may not represent a complete system. Figure 6-4 provides potential failure points that have diagnostic or test ability mechanisms.

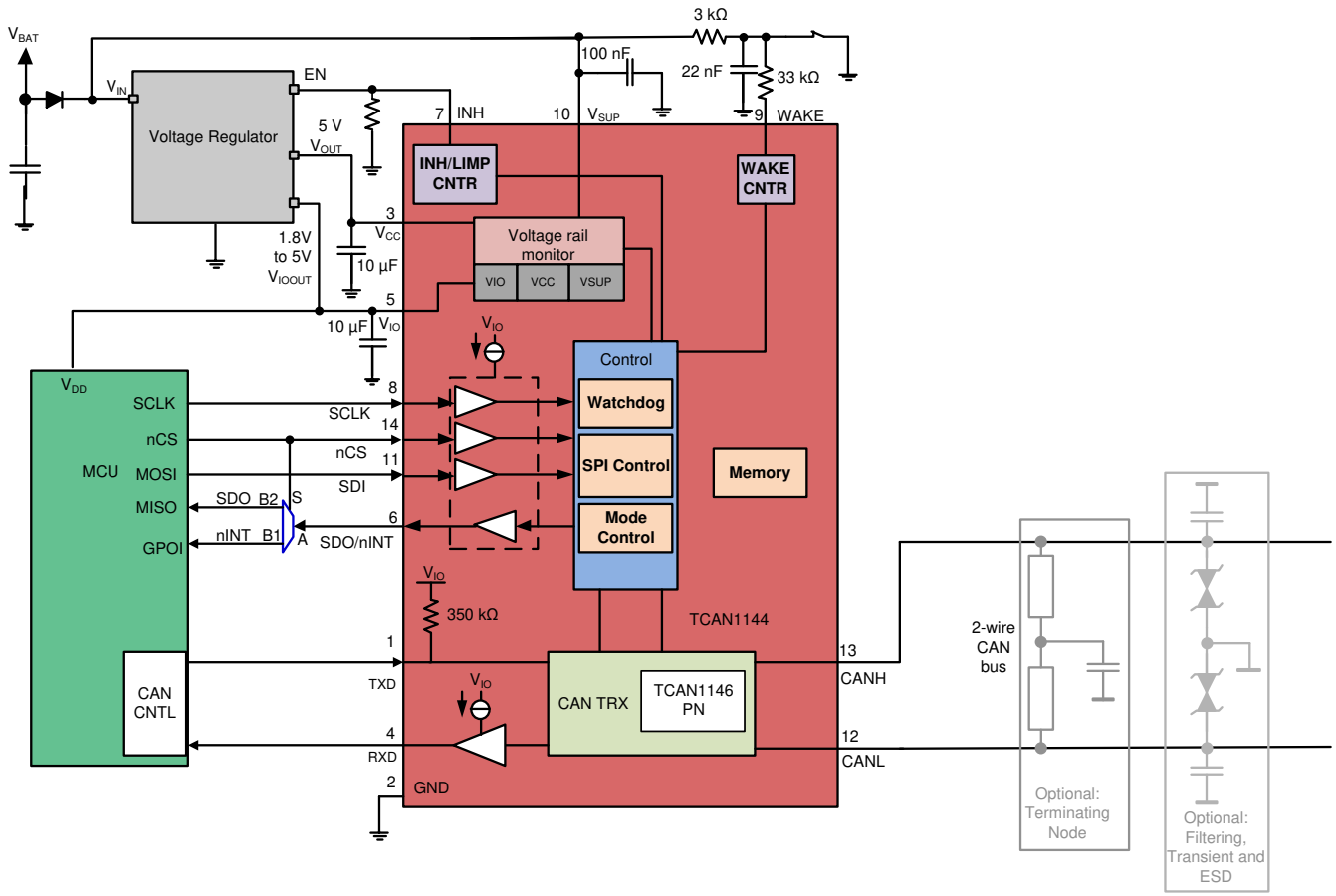

Figure 6-3. TCAN1144-Q1 and TCAN1146-Q1 General Purpose Application

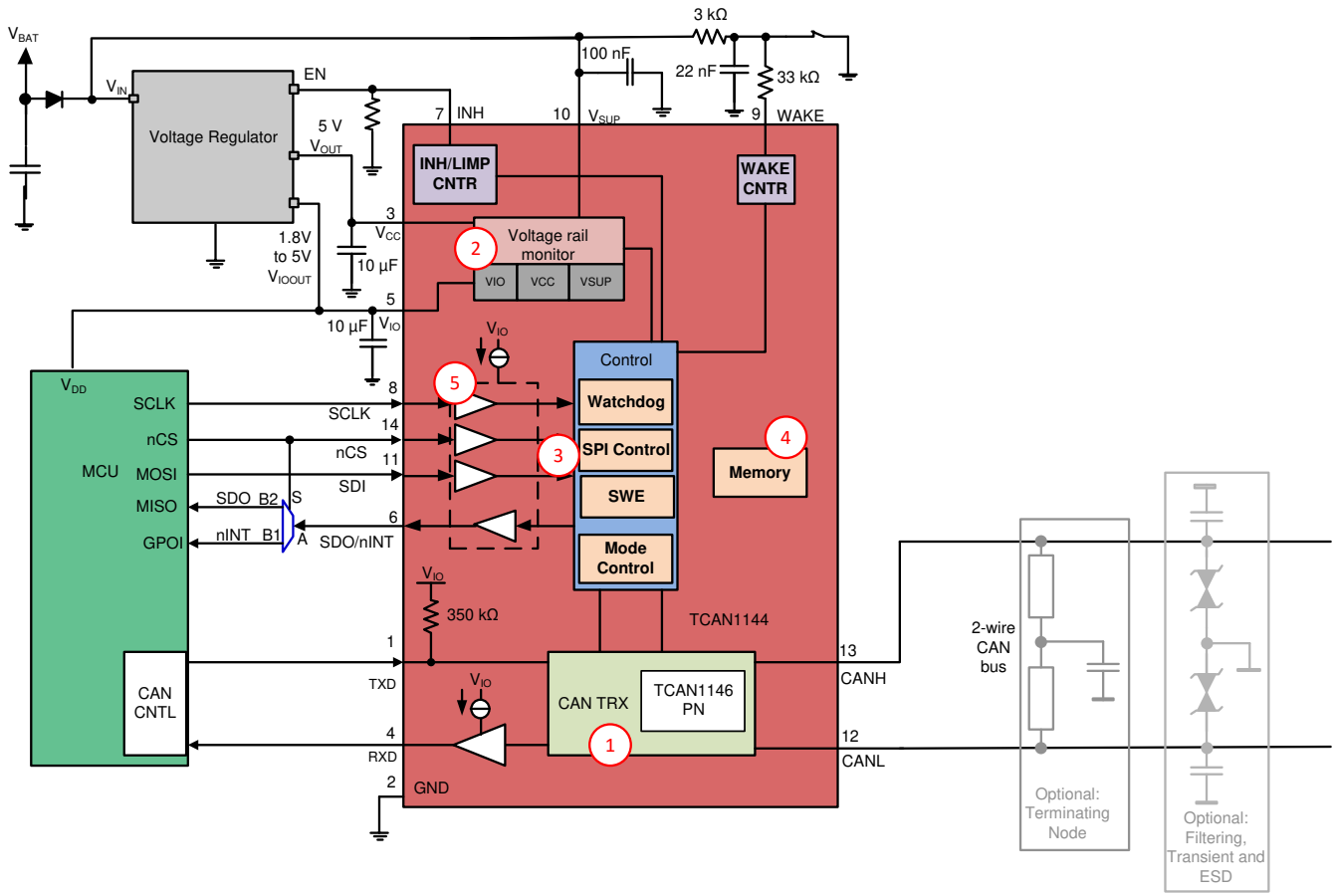

Figure 6-4. TCAN1144-Q1 and TCAN1146-Q1 Potential Failure Points

Potential Failure Point from Figure 6-4	Potential Failure Point Description	Section
1	CAN communication	See Section 8.3.1.1, Section 8.3.1.2, Section 8.3.1.3, Section 8.3.1.4 and Section 8.3.1.5
2	Supply voltage rail monitoring	See Section 8.3.2.1, Section 8.3.2.2 and Section 8.3.2.3
3	SPI/Processor communication	See Section 8.3.3.1, Section 8.3.3.2, Section 8.3.3.3 and Section 8.3.3.4
4	Device internal EEPROM	See Section 8.3.4.1
5	Floating pins	See Section 8.3.5.1, Section 8.3.5.2, Section 8.3.5.3 and Section 8.3.5.4

Figure 6-5. Potential Failure Points and Safety Mechanism

6.2 Hardware Component Functional Safety Concept

The TCAN1144-Q1 and TCAN1146-Q1 were developed using Texas Instruments Incorporated Quality Managed product development process and quailified according to AEC Q100 Grade 1. The process falls under TI's Functional Safety Quality-Managed, per ISO 26262:2018 as a Safety Element out of Context (SEooC).

6.3 Functional Safety Constraints and Assumptions

In creating a functional Safety Element out of Context (SEooC) concept and doing the functional safety analysis, TI generates a series of assumptions on system level design, functional safety concept, and requirements. These assumptions (sometimes called Assumptions of Use) are listed below. Additional assumptions about the detailed implementation of safety mechanisms are separately located in Section 8.3.

The device Functional Safety Analysis was done under the following system assumptions:

- **[SA_1]** The system integrator shall not exceed the recommended operating conditions in the component data sheet.
- **[SA_2]** A typical application is as shown in Figure 6-3

During integration activities these assumptions of use and integration guidelines described for this component shall be considered. Use caution if one of the above functional safety assumptions on this component cannot be met, as some identified gaps may be unresolvable at the system level.

7 Description of Hardware Component Parts

A semiconductor component can be divided into parts to enable a more granular functional safety analysis. This can be useful to help assign specific functional safety mechanisms to portions of the design where they provide coverage ending up with a more complete and customizable functional safety analysis. This section includes a brief description of each hardware part of this component and lists the functional safety mechanisms that can be applied to each. This section is intended to provide additional details about the assignment of functional safety mechanisms that can be found in the Safety Analysis Report. The content in this section is also summarized in Appendix Summary of Recommended Functional Safety Mechanism Usage .

7.1 CAN Transceiver

The TCAN1144-Q1 and TCAN1146-Q1 provides a flexible data rate control area network (CAN FD) transceiver used to communicate between a node processor and the CAN bus. CAN protocol has inherent mechanisms for data accuracy and is outside the scope of the device.

The following can be applied as functional safety mechanisms for this module:

- Section 8.3.1.1
- Section 8.3.1.2
- Section 8.3.1.3
- Section 8.3.1.5

7.2 Digital Core

The TCAN1144-Q1 and TCAN1146-Q1 contains an internal digital core that operates the device and contains several diagnostic features such as: TXD dominant time out timer, SPI communication processer and addressable registers, time out, windowed, or Q&A watchdog timer, and the sleep wake error timer. The digital core also interfaces with the internal EEPROM memory and has CRC checking capability to ensure good data retention.

- Section 8.3.1.4
- Section 8.3.3.1
- Section 8.3.3.2
- Section 8.3.3.3
- Section 8.3.3.4
- Section 8.3.4.1

7.3 EEPROM

The TCAN1144-Q1 and TCAN1146-Q1 have an internal EEPROM memory for storing device trim selections. This EEPROM is programmed in a test only mode utilizing an internal charge pump and is monitored with a CRC check by the digital core of the device.

- Section 8.3.4.1

7.4 Power Control IP

The TCAN1144-Q1 and TCAN1146-Q1 contains several circuit blocks that are responsible for internal power management of the device. The power control unit encompasses two internal regulators to generate a 5V and 1.5V supply, from the VSUP supply , for the analog and digital circuitry needed for the device to operate. The power control unit contains a bandgap voltage and current reference to provide biasing to the internal analog circuits. There are two oscillator inside the device that generates clock signals that operate the digital core in a synchronous fashion.

7.4.1 Voltage Monitors

The TCAN1144-Q1 and TCAN1146-Q1 contain three internal voltage monitors to ensure the health of the supply voltages on the VSUP, VCC, and VIO pins respectively. These monitors are used to provide under voltage lock out features for the internal circuits.

- Section 8.3.2.1
- Section 8.3.2.2

- Section 8.3.2.3

7.5 Thermal Shut Down

The TCAN1144-Q1 and TCAN1146-Q1 has a thermal shutdown feature that will disable the CAN transmitter and enter a thermal fail-safe mode should the silicon die overheat.

- Section 8.3.1.2

7.6 Digital Input/Outputs

The TCAN1144-Q1 and TCAN1146-Q1 has 6 digital I/O pins, four of which are used to implement the SPI communications and the other two are utilized for the TXD and RXD signals for the CAN. These digital I/Os operate on the voltage provided on the VIO supply pin, eliminating the need for external level shifting of the signals. Four of these input pins have integrated pull-up resistors that weakly biases them.

- Section 8.3.5.1
- Section 8.3.5.2
- Section 8.3.5.3
- Section 8.3.5.4

8 TCAN1144-Q1 and TCAN1146-Q1 Management of Random Faults

For a functional safety critical development it is necessary to manage both systematic and random faults. The device architecture does not include any functional safety mechanisms which can detect and respond to random faults when used correctly. This section of the document describes the architectural functional safety concept for each sub-block of the device. The system integrator shall review the recommended functional safety mechanisms in the functional safety analysis report (FMEDA) in addition to this safety manual to determine the appropriate functional safety mechanisms to include in their system. The component data sheet or technical reference manual (if available) are useful tools for finding more specific information about the implementation of these features.

8.1 Fault Reporting

The TCAN1144-Q1 and TCAN1146-Q1 utilize interrupt registers for fault reporting. The global register is provided from the device whenever nCS is pulled low and valid clock provided on SCLK. This register provides information on where to find other interrupts.

Table 8-1. INT_GLOBAL Register Field Descriptions (Address = 50h)

Bit	Field	Type	Reset	Description
7	GLOBALERR	RH	0b	Logical OR of all interrupts
6	INT_1	RH	0b	Logical OR of INT_1 register
5	INT_2	RH	0b	Logical OR of INT_2 register
4	INT_3	RH	0b	Logical OR of INT_3 register
3	INT_CANBUS	RH	0b	Logical OR of INT_CANBUS register
2-0	RSVD	R	0000b	Reserved

Table 8-2. INT_1 Register Field Descriptions (Address = 51h)

Bit	Field	Type	Reset	Description
7	WD	R/W1C	0b	Watchdog event interrupt. NOTE: This interrupt bit will be set for every watchdog error event and does not reliy upon the Watchdog error counter
6	CANINT	R/W1C	0b	CAN bus wake up interrupt
5	LWU	R/W1C	0b	Local wake up
4	WKERR	R/W1C	0b	Wake error bit is set when the SWE timer has expired and the state machine has returned to Sleep mode
3	FRAME_OVF	R/W1C	0b	Frame error counter overflow
2	CANSLNT	R/W1C	0b	CAN silent
1	CANTO	R/W1C	0b	CAN timeout
0	CANDOM	R/W1C	0b	CAN bus stuck dominant

Table 8-3. INT_2 Register Field Descriptions (Address = 52h)

Bit	Field	Type	Reset	Description
7	SMS	R/W1C	0b	Sleep mode status flag. Only sets when sleep mode is entered by a WKERR, UVIO timeout or UVIO + TSD fault
6	PWRON	R/W1C	1b	Power on
5	RSVD	R-0b	0b	Reserved
4	UVSUP	R/W1C	0b	V_{SUP} undervoltage
3	UVIO	R/W1C	0b	V_{IO} undervoltage
2	UVCC	R/W1C	0b	V_{CC} undervoltage
1	TSD	R/W1C	0b	Thermal Shutdown
0	TSDW	R/W1C	0b	Thermal Shutdown Warning

Table 8-4. INT_3 Register Field Descriptions (Address = 53h)

Bit	Field	Type	Reset	Description
7	SPIERR	R/W1C	0b	Sets when SPI status bit sets

Table 8-4. INT_3 Register Field Descriptions (Address = 53h) (continued)

Bit	Field	Type	Reset	Description
6	SWERR	RH	0b	Logical OR of (SW_EN=1 and NOT(SWCFG)) and FRAME_OVF. Selective Wake may not be enabled while SWERR is set
5	FSM	R/W1C	0b	Entered fail-safe mode. Can be cleared while in fail-safe mode.
4-1	RSVD	R	0000b	Reserved
0	CRC_EEPROM	R/W1C	0b	EEPROM CRC error

Table 8-5. INT_CANBUS Register Field Descriptions (Address = 54h)

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved
6	CANBUSTERMOPEN	R/W1C	0b	CAN bus has one termination point open
5	CANHCANL	R/W1C	0b	CANH and CANL shorted together
4	CANHBAT	R/W1C	0b	CANH shorted to Vbat
3	CANLGND	R/W1C	0b	CANL shorted to GND
2	CANBUSOPEN	R/W1C	0b	CAN bus open
1	CANBUSGND	R/W1C	0b	CAN bus shorted to GND or CANH shorted to GND
0	CANBUSBAT	R/W1C	0b	CAN bus shorted to Vbat or CANL shorted to Vbat

8.2 Functional Safety Mechanism Categories

This section includes a description of the different types of functional safety mechanisms that are applied to the design blocks of the device.

The functional safety mechanism categories are defined as follows:

Component Hardware Functional Safety Mechanisms — A safety mechanism that is implemented by TI in silicon which can communicate error status upon the detection of failures. The safety mechanism may require software to enable its functionality, to take action when a failure is detected, or both.

Component Hardware and Software Functional Safety Mechanisms — A test recommended by TI which requires both, safety mechanism hardware which has been implemented in silicon by TI, and which requires software. The failure modes of the hardware used in this safety mechanisms are analyzed or described as part of the functional safety analysis or FMEDA. The system implementer is responsible for analyzing the software aspects for this safety mechanism.

Component Software Functional Safety Mechanisms — A software test recommended by TI. The failure modes of the software used in this safety mechanism are not analyzed or described in the functional safety analysis or FMEDA. For some components, TI may provide example code or supporting code for the software functional safety mechanisms. This code is intended to aid in the development, but the customer shall do integration testing and verification as needed for their system functional safety concept.

System Functional Safety Mechanisms — A safety mechanism implemented externally of this component. For example an external monitoring IC would be considered to be a system functional safety mechanism.

Test for Safety Mechanisms — This test provides coverage for faults on a safety mechanism only. It does not provide coverage for the primary function.

Alternative Safety Mechanisms — An alternative safety mechanism is not capable of detecting a fault of safety mechanism hardware, but instead is capable of recognizing the primary function fault (that another safety mechanism may have failed to detect). Alternate safety mechanisms are typically used when there is no direct test for a safety mechanism.

8.3 Description of Functional Safety Mechanisms

This section provides a brief summary of the functional safety mechanisms available on this component.

8.3.1 CAN Communication

The TCAN1144-Q1 and TCAN1146-Q1 are enhanced high-speed CAN FD transceivers supporting data rates up to 5 Mbps. These devices are configured using serial peripheral interface (SPI) in order to use all the features available. The devices support 1.8 V to 5 V processors by applying the appropriate voltage to the V_{IO} pin, allowing lower voltage processors to be utilized.

The TCAN1144-Q1 and TCAN1146-Q1 provide CAN FD transceiver function: differential transmit capability to the bus and differential receive capability from the bus. The device includes many protection features providing device and CAN network robustness. The CAN bus has two logical states during operation: recessive and dominant.

Recessive bus state is when the bus is biased to a common mode of about 2.5 V via the high resistance internal input resistors of the receiver of each node on the bus across the termination resistors. Recessive is equivalent to logic high and is typically a differential voltage 0.5 V or less between CANH and CANL. Recessive state is also the idle state.

Dominant bus state is when the bus is driven differentially by one or more drivers. Current is induced to flow through the termination resistors and generate a differential voltage on the bus. Dominant is equivalent to logic low and is a differential voltage on the bus greater than the minimum threshold of 0.9 V for a CAN dominant. A dominant state overwrites the recessive state.

Devices safety mechanisms SM-1, SM-2, SM-3 and SM-4 are provided by the device itself while SM-17 is an inherent mechanism provided by CAN protocol.

8.3.1.1 SM-1: CAN bus fault diagnostic

The TCAN1144-Q1 and TCAN1146-Q1 provides advanced bus fault detection. TCAN1146-Q1 is used for illustration purposes. The device can determine certain fault conditions and set a status/interrupt flag so that the MCU can understand what the fault is. Detection takes place and is recorded if the fault is present during four dominant to recessive transitions with each dominant bit being > 1.5 µs. As with any bus architecture where termination resistors are at each end not every fault can be specified to the lowest level, meaning exact location. The fault detection circuitry is monitoring the CANH and CANL pins (currents) to determine if there is a short to battery, short to ground, short to each other or opens. From a system perspective, the location of the device also determine what can be detected. See device data sheet for detailed desciption of the CAN bus fault diagnostic.

8.3.1.2 SM-2: Thermal shutdown; TSD

The TCAN1144-Q1 and TCAN1146-Q1 has two trigger points for thermal events. The first is a thermal shutdown warning. Once the temperature exceeds this limit, an interrupt is issued. The second is the actual thermal shutdown (TSD) event.

This is a device preservation event. If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN transceiver and CAN transceiver circuitry thus blocking the signal to bus transmission path. A thermal shut down interrupt flag is set, and an interrupt is inserted so that the microprocessor is informed. If this event happens, other interrupt flags may be set as well. An example is a bus fault where the CAN bus is shorted to Vbat. When this happens, the digital core and SPI interface is still active. After a time of ≈ 300 ms the device checks the temperature of the junction. Thermal shutdown timer, t_{TSD}, starts when TSD fault event starts and exit to sleep mode when TSD fault is not present when TSD timer is expired. While in thermal shut down protected mode, a SPI write to change the device to either Normal or Standby mode is ignored while writes to change to sleep mode are accepted.

If the TSD event takes place and fail-safe mode is enabled, the same process takes place with and instead off thermal shut down protected stated the device enters fail-safe mode.

8.3.1.3 SM-3: CAN bus short circuit limiter, I_{OS}

These devices limit the short-circuit current when a CAN bus line is shorted. The CAN driver is current limited (dominant and recessive) with values of ± 115 mA for I_{OS_DOM} and ± 5 mA for I_{OS_REC}. During CAN communication the bus switches between dominant and recessive states; thus, the short-circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings, the average short-circuit current

should be used. The percentage dominant is limited by the TXD dominant time out and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and inter frame space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits. See data sheet for more information.

8.3.1.4 SM-4: CAN TXD pin dominant state timeout; t_{TXD_DTO}

The TCAN1144-Q1 and TCAN1146-Q1 supports dominant state time out (DTO). This is an internal function based upon the TXD path. The TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant (LOW) longer than the time out period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time out constant of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal (HIGH) is seen on TXD terminal; thus, clearing the dominant time out. The receiver remains active and the RXD terminal reflects the activity on the CAN bus and the bus terminals is biased to recessive level during a TXD DTO fault. This feature can be disabled by using register 8'h10[6] = 1b, DTO_DIS.

Note

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame.

8.3.1.5 SM-17: CAN protocol

CAN protocol has several mechanism that will make sure the data provided is correct, like CRC. If incorrect, the processor will disregard the CAN packets.

8.3.2 Supply Voltage Rail Monitoring

There are three under voltage events monitored in the TCAN1144-Q1 and TCAN1146-Q1, VSUP, VIO and VCC. The three supply terminals are input sources for the TCAN114x-Q1 and have under voltage detection circuitry which places the device in a protected state if an under voltage fault occurs, UV_{SUP}, UV_{CC} and UV_{IO}. This protects the bus during an under voltage event on these terminals. If VSUP is under voltage the device loses the source needed to keep the internal regulators active. This causes the device to go into a state where communication between the microprocessor and the TCAN114x-Q1 is disabled. The TCAN114x-Q1 is not able to receive information from the bus; and thus, does not pass any signals from the bus, including any Bus Wake via BWRR signals to the microprocessor.

Safety mechanisms SM-5, SM-6 and SM-7 cover this.

Table 8-6. UV_{SUP}, UV_{CC}

V_{SUP}	V_{CC}	DEVICE STATE	BUS	RXD
> UV_{SUP}	> UV_{CC}	Normal	Per TXD	Mirrors Bus
> UV_{SUP}	< UV_{CC}	Fail-safe or Sleep	High Impedance	High (Recessive)
< UV_{SUP}	NA	Power off	High Impedance	High Impedance

Table 8-7. Under Voltage Lockout

V_{SUP}	V_{IO}	V_{CC}	DEVICE STATE	BUS	RXD
> UV_{SUP}	> UV_{IO}	> UV_{CC}	Normal	Per TXD	Mirrors Bus
> UV_{SUP}	> UV_{IO}	< UV_{CC}	Fail-safe or Sleep	High Impedance	High (Recessive)
< UV_{SUP}	> UV_{IO}	NA	Power Off	High Impedance	High (Recessive)
> UV_{SUP}	< UV_{IO}	> UV_{CC}	Fail-safe or UV_{IO} Protected — > Sleep	High Impedance	High Impedance
> UV_{SUP}	< UV_{IO}	< UV_{CC}	Fail-safe or Sleep	High Impedance	High Impedance
< UV_{SUP}	< UV_{IO}	NA	Power Off	High Impedance	High Impedance

8.3.2.1 SM-5: VCC undervoltage; UV_{CC}

The TCAN1144-Q1 and TCAN1146-Q1 monitors the VCC supply rail that powers the CAN transceiver. For undervoltage events, there is a filter time, t_{UVFLTR}, that the event must last longer than for the t_{UVSLP} timer to start. Once the t_{UVSLP} timer expires and the under voltage condition is still present, the device enters sleep mode or fail-safe mode if enabled. See UV_{CC} state diagram.

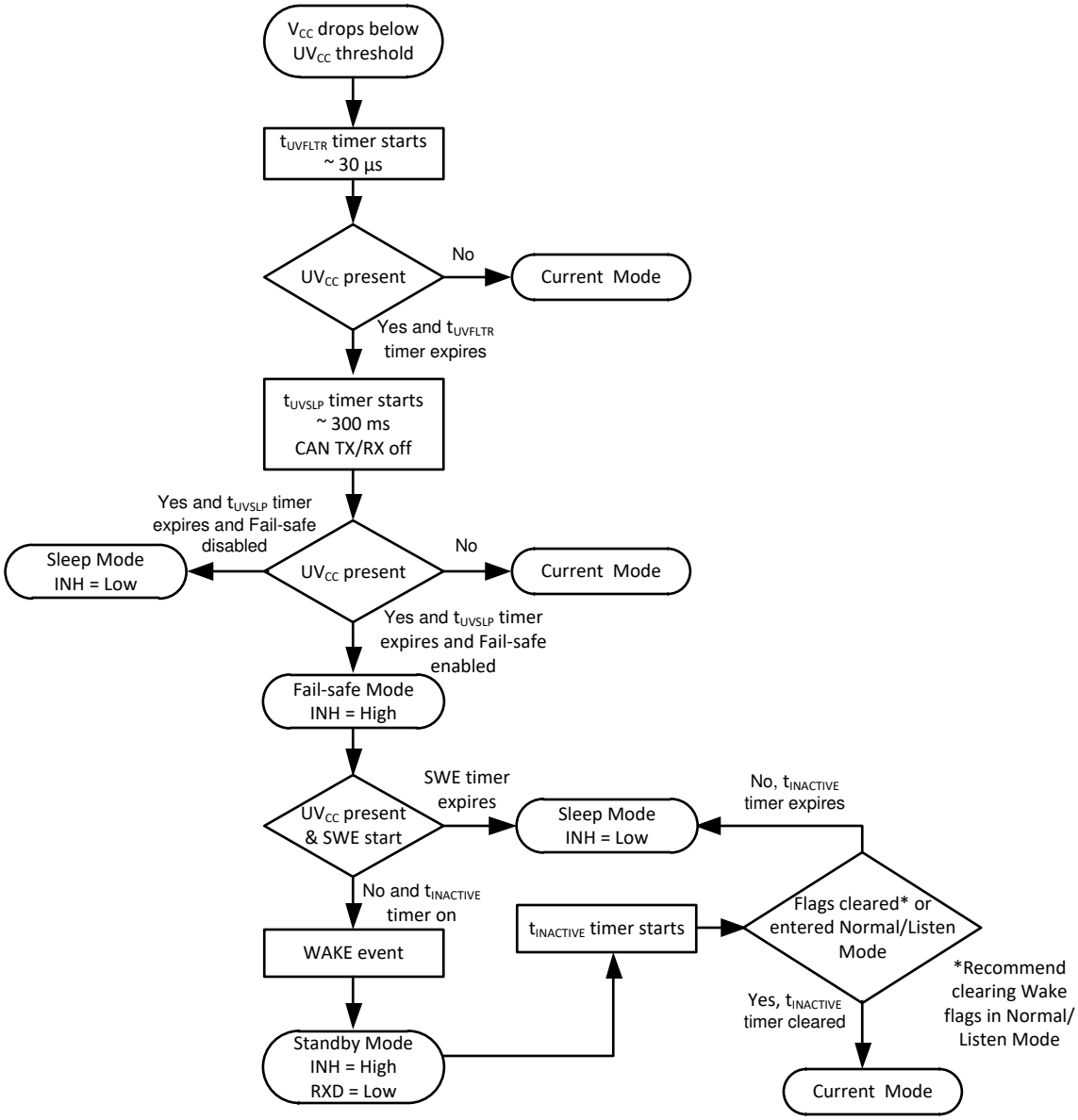

Figure 8-1. UV_{CC} State Diagram

8.3.2.2 SM-6: VSUP supply undervoltage; UV_{SUP}

The TCAN1144-Q1 and TCAN1146-Q1 monitors the VSUP supply rail for under voltage event, UV_{SUPF}. If this threshold is crossed the filter time, t_{UVFLTR}, starts and must expire to be considered an under voltage event. A UV_{SUP} event will cause the INH pin to turn off. When the VSUP is greater than UV_{SUP} and INH turns on the SWE timer will start as the device enters standby mode. If VSUP decreases until less than $V_{SUP(PU)F}$, the device shuts everything down as the POR level has been reached. When VSUP returns, the device comes up as if it is the initial power on. All registers are cleared and the device has to be reconfigured.

8.3.2.3 SM-7: VIO supply undervoltage; UV_{IO}

If VIO drops below UV_{IO} under voltage detection several functions are disabled. The transceiver switches off and disengages from the bus until VIO has recovered. When UV_{IO} triggers, the t_{UV} timer starts. If the timer times out and the UV_{IO} is still there, the device enters sleep mode. Once in sleep mode, a wake event is required to place the TCAN114x-Q1 into standby mode and enable the INH pin. As registers are cleared in sleep mode, the UV_{IO} interrupt flag is lost. If the UV_{IO} event is still in place, the cycle repeats. If during a thermal shut down event a UV_{IO} event happens, the device automatically enters sleep mode.

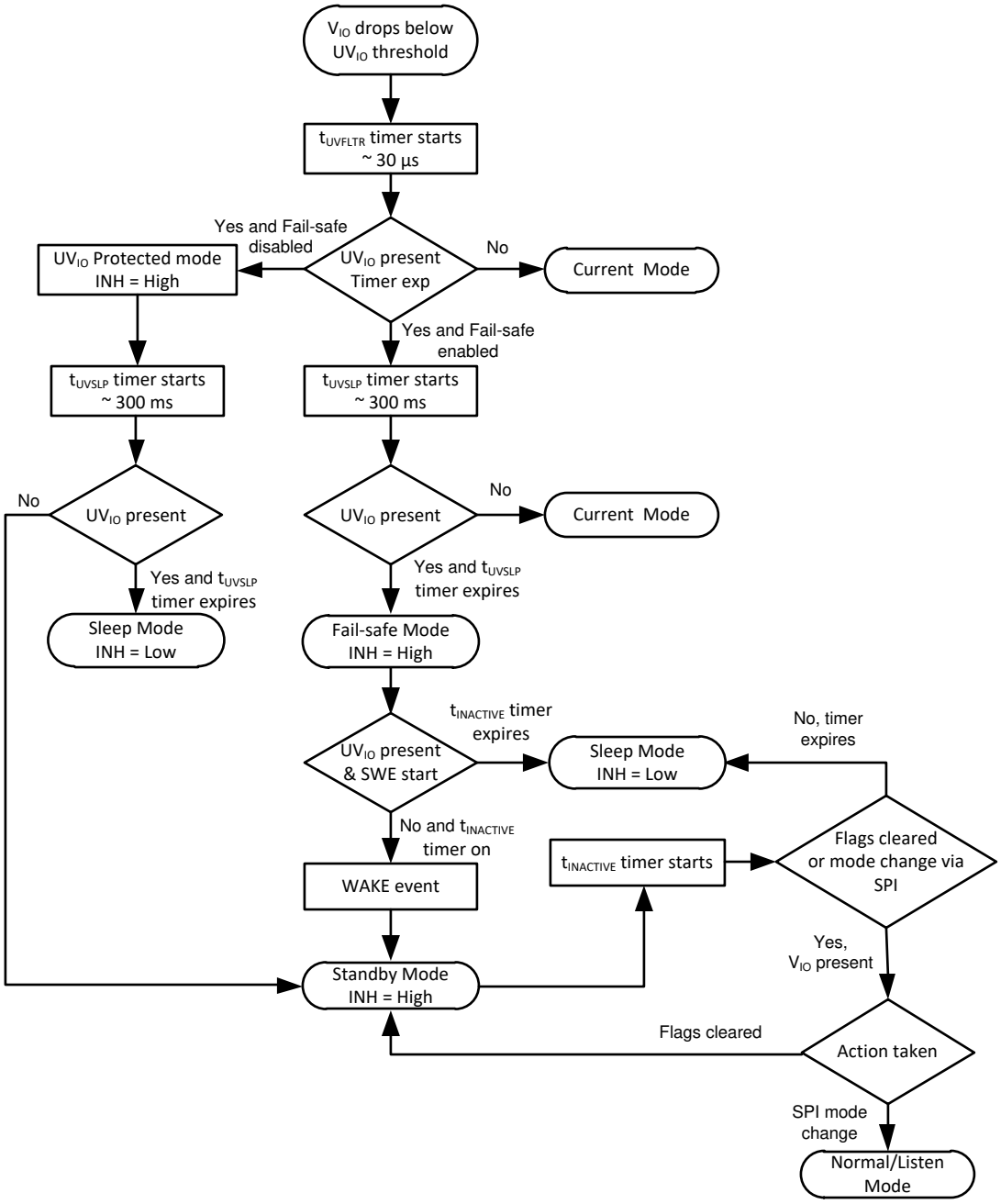

Figure 8-2. UV_{IO} State Diagram

8.3.3 SPI/Processor Communication

The TCAN1144-Q1 and TCAN1146-Q1 have several ways to determine if the communication between the processor and device is functioning correctly. SM-8, SM-9, SM-10 and SM-11 provide information on the methodologies.

8.3.3.1 SM-8: Timout, Window or Q&A watchdog error - Normal mode

The TCAN1144-Q1 and TCAN1146-Q1 support an integrated watchdog function. The devices provide a default window-based watchdog as well as a selectable time-out and question and answer (Q&A) watchdog using the SPI programming. The watchdog timer does not start until the first input trigger event when in normal and standby (when enabled) operational modes. The watchdog timer is off in sleep mode. The INH pin can be programmed as a LIMP function which provides a limp home capability when connected to external circuitry. Otherwise the nINT will reflect a watchdog failure. When in sleep mode, the limp function is off. When the error counter reaches the watchdog trigger event level, the limp pin turns on connecting VSUP to the pin as described in the INH/LIMP pin section. See the data sheet for detailed description on watchdog capability.

8.3.3.2 SM-9: SPI communication error; SPIERR

The Serial Peripheriial Interface (SPI) uses a standard configuration. Physically the digital interface pins are nCS (Chip Select Not), SDI (Serial Data In), SDO (Serial Data Out) and SCLK (Serial Clock). Each SPI transaction is a 16, 24 or 32 bits containing an address and read/write command byte followed by one to three data bytes.

Supporting two and three data bytes is accomplished utilizing burst read and write where the address is automatically incremented for the data along with the same number of clock cycles per bit. The data shifted out on the SDO pin for the transaction always starts with the Global Status Register (byte).

Once the SPI is enabled by a low on nCS, the device samples the input data on each rising edge of the SPI clock (SCLK). The data is shifted into an appropriate sized shift register and after the correct number of clock cycles the shift register is full and the SPI transaction is complete. For a write command code, the new data is written into the addressed register only after the exact number of clock cycles have been shifted in by SCLK and the nCS has a rising edge to deselect the device. For a burst write if there are 31 clock cycles of SCLK (1 clock cycle less than the full 3 byte write), the third byte write won't happen while the first two bytes write will be executed. If the correct number of clock cycles and data are not shifted in during one SPI transaction (nCS low), interrupts at 8'h50[7], 8'h50[4] and 8'h53[7], SPIERR, will be set.

8.3.3.3 SM-10: Scratchpad write/read

The TCAN1144-Q1 and TCAN1146-Q1 provide a memory scratchpad, 8'h0F[7:0] that makes it possible to write and read back data for verification of accuracy. This verifies SPI interface to register space.

8.3.3.4 SM-11: Sleep Wake Error Timer; $t_{INACTIVE}$

The sleep wake error (SWE) timer is a timer used to determine if specific external and internal functions are working. Upon power up, POR or UVSUP event, the SWE timer starts, $t_{INACTIVE}$, and the processor has typically 4.5 minutes to configure the device, clear the PWRON flag or change the device to normal or listen mode. This feature cannot be disabled for power up. If the device has not had the PWRON flag cleared or been placed into normal or listen mode, it enters sleep mode. The SWE timer can be disabled for the other scenarios that cause the device to enter fail-safe mode by setting SWE_DIS; 8'h1C[7] = 1 and FS_DIS at 8'h17[0] = 1.

The device wakes up if the CAN bus provides a WUP or a local wake event takes place thus entering standby mode. Once in standby mode, the $t_{SILENCE}$ and $t_{INACTIVE}$ timers start. If the $t_{INACTIVE}$ expires the device re-enters sleep mode. When the device receives a CANINT, and LWU or FRAME_OVF such that the device leaves sleep mode and enters standby mode, the processor has $t_{INACTIVE}$ to clear the flags and place it into normal mode. If this does not happen, the device enters sleep mode. When in standby, normal or listen mode and the CANSLNT flag persists for $t_{INACTIVE}$, the device enters sleep mode. Examples of events that could create this are the processor is no longer working and not able to exercise the SPI bus, or a go to sleep command comes in and the processor is not able to receive it or is not able to respond. See data sheet.

When fail-safe mode (FSM) is enabled and the SWE timer expires the device will enter FSM and will indicate the fault at 8'h50[7], 8'h50[4] and 8'h53[5] = FSM.

Figure 8-3 shows when the SWE timer, $t_{INACTIVE}$, starts and what mode transitions take place.

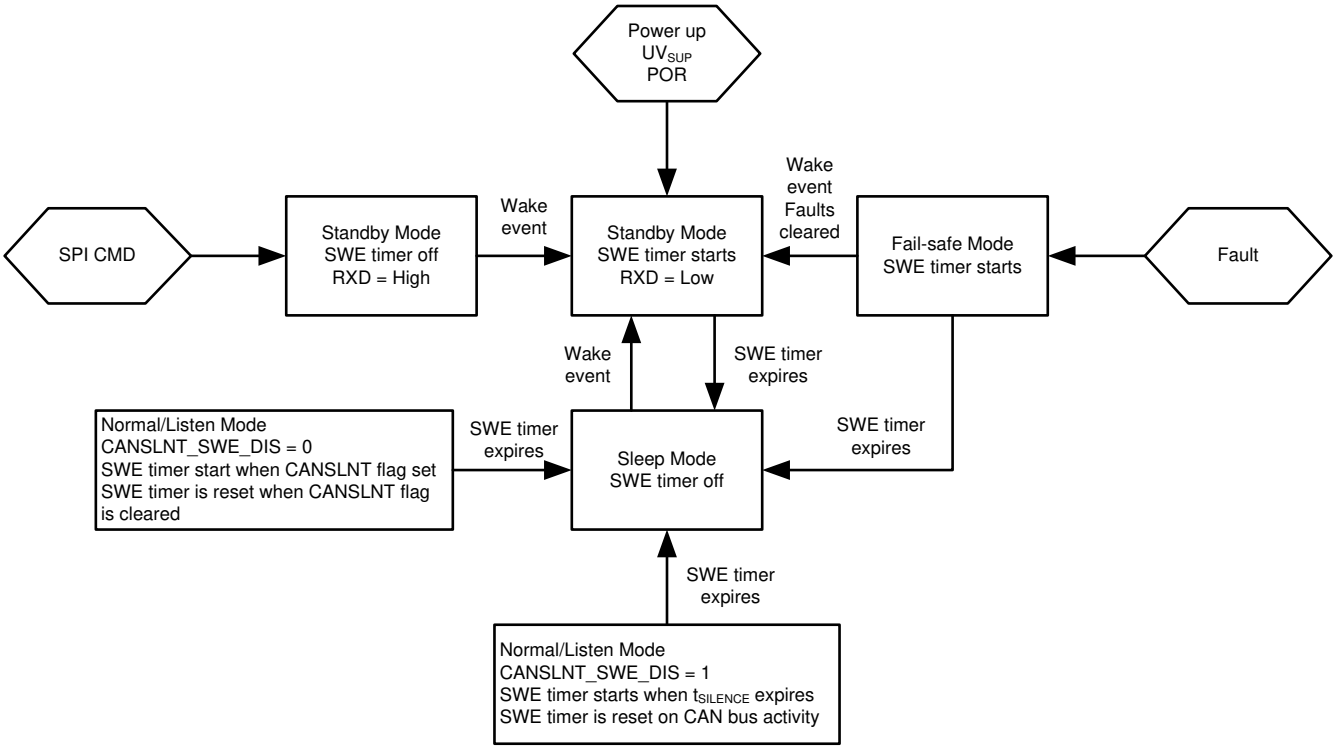

Figure 8-3. Sleep Wake Error (SWE) Timer, $t_{INACTIVE}$

8.3.4 Device Internal EEPROM

The TCAN1144-Q1 and TCAN1146-Q1 use an internal EEPROM for certain performance trimming. Upon power up the device loads an internal register from the EEPROM and performs a CRC check. This is repeated when the device leaves sleep mode or fail-safe mode due to a wake event. SM-12 provides information on the process and fault indication.

8.3.4.1 SM-12: Internal memory CRC; CRC_EEPROM

The CRC_EEPROM interrupt is set when the internal EEPROM used for trimming has a CRC error. Upon power up the device loads an internal register from the EEPROM and performs a CRC check. If an error is present after eight attempts of loading valid data the CRC_EEPROM interrupt will be set. This will indicate an error that may impact device performance. This is repeated when the device leaves sleep mode or fail-safe mode due to a wake event. The device will perform a CRC check on the internal registers loaded from the EEPROM. If there is an error the device will reload the registers from the EEPROM. If there is a CRC error the device will attempt to load the internal registers up to eight times. After the eighth attempt the CRC_EEPROM interrupt flag will be set. This will indicate an error that may impact the device performance.

8.3.5 Floating Pins

There are internal pull ups on critical terminals to place the device into known states if the terminal floats. SM-13, SM-14 and SM-15 provide more information.

Table 8-8. Terminal Bias

TERMINAL	PULL UP or PULL DOWN	COMMENT
SCLK	Pull up	Weakly biases input
SDI	Pull up	Weakly biases input
nCS	Pull up	Weakly biases input so the device is not selected
TXD	Pull up	Weakly biases input

Note

The internal bias should not be relied upon as only termination, especially in noisy environments but should be considered a fail-safe protection. Special care needs to be taken when the device is used with MCUs using open drain outputs.

8.3.5.1 SM-13: SCLK internal pull-up to VIO

In case of open (floating pins) the default state of SCLK pin is provided by an integrated pull-up resistors that weakly biases the pin.

8.3.5.2 SM-14: SDI internal pull-up to VIO

In case of open (floating pins) the default state of SDI pin is provided by an integrated pull-up resistors that weakly biases the pin.

8.3.5.3 SM-15: nCS internal pull-up to VIO

In case of open (floating pins) the default state of nCS pin is provided by an integrated pull-up resistor that weakly biases the pin. This keeps the device SPI from being constantly enabled or intermittently enabled due to noise.

8.3.5.4 SM-16: TXD internal pull-up to VIO

In case of open (floating pins) the default state of the TXD pin is provided by an integrated pull-up resistor that weakly biases the pin. This keeps the TXD pin from inadvertently having a dominant on TXD due to noise.

B Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial release.

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