Functional Safety Information

ISO154x-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for ISO154x-Q1 (8-D package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

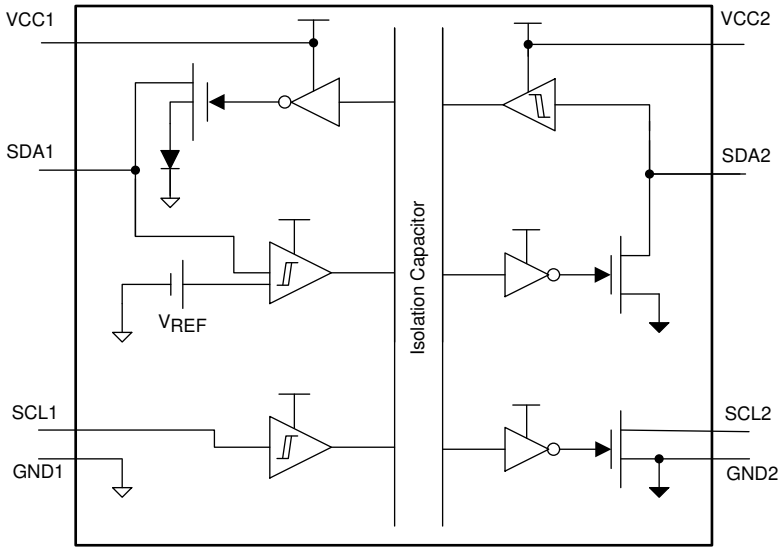

Figure 1-1. Functional Block Diagram

ISO154x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 8-D Package

This section provides Functional Safety Failure In Time (FIT) rates for 8-D package of ISO154x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	10
Die FIT Rate	3
Package FIT Rate	7

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 85 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55 °C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ISO154x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SDAx and/or SCLx out of electrical or timing specification	69%
SDAx and/or SCLx stuck high via external pull-up resistor	23%
SDAx and/or SCLx stuck low	6%
SDAx and/or SCLx output undetermined	2%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ISO1540-Q1 and ISO1541-Q1 (both in 8-D package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (seeTable 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External pull-up resistor on both SDA1/SCL1 to V_{CC1}, pull-up resistor on SDA2/SCL2 to V_{CC2}

4.1 ISO1541-Q1 in 8-D Package

Figure 4-1 shows the ISO1541-Q1 pin diagram for the 8-D package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ISO154x-Q1 data sheet.

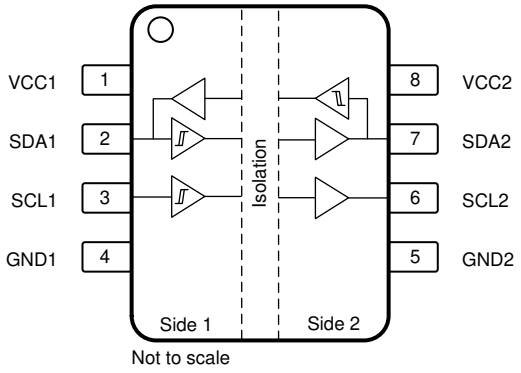

Figure 4-1. Pin Diagram (8-D) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	No power to the device on side-1. Observe that the absolute maximum ratings for SDA1/SCL1 are met; otherwise device damage may be plausible.	A
SDA1	2	SDA1 stuck to low, makes SDA2 also low. Communication corrupted to and from the master node.	B
SCL1	3	SCL1 stuck to low, makes SCL2 also low. Communication corrupted to and from the master.	B
GND1	4	Device continues to function as expected. Normal operation.	D
GND2	5	Device continues to function as expected. Normal operation.	D
SCL2	6	SCL2 stuck low. Data communication from master SCL1 to slave SCL2 lost. Communication corrupted.	B
SDA2	7	SDA2 stuck low, makes SDA1 also low. Communication corrupted to and from the master node.	B
V_{CC2}	8	No power to the device on side-2. Observe that the absolute maximum ratings for SDA2/SCL2 are met; otherwise device damage may be plausible.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	Operation undetermined. Either device is unpowered and SDA2/SCL2 are pulled to logic high to external pull-up resistors or through internal ESD diode on SDA1/SCL1 pin, device can power up if SDA1/SCL1 are logic high. If abs max rating of SDA1/SCL1 is not observed, device damage plausible.	A
SDA1	2	No data communication to and from the master node possible.	B
SCL1	3	Clock missing, so no I2C communication possible.	B
GND1	4	Device unpowered on side1. SDA2/SCL2 are logic high via external pull-up resistors.	B
GND2	5	Device unpowered on side2. SDA1/SCL1 are logic high via external pull-up resistors.	B
SCL2	6	Clock missing, so no I2C communication possible.	B
SDA2	7	No data communication possible.	B
V_{CC2}	8	Operation undetermined. Either device is unpowered and SDA1/SCL1 are pulled to logic high to external pull-up resistors or through internal ESD diode on SDA2/SCL2 pin, device can power up if SDA2/SCL2 are logic high. If abs max rating of SDA2/SCL2 is not observed, device damage plausible.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	SDA1	SDA1 stuck high. Communication corrupted. If SDA2 is driven logic low for extended duration, SDA1 stuck high creates short between supply and ground, possible device damage.	A
SDA1	2	SCL1	I2C Communication corrupted.	B
SCL1	3	GND1	SCL1 stuck to low, makes SCL2 also low. Communication corrupted to and from the master.	B
GND1	4	SCL1	Already considered in above row.	B
GND2	5	SCL2	SCL2 stuck low. Data communication from master SCL1 to slave SCL2 lost. Communication corrupted.	B
SCL2	6	SDA2	I2C Communication corrupted.	B
SDA2	7	V_{CC2}	SDA2 stuck high. Communication corrupted. If SDA1 is driven logic low for extended duration, SDA2 stuck high creates short between supply and ground, possible device damage.	A
V_{CC2}	8	SDA2	Already considered in above row.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	No effect. Normal operation.	D
SDA1	2	SDA1 stuck high. Communication corrupted. If SDA2 is driven logic low for extended duration, SDA1 stuck high creates short between supply and ground, possible device damage.	A
SCL1	3	SCL1 stuck high does not allow clock transitions to happen. I2C communication corrupted.	B
GND1	4	Device side-1 unpowered. Observe that the absolute maximum ratings for SCL1/SDA1 pins of the device are met, otherwise device damage may be plausible.	A
GND2	5	Device side-2 unpowered. Observe that the absolute maximum ratings for SCL2/SDA2 pins of the device are met, otherwise device damage may be plausible.	A
SCL2	6	SCL2 stuck high. If SCL1 is driven low for extended duration, SCL2 stuck high creates a path for high current from supply to ground with possible device damage.	A
SDA2	7	SDA2 stuck high. Communication corrupted. If SDA1 is driven logic low for extended duration, SDA2 stuck high creates short between supply and ground, possible device damage.	A
V_{CC2}	8	No effect. Normal operation.	D

4.2 ISO1540-Q1 in 8-D Package

Figure 4-2 shows the ISO1540-Q1 pin diagram for the 8-D package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ISO1541-Q1 data sheet.

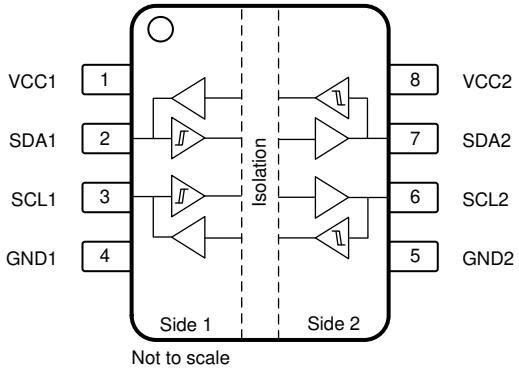

Figure 4-2. Pin Diagram (8-D Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	No power to the device on side-1. Observe that the absolute maximum ratings for SDA1/SCL1 are met; otherwise device damage may be plausible.	A
SDA1	2	SDA1 stuck to low, makes SDA2 also low. Communication corrupted.	B
SCL1	3	SCL1 stuck to low, makes SCL2 also low. Communication corrupted.	B
GND1	4	Device continues to function as expected. Normal operation.	D
GND2	5	Device continues to function as expected. Normal operation.	D
SCL2	6	SCL2 stuck low, makes SCL1 also low. Communication corrupted.	B
SDA2	7	SDA2 stuck low, makes SDA1 also low. Communication corrupted.	B
V_{CC2}	8	No power to the device on side-2. Observe that the absolute maximum ratings for SDA2/SCL2 are met; otherwise device damage may be plausible.	A

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	Operation undetermined. Either device is unpowered and SDA2/SCL2 are pulled to logic high to external pull-up resistors or through internal ESD diode on SDA1/SCL1 pin, device can power up if SDA1/SCL1 are logic high. If abs max rating of SDA1/SCL1 is not observed, device damage plausible.	A
SDA1	2	No data communication possible.	B
SCL1	3	Clock missing, so no communication possible.	B
GND1	4	Device unpowered on side1. SDA2/SCL2 are logic high via external pull-up resistors.	B
GND2	5	Device unpowered on side2. SDA1/SCL1 are logic high via external pull-up resistors.	B
SCL2	6	Clock missing, so no communication possible.	B
SDA2	7	No data communication possible.	B
V_{CC2}	8	Operation undetermined. Either device is unpowered and SDA1/SCL1 are pulled to logic high to external pull-up resistors or through internal ESD diode on SDA2/SCL2 pin, device can power up if SDA2/SCL2 are logic high. If abs max rating of SDA2/SCL2 is not observed, device damage plausible.	A

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	SDA1	SDA1 stuck high. Communication corrupted. If SDA2 is driven logic low for extended duration, SDA1 stuck high creates short between supply and ground, possible device damage.	A
SDA1	2	SCL1	I2C Communication corrupted.	B
SCL1	3	GND1	SCL1 stuck to low, makes SCL2 also low. Communication corrupted.	B
GND1	4	SCL1	Already considered in above row.	B
GND2	5	SCL2	SCL2 stuck low. Data communication corrupted.	B
SCL2	6	SDA2	I2C Communication corrupted.	B
SDA2	7	V_{CC2}	SDA2 stuck high. Communication corrupted. If SDA1 is driven logic low for extended duration, SDA2 stuck high creates short between supply and ground, possible device damage.	A
V_{CC2}	8	SDA2	Already considered in above row.	A

Table 4-9. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC1}	1	No effect. Normal operation.	D
SDA1	2	SDA1 stuck high. Communication corrupted. If SDA2 is driven logic low for extended duration, SDA1 stuck high creates short between supply and ground, possible device damage.	A
SCL1	3	SCL1 stuck high does not allow clock transitions to happen. I2C communication corrupted.	B
GND1	4	Device side-1 unpowered. Observe that the absolute maximum ratings for SCL1/SDA1 pins of the device are met, otherwise device damage may be plausible.	A
GND2	5	Device side-2 unpowered. Observe that the absolute maximum ratings for SCL2/SDA2 pins of the device are met, otherwise device damage may be plausible.	A
SCL2	6	SCL2 stuck high. If SCL1 is driven low for extended duration, SCL2 stuck high creates a path for high current from supply to ground with possible device damage.	A
SDA2	7	SDA2 stuck high. Communication corrupted. If SDA1 is driven logic low for extended duration, SDA2 stuck high creates short between supply and ground, possible device damage.	A
V_{CC2}	8	No effect. Normal operation.	D

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