Application Report

TCAN1145-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

1 Overview......2
2 Functional Safety Failure In Time (FIT) Rates......3
3 Failure Mode Distribution (FMD)......4
4 Pin Failure Mode Analysis (Pin FMA)......5

List of Figures

Figure 1-1. Functional Block Diagram......2
Figure 4-1. 14-pin SOIC (D) Pin Diagram, Top View......5
Figure 4-2. 14-pin VSON (DMT) Pin Diagram, Top View......5
Figure 4-3. 14-pin SOT (DYY) Pin Diagram, Top View......6

List of Tables

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11......3
Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2......3
Table 3-1. Die Failure Modes and Distribution......4
Table 4-1. TI Classification of Failure Effects......5
Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground......6
Table 4-3. Pin FMA for Device Pins Open-Circuited......7
Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin......8
Table 4-5. Pin FMA for Device Pins Short-Circuited to VSUP supply......9
Table 4-6. Pin FMA for Device Pins Short-Circuited to VCC supply......10
Table 4-7. Pin FMA for Device Pins Short-Circuited to VIO supply......11

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1 Overview

This document contains information for TCAN1145-Q1 which is a controller area network flexible data rate (CAN FD) transceiver in 14-pin SOIC (D), 14-pin VSON (DMT) and 14-pin SOT23 (DYY) packages to aid in a functional safety system design. Available Information:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

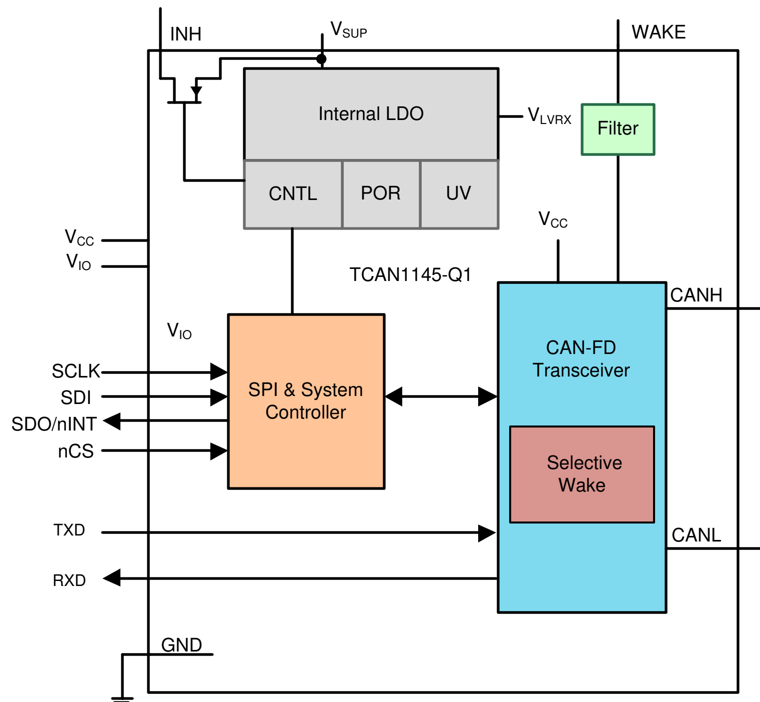

Figure 1-1. Functional Block Diagram

TCAN1145-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the 14-pin SOIC (D), 14-pin VSON (DMT) and 14-pin SOT23 (DYY) packages of the TCAN1145-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) 14-pin SOIC (D)	FIT (Failures Per 10^9 Hours) 14-pin VSON (DMT)	FIT (Failures Per 10^9 Hours) 14-pin SOT (DYY)
Total Component FIT Rate	21	9	9
Die FIT Rate	5	3	5
Package FIT Rate	16	6	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 290 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog/mixed	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCAN1145-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
CAN transceiver transmitter fail	20
CAN transceiver receiver fail	10
Power rail fail	14
Input/output fail	33
Digital core fail	23

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TCAN1145-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VSUP (see Table 4-5)
- Pin short-circuited to VCC (see Table 4-6)
- Pin short-circuited to VIO (see Table 4-7)

Table 4-2 through Table 4-7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TCAN114x-Q1 pin diagrams. For TCAN1145-Q1 pin 6 only supports SDO output and pin 7 only supports INH output. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCAN114x-Q1 data sheet.

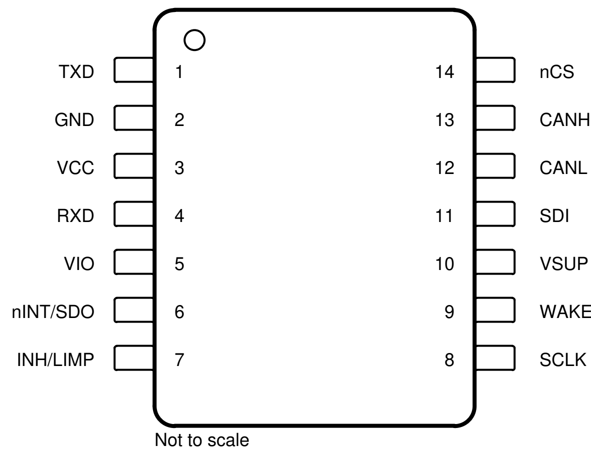

Figure 4-1. 14-pin SOIC (D) Pin Diagram, Top View

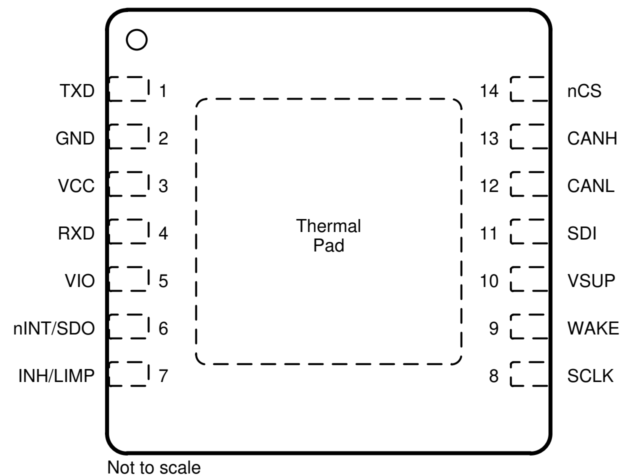

Figure 4-2. 14-pin VSON (DMT) Pin Diagram, Top View

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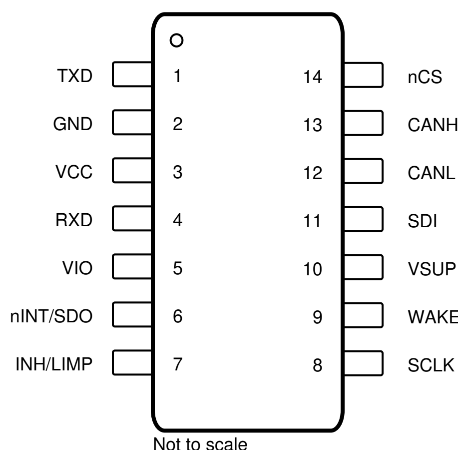

Figure 4-3. 14-pin SOT (DYY) Pin Diagram, Top View

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- All conditions are within recommended operating conditions
- VSUP = see recommended conditions in device data sheet
- VCC = 4.5 V to 5.5 V
- VIO = 1.71 V to 5.5 V

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Device will enter dominant time out mode. Unable to transmit data from processor to CAN bus	B
GND	2	None	D
VCC	3	Transceiver unpowered, high I_{CC} current	B
RXD	4	Transceiver output biased dominant. Unable to send data from CAN bus to processor	B
VIO	5	Digital pins unpowered, high I_{IO} current. No communiation between device and processor possible	B
SDO	6	SDO biased low, no SPI read capability from device to processor	B
INH	7	INH will not function, excessive VSUP current and not able to perform power enable function	B
SCLK	8	SCLK biased low, no SPI read/write capability between device and processor	B
WAKE	9	Will not be able to transition to high, which will not allow device to recognize a local wake up function	B
VSUP	10	Device unpowered, high I_{SUP} current.	B
SDI	11	SDI biased low, no SPI write capability from processor to device	B
CANL	12	$V_{O(REC)}$ spec violated. Degrade EMC performance	B
CANH	13	Device cannot drive dominant to the bus, no communication possible	B
nCS	14	nCS biased low, SPI always active	D

Note

The VSON (DMT) package includes a thermal pad that may or may not be soldered to GND.

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Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Unable to transmit data from processor to CAN bus	B
GND	2	Device is unpowered	B
VCC	3	Transceiver unpowered	B
RXD	4	Unable to send data from CAN bus to processor	B
VIO	5	Digital pins unpowered. No communication between device and processor possible	B
SDO	6	SDO internally biased to VIO. No SPI read capability from device to processor	B
INH	7	INH will not able to perform system power enable function	B
SCLK	8	SCLK internally biased to VIO. No SPI read/write capability between device and processor	B
WAKE	9	Will not be able to transition, which will not allow device to recognize a local wake up function	B
VSUP	10	Device unpowered	B
SDI	11	SDI internally biased to VIO. No SPI write capability from processor to device	B
CANL	12	Device cannot drive dominant to the bus, unable to communicate	B
CANH	13	Device cannot drive dominant to the bus, unable to communicate	B
nCS	14	nCS internally biased to VIO. No SPI read/write capability between device and processor	B

Note

The VSON (DMT) package includes a thermal pad that may or may not be soldered to GND

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	GND	Device will enter dominant time out mode. Unable to transmit data from processor to CAN bus	B
GND	2	VCC	Device unpowered, high I_{CC} current	B
VCC	3	RXD	RXD output biased recessive, unable to communicate bus data to processor.	B
RXD	4	VIO	RXD output biased recessive, unable to communicate bus data to processor.	B
VIO	5	SDO	No SPI read capability from device to processor	B
SDO	6	INH	SDO pin will be damaged due to high voltage	A
SCLK	8	WAKE	SCLK pin may be damaged if WAKE pin connected to VSUP	A
WAKE	9	VSUP	Will not be able to transition to low, which will not allow device to recognize a local wake up function	B
VSUP	10	SDI	SDI pin will be damaged and no SPI write communication from processor to device	A
SDI	11	CANL	SPI SDI bus line will toggle on and off based upon CAN traffic. During SPI communication CANL may toggle due to SDI traffic	B
CANL	12	CANH	Bus biased recessive, not communication possible. I_{OS} current may be reached on CANH/CANL	B
CANH	13	nCS	During SPI communication CANH may be biased dominant	B

Note

The VSON (DMT) package includes a thermal pad .

There is a chance the thermal pad if soldered down could short to any pin on device. What the thermal pad is soldered to determines the behavior.

Example: if soldered to a ground plane then the adjacent pins would behave as if shorted to ground.

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Table 4-5. Pin FMA for Device Pins Short-Circuited to VSUP supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	Absolute maximum violation, pin may be damaged. Unable to communicate from processor to CAN bus	A
GND	2	Device unpowered, high I_{SUP} current, may damage device	A
VCC	3	Absolute maximum violation, pin may be damaged. Unable to communicate from processor to CAN bus	A
RXD	4	Absolute maximum violation, pin may be damaged. Unable to communicate from CAN bus to processor	A
VIO	5	Absolute maximum violation, pin may be damaged	A
SDO	6	Absolute maximum violation, pin may be damaged. No SPI read capability from device to processor	A
INH	7	INH will be biased on and will not be able to turn off	B
SCLK	8	Absolute maximum violation, pin may be damaged. No SPI read/write capability between device and processor	A
WAKE	9	Will not be able to transition which will not allow device to recognize a local wake up function	B
VSUP	10	None	D
SDI	11	Absolute maximum violation, pin may be damaged, no SPI write capability from processor to device	A
CANL	12	RXD biased recessive, no communication from CAN bus to processor possible. I_{OS} current may be reached	B
CANH	13	$V_{O(REC)}$ spec violated. May degrade EMC performance	C
nCS	14	Absolute maximum violation, transceiver may be damaged. No SPI read/write capability between device and processor	A

Note

The VSON (DMT) package includes a thermal pad

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Table 4-6. Pin FMA for Device Pins Short-Circuited to VCC supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD biased recessive. Unable to transmit data from processor to CAN bus. Processor may be damaged if VCC > VIO	B
GND	2	Device unpowered, high I_{CC} current	B
VCC	3	None	D
RXD	4	Transceiver output biased recessive. Unable to send data from CAN bus to processor. Processor may be damaged if VCC > VIO	B
VIO	5	IO pins will operate as 5V input/outputs. Processor may be damaged if VCC > VIO	C
SDO	6	No SPI read capability from device to processor. Processor may be damaged if VCC > VIO	B
INH	7	May damage transceiver as absolute maximum voltage on VCC may be exceeded	A
SCLK	8	No SPI read/write capability between device and processor. Processor may be damaged if VCC > VIO	B
WAKE	9	May damage transceiver as absolute maximum voltage on VCC may be exceeded. May not be able to transition states which will not allow device to recognize a local wake up function	A
VSUP	10	Absolute maximum violation on VCC, transceiver may be damaged. Unable to communicate from processor to CAN bus	A
SDI	11	No SPI write capability from processor to device. Processor may be damaged if VCC > VIO	B
CANL	12	RXD always recessive, no communication possible. I_{OS} current may be reached	B
CANH	13	$V_{O(REC)}$ spec violated, degraded EMC performance.	C
nCS	14	No SPI read/write capability between device and processor. Processor may be damaged if VCC > VIO	B

Note

The VSON (DMT) package includes a thermal pad

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Table 4-7. Pin FMA for Device Pins Short-Circuited to VIO supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD	1	TXD biased recessive. Unable to transmit data from processor to CAN bus	B
GND	2	Device unpowered, high I_{IO} current	B
VCC	3	IO pins will operate as 5V input/outputs. Processor may be damaged if VCC > VIO.	C
RXD	4	Transceiver output biased recessive. Unable to send data from CAN bus to processor	B
VIO	5	None	D
SDO	6	No SPI read capability from device to processor	B
INH	7	May damage transceiver as absolute maximum voltage on VIO may be exceeded	A
SCLK	8	SCLK biased high. No SPI read/write capability between device and processor	B
WAKE	9	May damage transceiver as absolute maximum voltage on VIO may be exceeded. May not be able to transition states which will not allow device to recognize a local wake up function	A
VSUP	10	Absolute maximum violation on VIO pin, transceiver may be damaged	A
SDI	11	SDI biased high. No SPI write capability from processor to device	B
CANL	12	RXD biased recessive, no communication from bus to processor. I_{OS} current may be reached if VIO ≥ 3.3V.	B
CANH	13	$V_{O(REC)}$ spec violated. May degrade EMC performance	C
nCS	14	nCS biased high. No SPI read/write capability between device and processor	B

Note

The VSON (DMT) package includes a thermal pad

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