Application Report

BQ77915 Functional Safety FIT Rate, FMD, and Pin FMA

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1 Overview

This document contains information for BQ77915 (PW [TSSOP] package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

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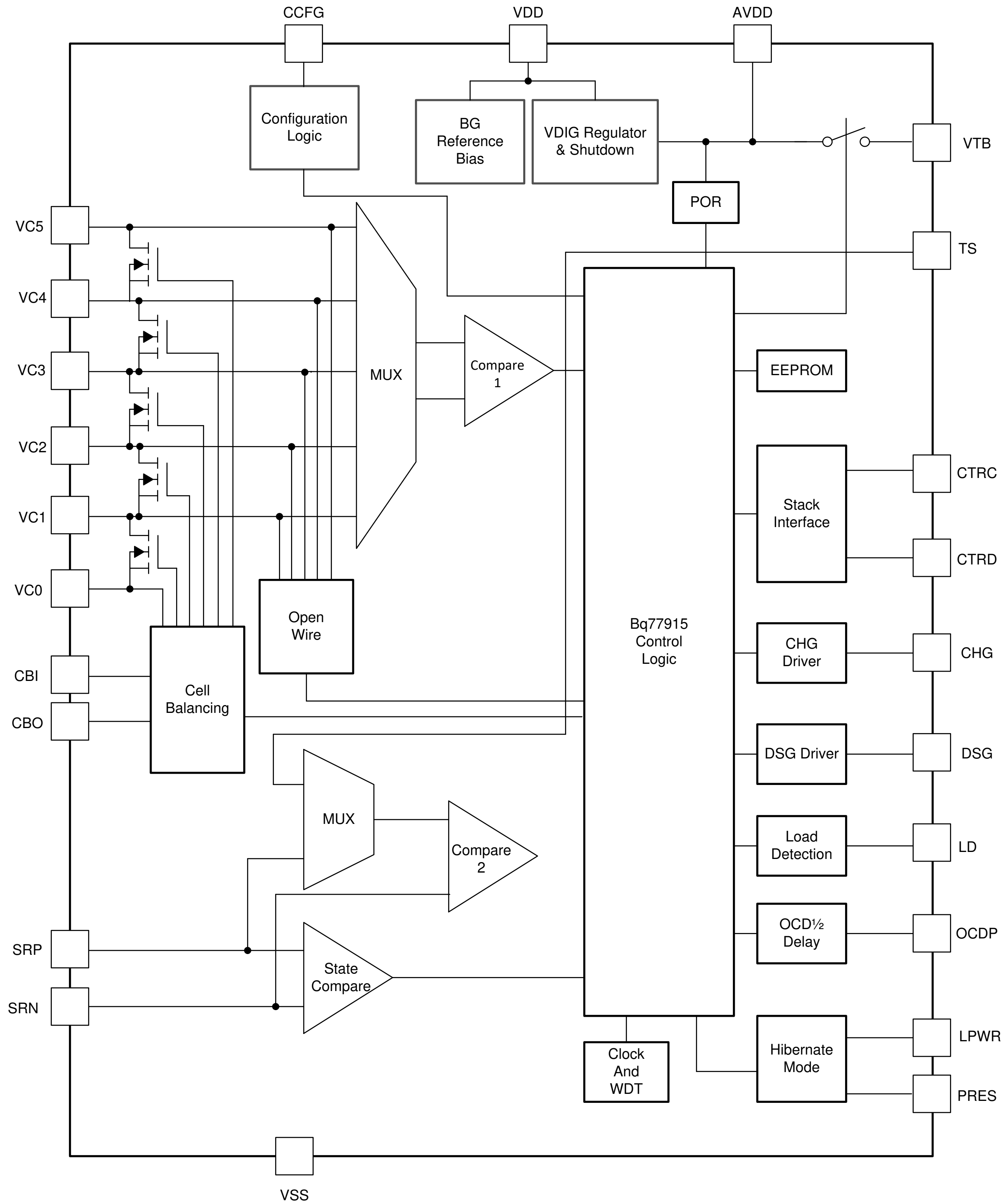

Figure 1-1. Functional Block Diagram

The BQ77915 device was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for BQ77915 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	17
Die FIT Rate	3
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1.0 mW TBD mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	**CMOS/BICMOS ASICs Analog and Mixed ≤50-V supply**	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for BQ77915 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Safe Faults	50%
Unsafe Faults	50%

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the BQ77915. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

The *Pin Diagram* represents the BQ779154 device pinout. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the BQ77915 data sheet.

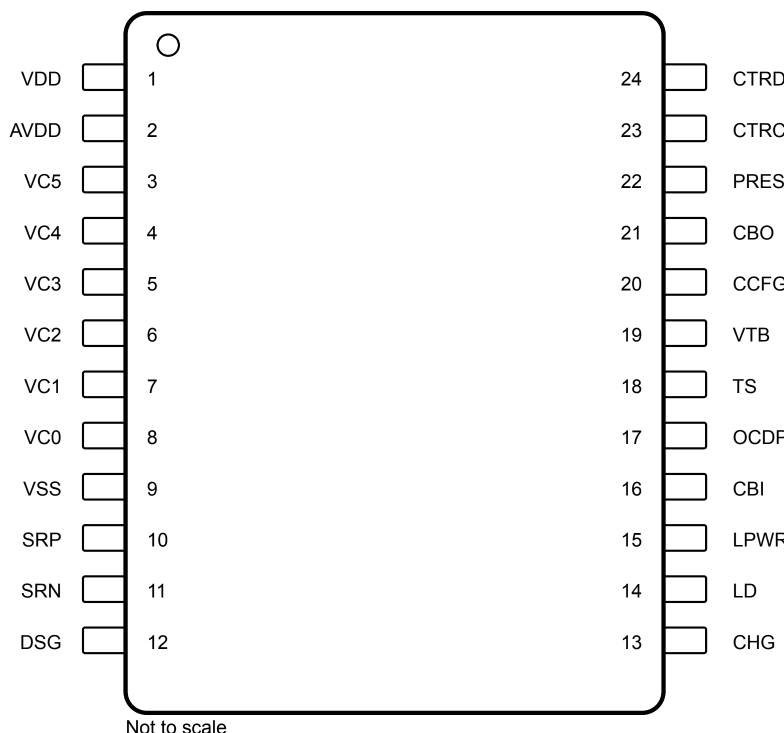

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	The device will not power up as the main supply is grounded. The device will remain in UVLO, CHG/DSG FET's will stay off.	B
AVDD	2	DPOR_Z will go up, shutting off the device and turning off CHG/DSG FETS.	B

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VC5	3	UV comparator will trip for Cell 5, causing DSG FET to turn off and battery will no longer discharge.	B
VC4	4	UV comparator will trip for this cell or an OV event will be triggered for cell above, CHG/DSG FET will be turned off and battery will stop charging.	B
VC3	5	UV comparator will trip for this cell or an OV event will be triggered for cell above, CHG/DSG FET will be turned off and battery will stop charging.	B
VC2	6	UV comparator will trip for this cell or an OV event will be triggered for cell above, CHG/DSG FET will be turned off and battery will stop charging.	B
VC1	7	UV comparator will trip for this cell or an OV event will be triggered for cell above, CHG/DSG FET will be turned off and battery will stop charging.	B
VC0	8	VC0 is normally connected to ground through a resistor. No effect	D
VSS	9	No Effect	D
SRP	10	Since SRP is normally connected to ground node anyways, this will have no effect.	D
SRN	11	SRN will be grounded, keeping the voltage at the same potential as SRP. No overcurrent detections will be functional.	B
DSG	12	DSG fet will always be off, in addition a large amount of current will be seen into the DSG pin when the DSG driver is enabled, this could potential damage some of the components in the current path.	A
CHG	13	CHG fet will always be off, in addition a large amount of current will be seen into the CHG pin when the CHG driver is enabled, this could potential damage some of the components in the current path.	A
LD	14	Load detect will not function properly; load removal will be detected even when there is still a load.	B
LWPWR	15	Will stay in hibernate if stacking. With non-stacking, there will be short from AVDD to ground, causing AVDD to collapse and the device to POR.	B
CBI	16	Cell balancing will always be enabled, unable to shut off cell balancing.	B
OCDP	17	OCD delay programming will not be configured correctly, will always detect a 100-KΩ resistor, meaning delays will be determined by EEPROM delay options.	C
TS	18	Overvoltage (OT) fault will trigger, causing CHG/DSG FETs to turn off.	B
VTB	19	Overvoltage (OT) fault will trigger, causing CHG/DSG FETs to turn off.	B
CCFG	20	The device will always be in 4-series configuration, having any different cell config in the battery pack will cause a UV and DSG FET turn off.	B
CBO	21	For non-stacking configuration, no change. If in stacking configuration, top cell will always think cell balancing is enabled, will not be able to disable cell balancing.	B
PRES	22	The device would remain in HIBERNATE mode and would not be able to power up into NORMAL mode.	B
CTRC	23	CHG FET will function normally.	D
CTRD	24	Discharge FET will function normally.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	The device will not power up as no voltage would go to internal VDD, the device will remain in UVLO, CHG/DSG FET's will stay off	B
AVDD	2	Supply will still be connected to all of the analog blocks, but without the 1uF cap the supply will collapse more easily with a load transient or any other disturbance	C
VC5	3	The device will lose the ability for OV/UV detection of this cell	B
VC4	4	The device will lose the ability for OV/UV detection of this cell	B
VC3	5	The device will lose the ability for OV/UV detection of this cell	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VC2	6	The device will lose the ability for OV/UV detection of this cell	B
VC1	7	The device will lose the ability for OV/UV detection of this cell	B
VC0	8	The device will lose the ability for OV/UV detection of this cell	B
VSS	9	With substrate floating, power to the The device will be lost and the device will be non-functional.	B
SRP	10	Voltage at SRP will float and current measurements will be random, could have some false OCD triggerings, which would shut off the CHG/DSG FET.	B
SRN	11	Voltage at SRP will float and current measurements will be random, could have some false OCD triggerings, which would shut off the CHG/DSG FET.	B
DSG	12	DSG Fet will be disabled.	B
CHG	13	The Charge FET will be disabled.	B
LD	14	Load detect feature will not work as the LD pin will not have the voltage divider from the load connected. When a fault occurs the LD pin will be pulled to ground and stay there.	B
LWPWR	15	For single device, no performance difference. For stackable interface, hibernate will not function correctly.	B
CBI	16	CBI will be enabled, with stacked devices Cell balancing enable communications between top and bottom device will not work.	B
OCDP	17	OCD1/2 delay settings will always read as highest resistor option (750K), OCD delays will be set to highest number.	C
TS	18	Floating TS pin will give undesired results during over/under temperature checks. Possible false triggering would cause the CHG/DSG Fets to turn off and battery to stop charging/discharging.	B
VTB	19	Divider from VTB to gnd (through TS pin) will not be connected. TS pin will always be grounded, causing an overtemperature fault to occur. CHG/DSG FETs will be turned off.	B
CCFG	20	When this pin is floating, internal biasing will set this the device to 5-cell configuration. If battery pack is not actually configured in 5-series mode (4 series or 3 series), UV will be detected and DSG Fet will turn off	B
CBO	21	For non stacking configuration, there is no performance difference. For stacking configuration, top device will have cell balancing always disabled.	B
PRES	22	The device will remain in HIBERNATE mode, will not be able to power up into NORMAL mode.	B
CTRC	23	The voltage pin will float, if it rises above 0.6 V (VMIN) it will cause the CHG FET to shut off and device will not function.	B
CTRD	24	The voltage pin will float, if it rises above 0.6V (VMIN) it will cause the DSCHG FET to shut off and device will not discharge.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	AVDD	Short to AVDD:VDD high voltage will be applied to the AVDD pin, causing overvoltage stress on all the low voltage components attached to AVDD.	A
AVDD	2	VC5	Short to VC5: VC5 high voltage will be applied to the AVDD pin (from VDD or VC5), causing overvoltage stress on all the low voltage components attached to AVDD.	A
VC5	3	VC4	Short to VC4:UV comparator will trip for Cell 5, causing DSG FET to turn off and battery will stop discharging.	B
VC4	4	VC3	Short to VC3:OV/UV will be triggered for this cell or the cell above/below. CHG/DSG FET will be turned off and battery will stop charging.	B
VC3	5	VC2	Short to VC2:OV/UV will be triggered for this cell or the cell above/below. CHG/DSG FET will be turned off and battery will stop charging.	B
VC2	6	VC1	Short to VC1: OV/UV will be triggered for this cell or the cell above/below. CHG/DSG FET will be turned off and battery will stop charging.	B

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VC1	7	VC0	Short to VC0: OV/UV will be triggered for this cell or the cell above/below. CHG/DSG FET will be turned off and battery will stop charging.	B
VC0	8	VSS	Short to VSS: no change as VC0 is tied to ground through RIN resistor.	D
VSS	9	SRP	Short to SRP: since SRP is normally connected to ground node anyways, this will have no effect.	D
SRP	10	SRN	Short to SRN: SPR and SRN will be shorted together, none of the overcurrent protections will be functional .	B
SRN	11	DSG	SRN will see high voltage, causing the ESD clamp to activate, holding the pin ~ 4 V, potential damage will be done to components in the SRN path.	A
DSG	12	CHG	If a fault occurs that shuts just one of DSG/CHG off and not the other, this will cause a shoot through current through the NMOS and PMOS device drivers. A high amount of current will go from CHG/DSG rail to ground, either collapsing the supply and shutting all FETs off or causing damage due to high current.	A
CHG	13	LD	Short to LD: Load detect feature will not work as CHG pin will interfere with the RLD voltage divider. Load removal will not be detected.	B
LD	14	LWPWR	During load detect, a high voltage could possibly be seen at LPWR pin, causing ESD to fire and a lot of current to be sunk into LPWR pin, possibly causing damage to low voltage components on LPWR pin.	A
LWPWR	15	CBI	Short to CBI: If CBI is being driven low (Cell balancing enabled), short to CBI will cause AVDD to collapse as AVDD is shorted to ground through the LPWR-CBI pins.	B
CBI	16	OCDP	Short to OCDP: OCDP is shorted to ground through a resistor, CBI will be grounded and cell balancing will be always enabled. Will lose the ability to turn off cell balancing.	B
OCDP	17	TS	Short to TS: Temperature measurements will be skewed by current source dumping current into OCDP pin. The device will always measure colder.	C
TS	18	VTB	Short to VTB: TS pin will always be measured at VTB, which will trigger an under temperature fault. CHG FET will be turned off.	B
VTB	19	CCFG	short to CCFG: VTB will rotate between AVDD and ground during normal operation, therefore the CCFG will change from 3-series configuration to 4-series configuration (depending on the current state of VTB). This will cause UV protection to erroneously kick in and shut off the DSG FET.	B
CCFG	20	CBO	Short to CBO: if cell balance is enabled, CCFG will be pulled low, putting the device into 3 cell configuration and causing UV faults on cells 4 and 5.	B
CBO	21	PRES	Short to PRES: CBO will force PRES to ground, the device will enter hibernate mode and stay there.	B
PRES	22	CTRC	Short to CTRC: if hibernate is off, PRES pin is held at VDD. This high voltage if seen on CTRC will disable the FET driver and charging will no longer function.	B
CTRC	23	CTRD	Short to CTRD: both CHG and DSG Fets will follow what's indicated in CTRD/C, the device will no longer be able to independently control CHG/DSG.	B
CTRD	24	CTRC	Short to CTRD: both CHG and DSG FETs will follow what iss indicated in CTRD/C, the device will no longer be able to independently control CHG/DSG.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Normal operation, as this pin is the power.	D

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Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	2	AVDD will be shorted to high voltage, causing ESD clamp to kick in, clamping pin voltage to ~4V and causing a large amount of current to flow from VDD to AVDD, possibly causing damage from overheating.	A
VC5	3	Normal operation as VC5 is at same voltage as VDD (TOPSTACK).	D
VC4	4	Connection to supply will trigger an OV event or a UV event for the cell above, CHG/DSG FET will be turned off and battery will stop charging.	B
VC3	5	Connection to supply will trigger an OV event or a UV event for the cell above, CHG/DSG FET will be turned off and battery will stop charging.	B
VC2	6	Connection to supply will trigger an OV event or a UV event for the cell above, CHG/DSG FET will be turned off and battery will stop charging.	B
VC1	7	Connection to supply will trigger an OV event or a UV event for the cell above, CHG/DSG FET will be turned off and battery will stop charging.	B
VC0	8	The device will not power up as VC0 is tied to ground, the device will remain in UVLO, CHG/DSG FET's will stay off.	B
VSS	9	The device will not power up as the main supply is grounded. The device will remain in UVLO, CHG/DSG FETs will stay off.	B
SRP	10	High voltage will be applied to SRP, causing the ESD to trigger and clamp this pin around 4 V. A large amount of current will flow from VDD to SRP, possibly causing damage/overheating.	A
SRN	11	High voltage will be applied to SRN, causing the ESD to trigger and clamp this pin around 4 V. A large amount of current will flow from VDD to SRN, possibly causing damage/overheating.	A
DSG	12	When EN_DSG goes low, a large amount of current will flow from VDD to GND, potentially causing damage to components in the current path.	A
CHG	13	CHG pin will be (internally) clamped to 20 V, if a fault occurs that would pull down CHG a large amount of current will flow from CHG to ground, potentially damaging components in the current path.	A
LD	14	Load detect pin will be clamped (internally) to 18V, ~450 µA will be drawn from VDD through LD. Load detect feature will not function properly.	B
LWPWR	15	High voltage will be applied to LPWR pin, causing the ESD to trigger and clamp this pin around 4 V. A large amount of current will flow from VDD to LPWR, possibly causing damage/overheating.	A
CBI	16	High voltage will be applied to CBI pin, causing the ESD to trigger and clamp this pin around 4 V. A large amount of current will flow from VDD to CBI, possibly causing damage/overheating.	A
OCDP	17	High voltage will be applied to the OCDP pin, causing the ESD to trigger and clamp this pin around 4 V. A large amount of current will flow from VDD to OCDP, possibly causing damage/ overheating.	A
TS	18	Overvoltage on the pin will cause the ESD protection to activate, clamping the voltage at around 5 V. A high amount of current will flow from VDD through the TS pin, possibly causing damage and overstressing the components.	A
VTB	19	Overvoltage on the pin will cause the ESD protection to activate, clamping the voltage at around 5 V. A high amount of current will flow from VDD through theVTB pin, possibly causing damage and overstressing the components. The TS pin may also see high voltage through the voltage divider resistors.	A
CCFG	20	Overvoltage on the pin will cause the ESD protection to activate, clamping the voltage at around 5 V. A high amount of current will flow from VDD through the CCFG pin, possibly causing damage and overstressing components.	A
CBO	21	In stacked configuration, top device would not be able to be driven low to enable cell balancing. Cell balancing would remain disabled for top device.	B
PRES	22	The device will not be able to enter HIBERNATE mode as pin will be shorted to supply.	B
CTRC	23	Charge FET will be disabled; the device will not function.	B
CTRD	24	Discharge FET will be disabled;, the device will not function.	B

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