Application Report

BQ77904, BQ77905 Functional Safety FIT Rate, FMD, and Pin FMA

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1 Overview

This document contains information for BQ77904 and BQ77905 (TSSOP package) to aid in a functional safety system design. Information provided is as follows:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

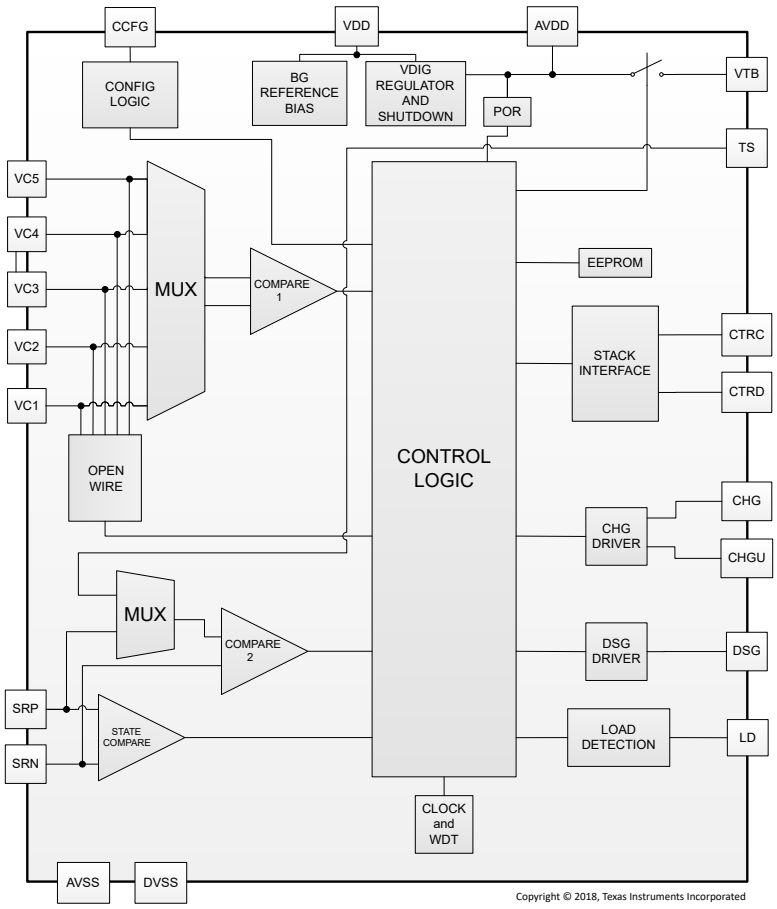

Figure 1-1. Functional Block Diagram

BQ77904 and BQ77905 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for BQ77904 and BQ77905, based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	14
Die FIT Rate	3
Package FIT Rate	11

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1.0 mW TBD mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed =<50V supply	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2, Section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for BQ77904, BQ77905 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Safe faults	50%
Unsafe faults	50%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the BQ77904, BQ77905. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the BQ77904, BQ77905 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the BQ77904, BQ77905 datasheet.

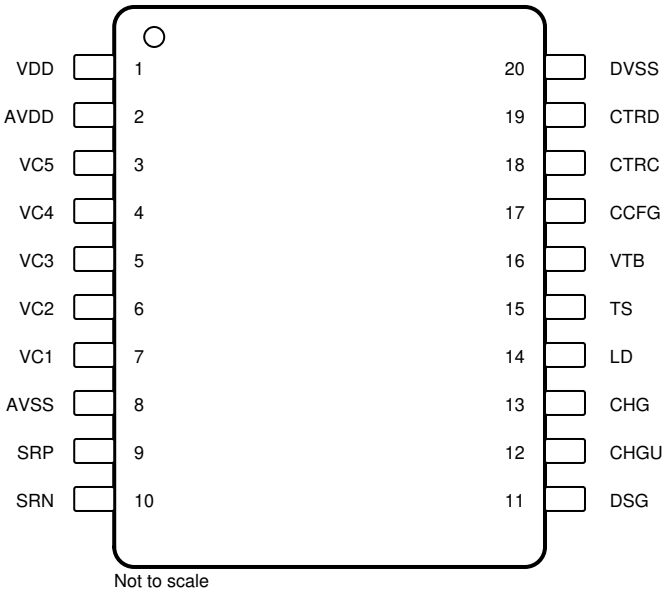

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Part will not power up as the main supply is grounded. Part will remain in UVLO, CHG/DSG FET's will stay off	B
AVDD	2	DPOR_Z will go up, shutting off part and turning off CHG/DSG FETS	B
VC5	3	UV comparator will trip for Cell 5, causing DSG FET to turn off and battery will no longer discharge	B
VC4	4	UV comparator will trip for this cell or an OV event will be triggered for cell above, CHG/DSG FET will be turned off and battery will stop charging	B

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VC3	5	UV comparator will trip for this cell or an OV event will be triggered for cell above, CHG/DSG FET will be turned off and battery will stop charging	B
VC2	6	UV comparator will trip for this cell or an OV event will be triggered for cell above, CHG/DSG FET will be turned off and battery will stop charging	B
VC1	7	UV comparator will trip for this cell or an OV event will be triggered for cell above, CHG/DSG FET will be turned off and battery will stop charging	B
AVSS	8	No Effect	D
SRP	9	Since SRP is normally connected to ground node anyways, this will have no effect	D
SRN	10	SRN will be grounded, keeping the voltage at the same potential as SRP. No overcurrent detections will be functional	B
DSG	11	DSG fet will always be off, in addition a large amount of current will be seen into the DSG pin when the DSG driver is enabled, this could potential damage some of the components in the current path.	A
CHGU	12	CHGU will be grounded, but large amount of current will flow through the driver when CHG_EN goes high, potentially damaging components in the current path	A
CHG	13	CHG fet will always be off, in addition a large amount of current will be seen into the CHG pin when the CHG driver is enabled, this could potential damage some of the components in the current path.	A
LD	14	Load detect will not function properly, Load removal will be detected even when there is still a load	B
TS	15	Overvoltage (OT) fault will trigger, causing CHG/DSG FETs to turn of	B
VTB	16	During TS measurment cycle, a large current ~5mA will flow from VDD to ground through the VTB pin. TS will be at 0V and and an overtemperature fault will trigger. CHG/DSG FETs will be turned off	B
CCFG	17	Part will always be in 4s configuration, having any different cell config in the battery pack will cause a UV and DSG FET turn off	B
CTRC	18	CHG FET will function normally	D
CTRD	19	Discharge FET will function normally	D
DVSS	20	No change, part will function normally	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Part will not power up as no voltage would go to internal VDD, part will remain in UVLO, CHG/DSG FET's will stay off.	B
AVDD	2	Supply will still be connected to all of the analog blocks, but without the 1uF cap the supply will collapse more easily with a load transient or any other disturbance.	C
VC5	3	Part will lose the ability for OV/UV detection of this cell.	B
VC4	4	Part will lose the ability for OV/UV detection of this cell.	B
VC3	5	Part will lose the ability for OV/UV detection of this cell.	B
VC2	6	Part will lose the ability for OV/UV detection of this cell.	B
VC1	7	Part will lose the ability for OV/UV detection of this cell.	B
AVSS	8	With substrate floating, power to the part will be lost and part will be non-functional.	B
SRP	9	Voltage at SRP will float and current measurements will be random, could have some false OCD triggerings, which would shut off the CHG/DSG FET.	B
SRN	10	Voltage at SRN will float and current measurements will be random, could have some false OCD triggerings, which would shut off the CHG/DSG FET	B
DSG	11	DSG Fet will be disabled.	B
CHGU	12	CHGU floating is not a problem, unless in stacked configuration. Part would lose stacking functionality.	B

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CHG	13	The Charge FET will be disabled.	B
LD	14	Load detect feature will not work as the LD pin will not have the voltage divider from the load connected. When a fault occurs the LD pin will be pulled to ground and stay there.	B
TS	15	Floating TS pin will give undesired results during over/under temperature checks. Possible false triggering would cause the CHG/DSG Fets to turn off and battery to stop charging/discharging.	B
VTB	16	Divider from VTB to gnd (through TS pin) will not be connected. TS pin will always be grounded, causing an overtemperature fault to occur. CHG/DSG FETs will be turned off.	B
CCFG	17	When this pin is floating, internal biasing will set this part to 5 cell configuration. If battery pack is not actually configured in 5s mode (4s or 3s), UV will be detected and DSG Fet will turn off.	B
CTRC	18	Voltage pin will float, if it rises above 0.6V (VMIN) it will cause the CHG FET to shut off and device will not function.	B
CTRD	19	Voltage pin will float, if it rises above 0.6V (VMIN) it will cause the DSCHG FET to shut off and device will not.	B
DVSS	20	Power to part will be lost, part will lose functionality.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	AVDD	Short to AVDD:VDD high voltage will be applied to the AVDD pin, causing overvoltage stress on all the low voltage components attached to AVDD.	A
AVDD	2	VC5	Short to VC5: VC5 high voltage will be applied to the AVDD pin (from VDD or VC5), causing overvoltage stress on all the low voltage components attached to AVDD.	A
VC5	3	VC4	Short to VC4:UV comparator will trip for Cell 5, causing DSG FET to turn off and battery will stop discharging.	B
VC4	4	VC3	Short to VC3:OV/UV will be triggered for this cell or the cell above/below. CHG/DSG FET will be turned off and battery will stop charging.	B
VC3	5	VC2	Short to VC2:OV/UV will be triggered for this cell or the cell above/below. CHG/DSG FET will be turned off and battery will stop charging.	B
VC2	6	VC1	Short to VC1: OV/UV will be triggered for this cell or the cell above/below. CHG/DSG FET will be turned off and battery will stop charging	B
VC1	7	AVSS	Short to AVSS: OV/UV will be triggered for this cell or the cell above/below. CHG/DSG FET will be turned off and battery will stop charging.	B
AVSS	8	SRP	Short to SRP: Since SRP is normally connected to ground node anyways, this will have no effect.	D
SRP	9	SRN	Short to SRN: SPR and SRN will be shorted together, none of the overcurrent protections will be functional.	B
SRN	10	DSG	Short to DSG: Overvoltage stress will occur, causing ESD on SRN to kick in and possible damage to the part.	A
DSG	11	CHGU	Short to CHGU: usually this would function without issues, unless a fault occurs that would turn one of CHG/DSG off and leave the other one on. In this case a large amount of current would flow across the drivers from supply to ground, potentially causing damage to components in the current path.	A
CHGU	12	CHG	Short to CHG: Part would lose stacking functionality as CHGU is used when device stacking is implemented.	B
CHG	13	LD	Short to LD: Load detect feature will not work as CHG pin will interfere with the RLD voltage divider. Load removal will not be detected.	B
LD	14	TS	Short to TS pin: if fault occurs, PACK -(minus) could potentionally go to high voltage and apply this high voltage to TS pin, causing potential voltage overstress to TS pin.	A
TS	15	VTB	Short to VTB: TS pin will always be measured at VTB, which will trigger an under temperature fault. CHG FET will be turned off.	B

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VTB	16	CCFG	Short to CCFG: VTB will rotate between AVDD and ground during normal operation, therefore the CCFG will change from 3s configuration to 4s configuration (depending on the current state of VTB). This will cause UV protection to erroneously kick in and shut off the DSG FET.	B
CCFG	17	CTRC	Short to CTRC: If CTRC is 0V, Part will configure in 3 cell configuration even if it's in 4/5 Cell config. Fault protections of higher cells will not function. If CTRC is stacked and voltage is greater than AVDD, high voltage will cause ESD to trigger and large currents will run through this pin.	A
CTRC	18	CTRD	Short to CTRD: both CHG and DSG Fets will follow what's indicated in CTRD/C, affect will be if DSCHG FET is disabled here CHG Fet will also be disabled.	B
CTRD	19	DVSS	Short to DVSS: CTRD will be grounded, indicating discharge FET should be on. Device will function normally.	D
DVSS	20	SRN	Short to SRN: Overcurrent protections will no longer function as SRP and SRN are at the same potential.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	Normal Operation, as this pin is the power.	D
AVDD	2	AVDD will be shorted to high voltage, causing ESD clamp to kick in, clamping pin voltage to ~4 V and causing a large amount of current to flow from VDD to AVDD, possibly causing damage from overheating.	A
VC5	3	Normal Operation as VC5 is at same voltage as VDD (TOPSTACK).	D
VC4	4	Connection to supply will trigger an OV event or a UV event for the cell above, CHG/DSG FET will be turned off and battery will stop charging.	B
VC3	5	Connection to supply will trigger an OV event or a UV event for the cell above, CHG/DSG FET will be turned off and battery will stop charging.	B
VC2	6	Connection to supply will trigger an OV event or a UV event for the cell above, CHG/DSG FET will be turned off and battery will stop charging.	B
VC1	7	Connection to supply will trigger an OV event or a UV event for the cell above, CHG/DSG FET will be turned off and battery will stop charging.	B
AVSS	8	Part will not power up as the main supply is grounded. Part will remain in UVLO, CHG/DSG FETs will stay off.	B
SRP	9	High voltage will be applied to SRP, causing the ESD to trigger and clamp this pin around 4 V. A large amount of current will flow from VDD to SRP, possibly causing damage/overheating.	A
SRN	10	High voltage will be applied to SRN, causing the ESD to trigger and clamp this pin around 4 V. A large amount of current will flow from VDD to SRN, possibly causing damage/overheating.	A
DSG	11	When EN_DSG goes low, a large amount of current will flow from VDD to gnd, potentially causing damage to components in the current path.	A
CHGU	12	When EN_CHG goes low, a large amount of current will flow from VDD to gnd, potentially causing damage to components in the current path.	A
CHG	13	CHG pin will be (internally) clamped to 20 V, if a fault occurs that would pull down CHG a large amount of current will flow from CHG to ground, potentially damaging components in the current path.	A
LD	14	Load detect pin will be clamped (internally) to 18 V, ~450 µA will be drawn from VDD through LD. Load detect feature will not function properly.	B
TS	15	Overvoltage on the pin will cause the ESD protection to activate, clamping the voltage at around 5 V. A high amount of current will flow from VDD through theTS pin, possibly causing damage and overstressing the components.	A

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VTB	16	Overvoltage on the pin will cause the ESD protection to activate, clamping the voltage at around 5 V. A high amount of current will flow from VDD through theVTB pin, possibly causing damage and overstressing the components. TS pin may also see high voltage through the voltage divider resistors.	A
CCFG	17	Overvoltage on the pin will cause the ESD protection to activate, clamping the voltage at around 5 V. A high amount of current will flow from VDD through the CCFG pin, possibly causing damage and overstressing the components.	A
CTRC	18	Charge FET will be disabled, part will not function	B
CTRD	19	Discharge FET will be disabled, part will not discharge	B
DVSS	20	Part will not power up as the main supply is grounded. Part will remain in UVLO, CHG/DSG FET's will stay off.	B

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