Functional Safety Information

LMR50410-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the LMR50410-Q1 in the SOT-23-6 package to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

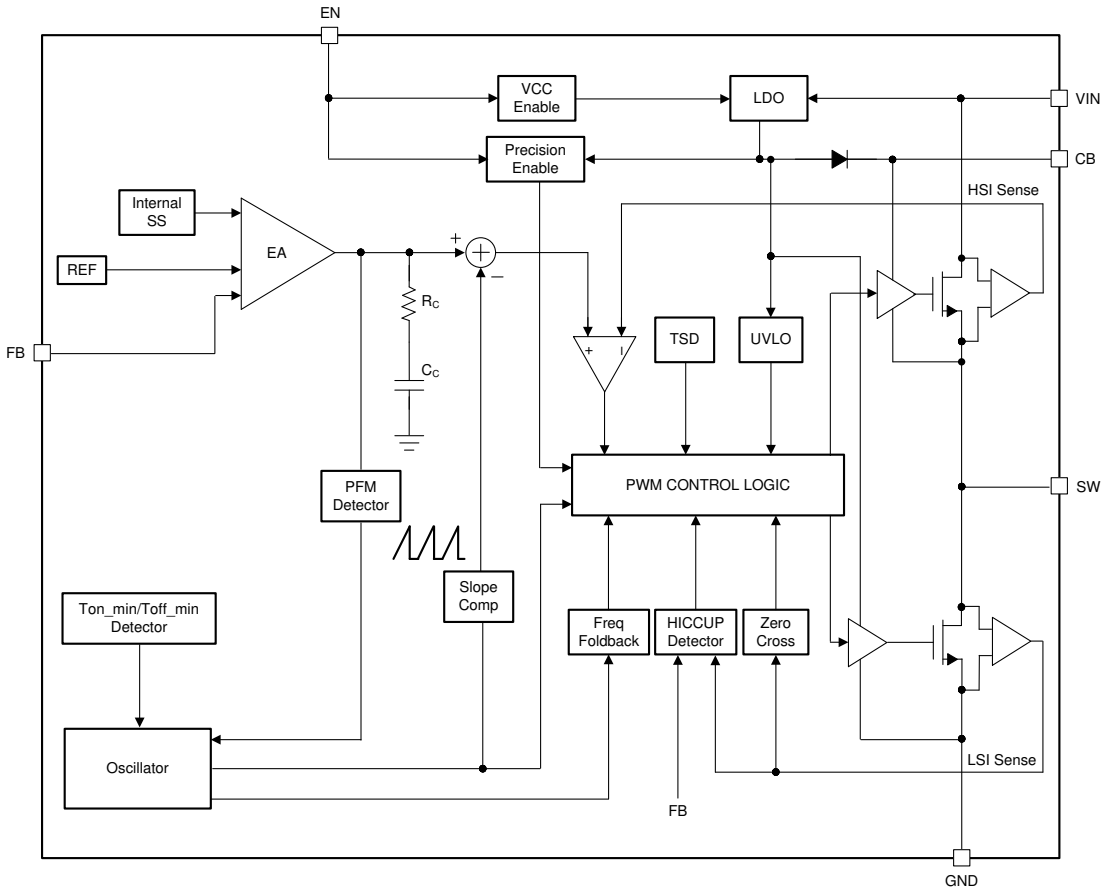

Figure 1-1. Functional Block Diagram

LMR50410-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR50410-Q1 in Table 2-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity are from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 2-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW Output	50%
SW output not in specification -- voltage or timing	45%
SW driver FET suck on	5%

3 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the LMR50410-Q1 based on the following two different industry-wide used reliability standards:

- Table 3-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 3-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 3-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	13
Die FIT Rate	10
Package FIT Rate	3

The failure rate and mission profile information in Table 3-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 250 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 3-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	**CMOS/BICMOS ASICs Analog & Mixed =<50V supply**	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 3-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LMR50410-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the '*Recommended Operating Conditions*' and the '*Absolute Maximum Ratings*' found in the appropriate device data sheet.
- Configuration as shown in the '*Example Application Circuit*' found in the appropriate device data sheet.

Figure 4-1 shows the LMR50410-Q1 pin diagram for the SOT-23-6 package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the appropriate device data sheet.

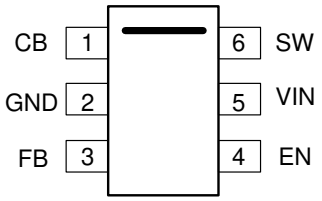

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CB	1	No output voltage	B
GND	2	Normal Operation	D
FB	3	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage (VIN) level. Possible damage to customer load and/or output stage components may occur. No effect on device.	B
EN	4	Loss of ENABLE functionality Device will remain in shut-down mode.	B
VIN	5	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A
SW	6	Damage to internal FET.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CB	1	No output voltage	B
GND	2	VOUT might be abnormal due to switching noise on analog circuits	B
FB	3	VOUT will be higher than programmed output voltage.	B
EN	4	Loss of ENABLE functionality. Erratic operation; probable loss of regulation.	B
VIN	5	No output voltage	B
SW	6	No output voltage	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
CB	1	GND	No output voltage	B
GND	2	FB	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage (VIN) level. Possible damage to customer load and/or output stage components may occur. No effect on device.	B
FB	3	GND	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage (VIN) level. Possible damage to customer load and/or output stage components may occur. No effect on device.	B
EN	4	VIN	No damage to device. Loss of ENABLE functionality.	B
VIN	5	SW	Damage to internal FET.	A
SW	6	VIN	Damage to internal FET.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CB	1	No output voltage. CBOOT ESD clamp will run current to destruction.	A
GND	2	No output voltage. Damage to other pins referred to GND.	A
FB	3	If VIN exceeds 16V damage will occur. No output voltage.	A
EN	4	No damage to device. Loss of ENABLE functionality.	B
VIN	5	No effect	D
SW	6	internal FET.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2020) to Revision A (October 2020)	Page
• Removed references of LMR50410	2

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265