Functional Safety Information

DRV8703-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for DRV8703-Q1 (VQFN (32) package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

DRV8703-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

Figure 1-1 shows the device functional block diagram for reference.

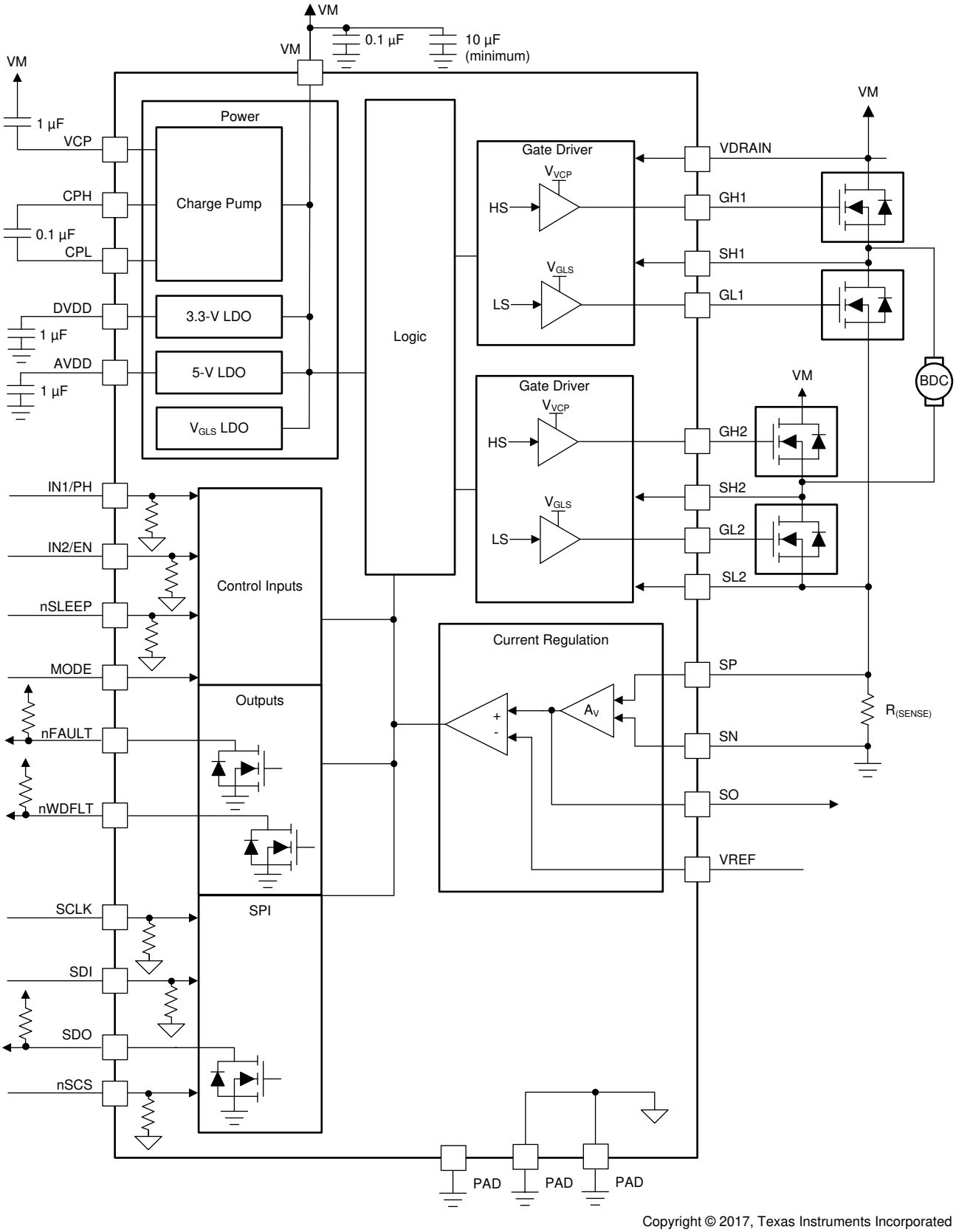

Figure 1-1. Functional Block Diagram

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for DRV8703-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	20
Die FIT Rate	3
Package FIT Rate	17

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 250 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS, Digital, analog/mixed	25 FIT	55 °C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for DRV8703-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Low side gate turned ON, when commanded OFF	20.5%
Low side gate turned OFF, when commanded ON	16.0%
Low side gate to source voltage too high or too low	0.5%
Low side gate driver slew rate too fast or too slow	2.5%
High side gate turned ON, when commanded OFF	20.5%
High side gate turned OFF, when commanded ON	15.0%
High side gate to source voltage too high or too low	0.5%
High side gate driver slew rate too fast or too slow	3.5%
Dead time between high side FET and low side FET transition incorrect	1.0%
Current sense feedback and regulation incorrect	6.0%
Drain Source voltage monitoring incorrect	4.0%
Incorrect communication or fault indication	10.0%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the DRV8703-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)

These PIN FMA tables also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the DRV8703-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the DRV8703-Q1 data sheet.

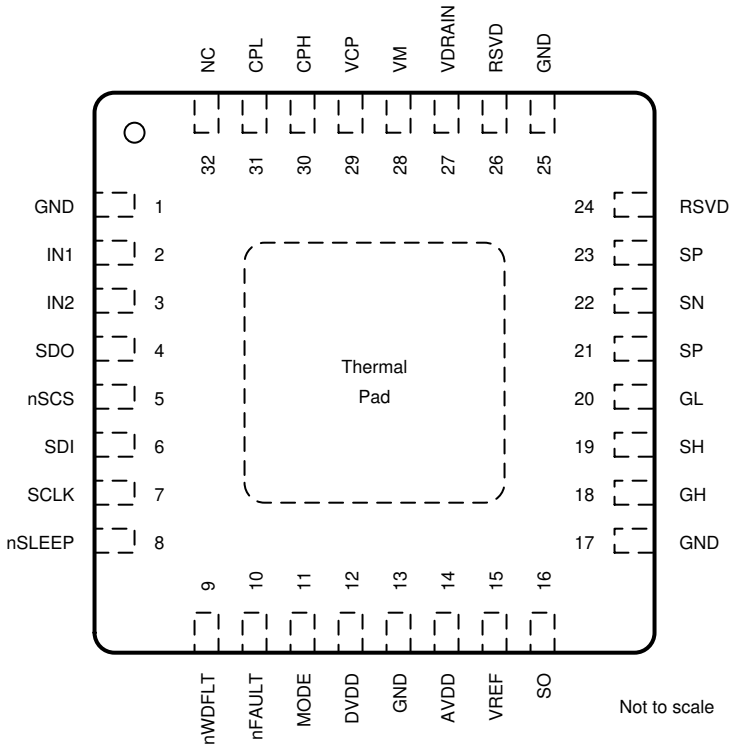

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used with external components consistent with the values described in the external component table of the datasheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Intended operation	D
IN1/PH	2	Gate driver input control stuck low. Driver output may not match input.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN2/EN	3	Gate driver input control stuck low. Driver output may not match input.	B
SDO	4	SPI communication compromised.	B
nSCS	5	SPI communication compromised.	B
SDI	6	SPI communication compromised.	B
SCLK	7	SPI communication compromised.	B
nSLEEP	8	Device stuck in sleep state. Outputs non-operational.	B
nWDFLT	9	Watchdog fault indication always enabled.	B
nFAULT	10	Device fault output indicator always active.	B
MODE	11	Device MODE setting potentially incorrect.	B
DVDD	12	Device external digital power supply stuck low. Device non-operational.	B
GND	13	Intended operation	D
AVDD	14	Device non-operational. Power dissipation through AVDD	B
VREF	15	Current limit will trip every cycle	B
SO	16	Device current sense feedback invalid.	B
GND	17	Intended operation	D
GH1	18	HS1 MOSFET off, energy limited by TDRIVE. Device will report VGS fault	B
SH1	19	HS1 MOSFET non-functional. Device will report VDS fault	B
GL1	20	LS1 MOSFET off, energy limited by TDRIVE. Device will report VGS fault	B
SP	21	Device current sense feedback invalid.	B
SN	22	Device current sense feedback invalid.	B
SL2	23	Sense amplifier output is always low, no current regulation	B
GL2	24	LS2 MOSFET off, energy limited by TDRIVE. Device will report VGS fault	B
SH2	25	HS2 MOSFET non-functional. Device will report VDS fault	B
GH2	26	HS2 MOSFET off, energy limited by TDRIVE. Device will report VGS fault	B
VDRAIN	27	Device overcurrent monitors and open load diagnostic non-operational.	B
PVDD	28	Device external power supply stuck low. Device gate drivers and shunt amplifier non-operational.	B
VCP	29	Device will be damaged	A
CPH	30	Device will be damaged	A
CPL	31	Device will report a charge pump fault	A
NC	32	No effect	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device behavior undefined, may retain operation due to alternative GND pin.	C
IN1/PH	2	Gate driver input control missing. Driver output may not match input.	B
IN2/EN	3	Gate driver input control missing. Driver output may not match input.	B
SDO	4	SPI communication compromised.	B
nSCS	5	SPI communication compromised.	B
SDI	6	SPI communication compromised.	B
SCLK	7	SPI communication compromised.	B
nSLEEP	8	Device stuck in sleep state. Outputs non-operational.	B
nWDFLT	9	Device Watchdog fault output indicator invalid.	B
nFAULT	10	Device fault output indicator invalid.	B
MODE	11	Device MODE setting potentially incorrect.	B
DVDD	12	Device external digital power supply missing. Device non-operational.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	13	Device behavior undefined, may retain operation due to alternative GND pin.	C
AVDD	14	Device behavior undefined, regulator may not be stable.	B
VREF	15	Current limit will be unstable	B
SO	16	Device current sense feedback invalid.	B
GND	17	Device behavior undefined, may retain operation due to alternative GND pin.	C
GH1	18	HS1 MOSFET off	B
SH1	19	HS1 MOSFET non-functional, Device will report VDS fault	B
GL1	20	LS1 MOSFET off	B
SP	21	Device current sense feedback invalid.	B
SN	22	Device current sense feedback invalid.	B
SL2	23	Device will report a VDS fault	B
GL2	24	LS2 MOSFET off	B
SH2	25	HS2 MOSFET non-functional, Device will report VDS fault	B
GH2	26	HS2 MOSFET off	B
VDRAIN	27	Device overcurrent monitors and open load diagnostic non-operational.	B
PVDD	28	Device external power supply missing. Device gate drivers and shunt amplifier non-operational.	B
VCP	29	Charge pump undervoltage and gate drivers disabled.	B
CPH	30	Charge pump undervoltage and gate drivers disabled.	B
CPL	31	Charge pump undervoltage and gate drivers disabled.	B
NC	32	Intended operation	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	2	Logic operation is changed. Driver output may not match input.	B
IN1/PH	2	3	Logic operation is changed. Driver output may not match input.	B
IN2/EN	3	4	Logic operation is changed. Driver output may not match input.	B
SDO	4	5	SPI communication compromised.	B
nSCS	5	6	SPI communication compromised.	B
SDI	6	7	SPI communication compromised.	B
SCLK	7	8	Device stuck in sleep state. Outputs non-operational.	B
nSLEEP	8	9	Watchdog and fault output indicator function compromised.	B
nWDFLT	9	10	Device fault output indicator always active.	B
nFAULT	10	11	MODE will change to PH/EN whenever a FAULT occurs and nSLEEP toggled	B
MODE	11	12	Device MODE setting potentially incorrect.	B
DVDD	12	13	Device external digital power supply missing. Device non-operational.	B
GND	13	14	Device non-operational. Power dissipation through AVDD	B
AVDD	14	15	Current regulation disabled	B
VREF	15	16	Device current sense feedback invalid.	B
SO	16	17	Device current sense feedback invalid.	B
GND	17	18	HS1 MOSFET off, energy limited by TDRIVE. Device will report VGS fault	B
GH1	18	19	HS1 MOSFET off, energy limited by TDRIVE. Device will report VGS fault	B
SH1	19	20	GL1 output invalid, may violate GL1 abs max.	A
GL1	20	21	LS1 MOSFET off, energy limited by TDRIVE. Device will report VGS fault	B
SP	21	22	Device current sense feedback invalid.	B
SN	22	23	Device current sense feedback invalid.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
SL2	23	24	LS2 MOSFET off, energy limited by TDRIVE. Device will report VGS fault	B
GL2	24	25	GL2 output invalid, may violate GL2 abs max.	A
SH2	25	26	HS2 MOSFET off, energy limited by TDRIVE. Device will report VGS fault	B
GH2	26	27	HS2 MOSFET off, energy limited by TDRIVE. Device will report VGS fault	B
VDRAIN	27	28	Hard short instead of a kelvin connection may degrate VDS accuracy	B
PVDD	28	29	Device will report a charge pump fault	A
VCP	29	30	Device will not power up	A
CPH	30	31	Device will report a charge pump fault	A
CPL	31	32	No effect	B
NC	32	1	No effect	B

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