Application Report
SNVA920A–January 2020–Revised April 2020

LM61435-Q1, LM61440-Q1, and LM61460-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for LM61435-Q1, LM61440-Q1, and LM61460-Q1 (VQFN-HR package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

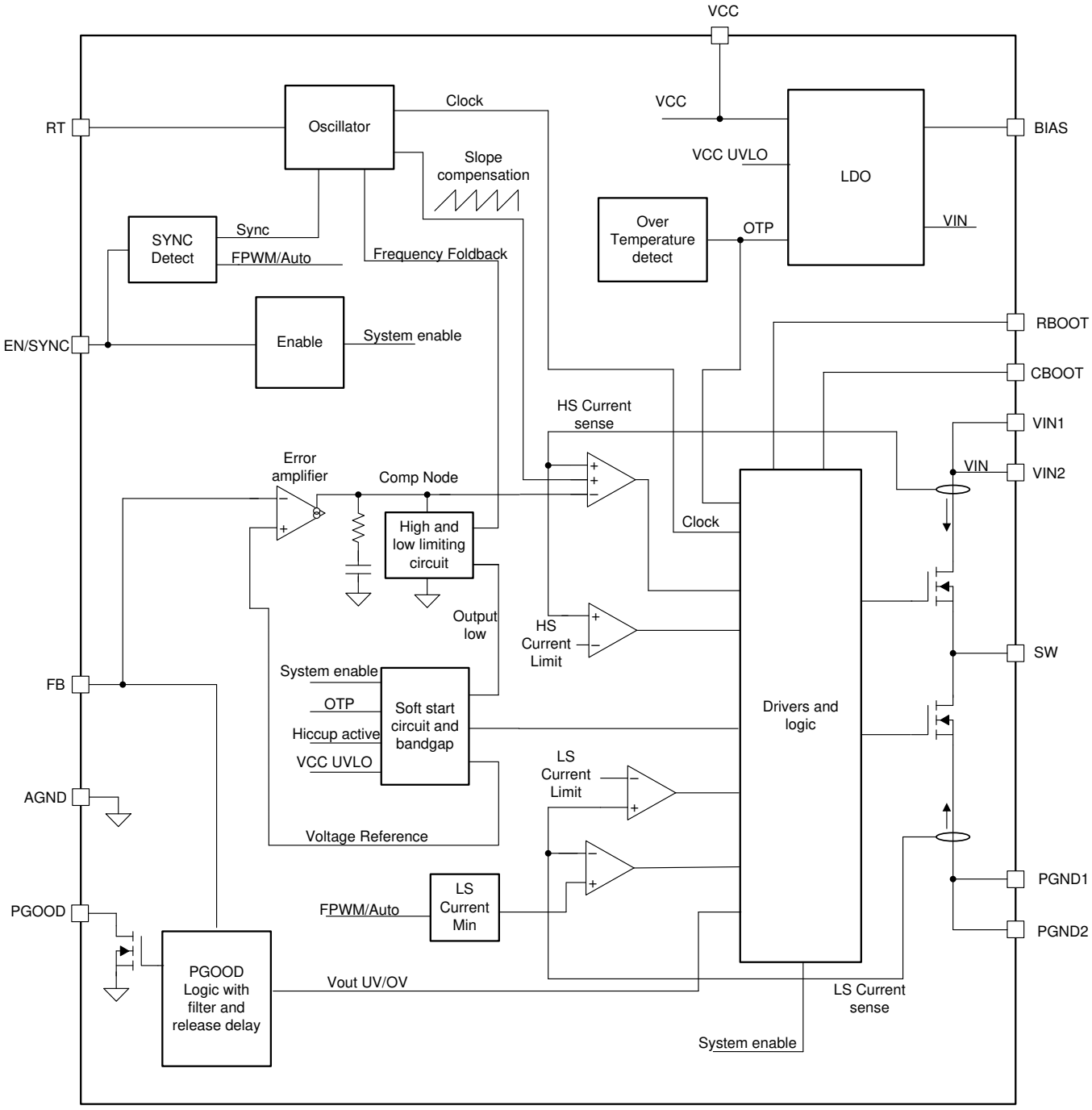

Figure 1. Functional Block Diagram

LM61435-Q1, LM61440-Q1, and LM61460-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM61435-Q1, LM61440-Q1, and LM61460-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	17
Die FIT Rate	9
Package FIT Rate	8

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 600mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BiPolar	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM61435-Q1, LM61440-Q1, and LM61460-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW No output	45%
SW output not in specification - voltage or timing	40%
SW power FET stuck on	5%
PGOOD false trip, fails to trip	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM61435-Q1, LM61440-Q1, and LM61460-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin open-circuited (see Table 6)
- Pin short-circuited to an adjacent pin (see Table 7)
- Pin short-circuited to supply (see Table 8)

Table 5 through Table 8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 2 shows the LM61435-Q1, LM61440-Q1, and LM61460-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the LM61435-Q1, LM61440-Q1, and LM61460-Q1 datasheet.

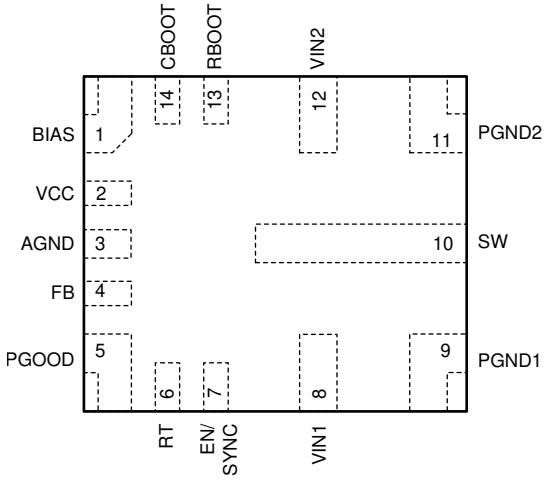

Figure 2. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the LM61460-Q1 data sheet is used.

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	Normal Operation	D
VCC	2	VOUT=0V	B
AGND	3	Normal Operation	D
FB	4	VOUT >> than programmed output voltage.	B
PGOOD	5	PGOOD not valid signal. VOUT in regulation	D
RT	6	VOUT=0V	B
EN/SYNC	7	VOUT=0V	B
VIN1	8	VOUT=0V	B
PGND1	9	VOUT normal	D
SW	10	Damage to HS FET	A
PGND2	11	VOUT normal	D
VIN2	12	VOUT=0V	B
RBOOT	13	VOUT=0V	A
CBOOT	14	VOUT=0V	B

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	Normal Operation	D
VCC	2	VCC output will be unstable and can increase above 5.5V rating of VCC pin	A
AGND	3	VOUT might be abnormal due to switching noise on analog circuits	B
FB	4	VOUT >> than programmed output voltage.	B
PGOOD	5	PGOOD not valid signal. VOUT in regulation	D
RT	6	VOUT=0V	B
EN/SYNC	7	VOUT=0V	B
VIN1	8	VOUT normal. Current loop will be affected, potentially affecting noise/jitter/EMI/reliability.	C
PGND1	9	VOUT normal. Current loop will be affected, potentially affecting noise/jitter/EMI/reliability.	C
SW	10	VOUT=0V	B
PGND2	11	VOUT normal. All current will be in this loop, potentially affecting noise/jitter/EMI/reliability.	C
VIN2	12	VOUT normal. All current will be in this loop, potentially affecting noise/jitter/EMI/reliability.	C
RBOOT	13	VOUT normal	D
CBOOT	14	VOUT=0V	B

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	VCC ESD clamp damaged if BIAS > 5V.	A
VCC	2	VOUT=0V	B
AGND	3	VOUT >> than programmed output voltage.	B
FB	4	VOUT=0V, Damage if PGOOD>16V	A
PGOOD	5	VOUT=0V	B
RT	6	VOUT=0V, Damage if EN/SYNC>5.5V	A
EN/SYNC	7	VOUT normal	D
VIN1	8	VOUT=0V	B
PGND1	9	VOUT=0V. Damage to low-side circuitry if PGND >> AGND	B
SW	10	Damage to HS FET	A
PGND2	11	VOUT=0V. Damage to low-side circuitry if PGND >> AGND	B
VIN2	12	VOUT=0V	B
RBOOT	13	VOUT normal	D
CBOOT	14	VOUT=0V	B

Table 8. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	If VIN exceeds 16V damage will occur. If below, normal operation	A
VCC	2	If VIN exceeds 5.5V damage will occur.	A
AGND	3	VOUT=0V. Damage to other pins referred to GND.	A
FB	4	If VIN exceeds 16V damage will occur. VOUT=0V.	A
PGOOD	5	VOUT=0V. PGOOD ESD clamp will run current to destruction	A
RT	6	VOUT=0V	B
EN/SYNC	7	VOUT normal	D
VIN1	8	Normal Operation	D
PGND1	9	VOUT=0V. Damage to low-side circuitry if PGND >> AGND	B
SW	10	Damage to LS FET	A
PGND2	11	VOUT=0V. Damage to low-side circuitry if PGND >> AGND	B
VIN2	12	Normal Operation	D
RBOOT	13	VOUT=0V. RBOOT ESD clamp will run current to destruction.	A
CBOOT	14	VOUT=0V. CBOOT ESD clamp will run current to destruction.	A

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2020) to A Revision	Page
• Added *Section 4*	5

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