

LM62460-Q1, LM61480-Q1, and LM61495-Q1 Functional Safety FIT Rate, FMD and Pin FMA



Table of Contents

| | |
|--|----|
| 1 Overview..... | 2 |
| 2 Functional Safety Failure In Time (FIT) Rates..... | 3 |
| 3 Failure Mode Distribution (FMD) | 4 |
| 4 Pin Failure Mode Analysis (Pin FMA) | 5 |
| 5 Revision History..... | 10 |

1 Overview

This document contains information for LM62460-Q1, LM61480-Q1, and LM61495-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

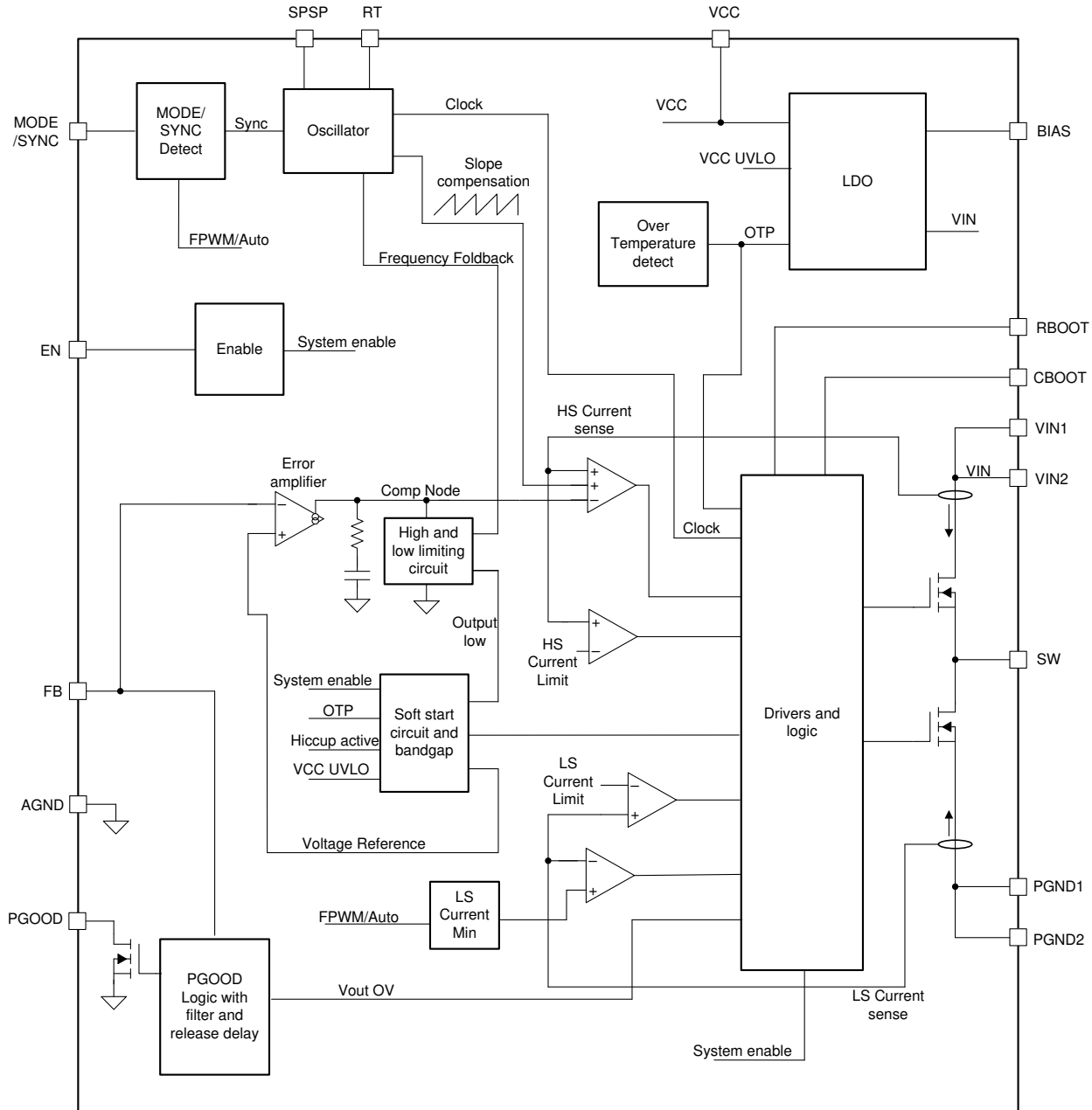


Figure 1-1. Functional Block Diagram

LM62460-Q1, LM61480-Q1, and LM61495-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM62460-Q1, LM61480-Q1, and LM61495-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per 10 ⁹ Hours) |
|------------------------------|--|
| Total Component FIT Rate | 26 |
| Die FIT Rate | 9 |
| Package FIT Rate | 17 |

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 800mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

| Table | Category | Reference FIT Rate | Reference Virtual T _J |
|-------|--|--------------------|----------------------------------|
| 5 | CMOS/BICMOS ASICs Analog & Mixed = < 50-V supply | 25 FIT | 55°C |

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM62460-Q1, LM61480-Q1, and LM61495-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

| Die Failure Modes | Failure Mode Distribution (%) |
|--|-------------------------------|
| SW No output | 50% |
| SW output not in specification - voltage or timing | 40% |
| SW power FET stuck on | 5% |
| PGOOD false trip, fails to trip | 5% |

The FMD in [Table 3-1](#) excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM62460-Q1, LM61480-Q1, and LM61495-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

| Class | Failure Effects |
|-------|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

[Figure 4-1](#) shows the LM62460-Q1, LM61480-Q1, and LM61495-Q1 pin diagram. For a detailed description of the device pins please refer to the 'Pin Configuration and Functions' section in the LM62460-Q1, LM61480-Q1, and LM61495-Q1 datasheet.

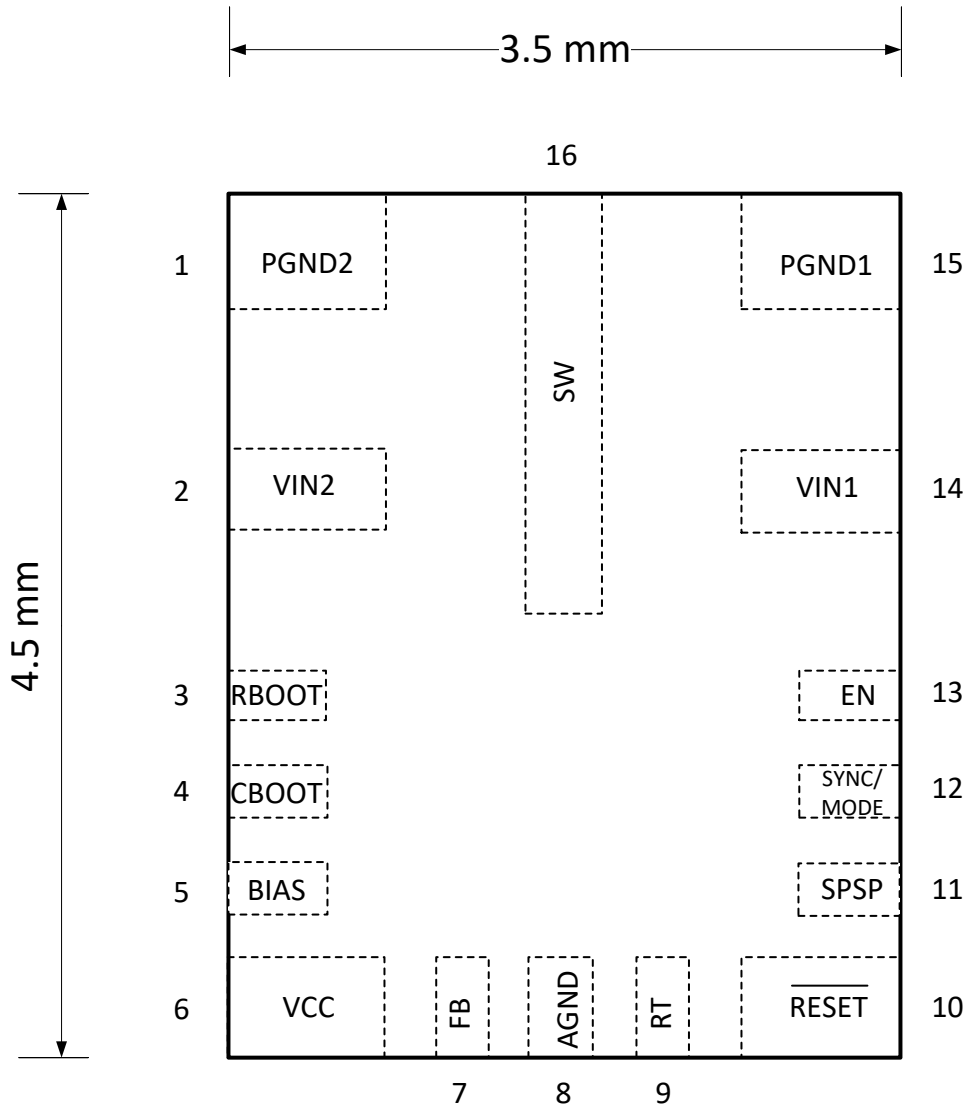


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the [LM61495-Q1 data sheet](#) is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

| Pin Name | Pin No | Description of Potential Failure Effect(s) | Failure Effect Class |
|-----------|--------|--|----------------------|
| PGND2 | 1 | Normal Operation | D |
| VIN2 | 2 | VOUT = 0 V | B |
| RBOOT | 3 | VOUT = 0 V, damage if VIN > 5.5 V | A |
| CBOOT | 4 | VOUT = 0 V | B |
| BIAS | 5 | Normal Operation | D |
| VCC | 6 | VOUT = 0 V | B |
| FB | 7 | VOUT >> than programmed output voltage | B |
| AGND | 8 | Normal Operation | D |
| RT | 9 | Switch frequency = 2.2 MHz | C |
| RESET | 10 | RESET value not valid. VOUT normal | D |
| SPSP | 11 | Spread spectrum off | C |
| SYNC/MODE | 12 | Mode = Auto PFM at light load. VOUT normal | C |
| EN | 13 | VOUT = 0 V | B |
| VIN1 | 14 | VOUT = 0 V | B |
| PGND1 | 15 | Normal Operation | D |
| SW | 16 | Damage to HS FET | A |

Table 4-3. Pin FMA for Device Pins Open-Circuited

| Pin Name | Pin No | Description of Potential Failure Effect(s) | Failure Effect Class |
|-----------|--------|---|----------------------|
| PGND2 | 1 | VOUT normal. Current loop will be affected, potentially affecting noise/jitter/EMI/reliability. | C |
| VIN2 | 2 | VOUT normal. All current will be in other VIN1 loop, potentially affecting noise/jitter/EMI/reliability | C |
| RBOOT | 3 | VOUT normal, lower efficiency, higher junction temp | C |
| CBOOT | 4 | VOUT = 0 V | B |
| BIAS | 5 | Normal Operation | D |
| VCC | 6 | VCC output can oscillate and internal circuitry may not function correctly | B |
| FB | 7 | VOUT >> than programmed output voltage | B |
| AGND | 8 | VOUT might be abnormal due to switching noise on analog circuits | B |
| RT | 9 | Switch frequency may become unstable | B |
| RESET | 10 | RESET signal not valid. Normal operation | C |
| SPSP | 11 | Spread spectrum enable/disable can be unstable | C |
| SYNC/MODE | 12 | Mode may switch randomly. Unpredictable behavior | C |
| EN | 13 | Device can shut off | B |
| VIN1 | 14 | VOUT normal. All current will be in other VIN2 loop, potentially affecting noise/jitter/EMI/reliability | C |
| PGND1 | 15 | VOUT normal. Current loop will be affected, potentially affecting noise/jitter/EMI/reliability. | C |
| SW | 16 | VOUT = 0 V | B |

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

| Pin Name | Pin No | Description of Potential Failure Effect(s) | Failure Effect Class |
|-----------|--------|---|----------------------|
| PGND2 | 1 | VOUT = 0 V. Damage to low-side circuitry if PGND >> AGND | B |
| VIN2 | 2 | VOUT = 0 V | B |
| RBOOT | 3 | VOUT normal | D |
| CBOOT | 4 | VOUT = 0 V | B |
| BIAS | 5 | VCC ESD clamp damaged if BIAS > 5 V | A |
| VCC | 6 | VOUT = 0 V | C |
| FB | 7 | VOUT >> than programmed output voltage | B |
| AGND | 8 | Switch frequency = 2.2 MHz | C |
| RT | 9 | Switch frequency may change, RT can become damaged if RESET > 5.5 V. RESET may not be valid | B |
| RESET | 10 | Spread spectrum can enable/disable, RESET can become damaged if biased above 20 V. | A |
| SPSP | 11 | Spread spectrum, sync, and mode functionality can be unstable. | C |
| SYNC/MODE | 12 | Can disable device, change modes, or interrupt syncing | B |
| EN | 13 | Device enabled | B |
| VIN1 | 14 | VOUT = 0 V. Damage to low-side circuitry if PGND >> AGND | B |
| PGND1 | 15 | VOUT = 0 V. Damage to low-side circuitry if PGND >> AGND | B |
| SW | 16 | Damage to HS FET | A |

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

| Pin Name | Pin No | Description of Potential Failure Effect(s) | Failure Effect Class |
|-----------|--------|---|----------------------|
| PGND2 | 1 | VOUT = 0 V. Damage to low-side circuitry if PGND >> AGND | B |
| VIN2 | 2 | Normal operation | D |
| RBOOT | 3 | VOUT = 0 V. RBOOT ESD clamp will run current to destruction. | A |
| CBOOT | 4 | VOUT = 0 V. CBOOT ESD clamp will run current to destruction. | A |
| BIAS | 5 | If VIN exceeds 16 V damage will occur. If below, normal operation | A |
| VCC | 6 | If VIN exceeds 5.5 V damage will occur. | A |
| FB | 7 | If VIN exceeds 16 V (fixed version) or 5.5 V (adjustable version) damage will occur. VOUT = 0 V | A |
| AGND | 8 | VOUT = 0 V. Damage to other pins referred to GND. | A |
| RT | 9 | If VIN exceeds 5.5 V damage will occur. VOUT = 0 V | A |
| RESET | 10 | If VIN exceeds 20 V damage will occur. VOUT = 0 V | A |
| SPSP | 11 | Spread spectrum enabled | D |
| SYNC/MODE | 12 | Mode set to FPWM | C |
| EN | 13 | Device enabled | C |
| VIN1 | 14 | Normal operation | D |
| PGND1 | 15 | VOUT = 0 V. Damage to low-side circuitry if PGND >> AGND | B |
| SW | 16 | Damage to LS FET | A |

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2020) to Revision A (April 2021)

Page

- Updated [Table 4-3](#) 5

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated