ABSTRACT

This application report provides a summary of the differences between the RM42x versus the RM48x and RM46x series of microcontrollers.

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1 Introduction

The RM42x series incorporates a subset of the functionality incorporated on the RM48x and RM46x series. There are some enhancements implemented on the RM42x similar to the enhancements implemented on the RM46x series vs the overall superset RM48x series, while still maintaining application code compatibility to the overall superset series when the code is targeted to the subset functionality. An application written for the RM48x or RM46x series runs correctly on the RM42x series as long as only the common functions and features are exercised.

A product overview can be found in the Hercules Product Brochure that outlines content differences between all three series of devices.
2 Memory Configuration Differences

The memory configurations of each of the three series of microcontrollers are different. In each series, the memories are sized according to the targeted applications. Table 1 shows the primary memory spaces within each series of microcontrollers in order to highlight the differences.

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>RM48x</th>
<th>RM46x</th>
<th>RM42x</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash: Program Memory</td>
<td>3MB/2MB</td>
<td>1.25MB/1MB</td>
<td>384kB</td>
</tr>
<tr>
<td>Flash: Boot Sector</td>
<td>1 X 32kB Sector</td>
<td>Up to 2 X 16kB Sectors</td>
<td>Up to 12 X 8kB sectors</td>
</tr>
<tr>
<td>Flash: EEPROM Emulation</td>
<td>4 X 16kB Sectors</td>
<td>4 X 16kB Sectors</td>
<td>4 X 4kB Sectors</td>
</tr>
<tr>
<td>CPU Data RAM</td>
<td>Up to 256kB</td>
<td>Up to 192kB</td>
<td>32kB</td>
</tr>
<tr>
<td>MibADC1 RAM</td>
<td>64 Result Buffers</td>
<td>64 Result Buffers</td>
<td>64 Result Buffers</td>
</tr>
<tr>
<td>MibADC2 RAM</td>
<td>64 Result Buffers</td>
<td>64 Result Buffers</td>
<td>N/A</td>
</tr>
<tr>
<td>N2HET1 RAM</td>
<td>160 Instruction RAM</td>
<td>160 Instruction RAM</td>
<td>128 Instruction RAM</td>
</tr>
<tr>
<td>N2HET RAM</td>
<td>160 Instruction RAM</td>
<td>160 Instruction RAM</td>
<td>N/A</td>
</tr>
<tr>
<td>DCAN1 RAM</td>
<td>64 Mailboxes</td>
<td>64 Mailboxes</td>
<td>32 Mailboxes</td>
</tr>
<tr>
<td>DCAN2 RAM</td>
<td>64 Mailboxes</td>
<td>64 Mailboxes</td>
<td>16 Mailboxes</td>
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<td>DCAN3 RAM</td>
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<td>64 Mailboxes</td>
<td>N/A</td>
</tr>
<tr>
<td>MibSPI1 RAM</td>
<td>128 Words</td>
<td>128 Words</td>
<td>128 Words</td>
</tr>
<tr>
<td>MibSPI3 RAM</td>
<td>128 Words</td>
<td>128 Words</td>
<td>N/A</td>
</tr>
<tr>
<td>MibSPI5 RAM</td>
<td>128 Words</td>
<td>128 Words</td>
<td>N/A</td>
</tr>
<tr>
<td>FlexRay RAM</td>
<td>8kB Message RAM</td>
<td>8kB Message RAM</td>
<td>N/A</td>
</tr>
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</table>

3 Package Compatibility Considerations

Both the RM48x and RM46x series of microcontrollers are supported in either a 337 ball grid array (337 BGA) or a 144-pin quad flat pack (144 QFP) package. The RM42x series of devices is available in a 100-pin quad flat pack (100 QFP) package.

3.1 Pin-Out Compatibility

Given that the RM42x series of microcontrollers is not available in a common package or pinout with the RM48x and RM46x series of microcontrollers, an effort was made to insure there was functional compatibility between the series of devices such that the subset series could be easily adapted into a design that previously had used the super set series. This is accomplished by making each side of the family of devices very similar in order to minimize PCB layout migration issues when going from 144-pin to 100-pin devices. Table 2 demonstrates how the default functional pins of the 100QFP package for the RM42x series map to the subset of default functional pins of the 144QFP on the RM48x and RM46x series of microcontrollers.

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name/Function</th>
<th>Pin Name/Function</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GiOA[0]/INT[0]</td>
<td>GiOA[0]/INT[0]</td>
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</tr>
<tr>
<td>3</td>
<td>FLT1</td>
<td>FLT1</td>
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<tr>
<td>4</td>
<td>FLT2</td>
<td>FLT2</td>
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</tr>
<tr>
<td>6</td>
<td>VCCIO</td>
<td>VCCIO</td>
<td></td>
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<tr>
<td>7</td>
<td>VSS</td>
<td>VSS</td>
<td></td>
</tr>
<tr>
<td>Pin Number</td>
<td>Pin Name/Function</td>
<td>Pin Number</td>
<td>Pin Name/Function</td>
</tr>
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<td>------------</td>
<td>------------------</td>
<td>------------</td>
<td>------------------</td>
</tr>
<tr>
<td>11</td>
<td>N2HET[22]</td>
<td>15</td>
<td>N2HET[22]</td>
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<tr>
<td>13</td>
<td>VCC</td>
<td>17</td>
<td>VCC</td>
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<td>14</td>
<td>OSCIN</td>
<td>18</td>
<td>OSCIN</td>
</tr>
<tr>
<td>15</td>
<td>KELVIN_GND</td>
<td>19</td>
<td>KELVIN_GND</td>
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<tr>
<td>16</td>
<td>OSCOUT</td>
<td>20</td>
<td>OSCOUT</td>
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<tr>
<td>17</td>
<td>VSS</td>
<td>21</td>
<td>VSS</td>
</tr>
<tr>
<td>19</td>
<td>N2HET[0]</td>
<td>25</td>
<td>N2HET[0]</td>
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<td>VSS</td>
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<td>21</td>
<td>VCC</td>
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<td>VCC</td>
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<td>23</td>
<td>SPI2nCS[0]</td>
<td>32</td>
<td>MibSPI5nCS[0]</td>
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<td>24</td>
<td>TEST</td>
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<td>TEST</td>
</tr>
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<td>27</td>
<td>MibSPI1nCS[2]</td>
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<td>28</td>
<td>VCCIO</td>
<td>42</td>
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<td>VCC</td>
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<td>34</td>
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<td>SPI3SIMO</td>
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<td>SPI3CLK</td>
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<td>MibSPI3CLK</td>
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<td>37</td>
<td>SPI3nENA</td>
<td>54</td>
<td>MibSPI3nENA</td>
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## Table 2. Functional Pin Compatibility Mapping (continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name/Function</th>
<th>RM48x and RM46x Pin Number</th>
<th>Pin Name/Function</th>
<th>Comments</th>
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</thead>
<tbody>
<tr>
<td>38</td>
<td>SPI3nCS[0]</td>
<td>55</td>
<td>MibSPI3nCS[0]</td>
<td>Subset is limited to standard/non-buffered mode</td>
</tr>
<tr>
<td>39</td>
<td>MibSPI1nCS[3]</td>
<td>3</td>
<td>MibSPI1nCS[3]</td>
<td>The directly compatible pin for MibSPI1nCS[3] is located on a different side of the 144QFP superset than on the 100QFP subset. This may require some additional board layout consideration when updating the superset/144QFP board design to accommodate the subset/100QFP.</td>
</tr>
<tr>
<td>40</td>
<td>ADIN[16]</td>
<td>58</td>
<td>AD1IN[16]</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>ADIN[17]</td>
<td>59</td>
<td>AD1IN[17]</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>ADIN[0]</td>
<td>60</td>
<td>ADIN[0]</td>
<td></td>
</tr>
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<td>44</td>
<td>ADIN[20]</td>
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</tr>
<tr>
<td>45</td>
<td>ADIN[21]</td>
<td>65</td>
<td>AD1IN[21]</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>VCCAD/ADREFHI</td>
<td>66</td>
<td>ADREFHI</td>
<td>VCCAD and REFHI are combined on the subset package. REFHI limited to a range of 3-3.6V</td>
</tr>
<tr>
<td>47</td>
<td>VSSAD/ADREFLO</td>
<td>67</td>
<td>ADREFHI</td>
<td>VSSAD and REFLO are combined on the subset package. REFLO limited to GND.</td>
</tr>
<tr>
<td>48</td>
<td>ADIN[9]</td>
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<td>50</td>
<td>ADIN[10]</td>
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<td>AD1IN[10]</td>
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<td>52</td>
<td>ADIN[3]</td>
<td>74</td>
<td>AD1IN[3]</td>
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<tr>
<td>57</td>
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<td>83</td>
<td>AD1IN[8]</td>
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<tr>
<td>58</td>
<td>ADEVT</td>
<td>86</td>
<td>ADEVT</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>VSS</td>
<td>88</td>
<td>88</td>
<td>This subset pin has no direct matching pin in the 144QFE but can be connected directly to the common ground for the MCU.</td>
</tr>
<tr>
<td>60</td>
<td>VCCIO</td>
<td>-</td>
<td>-</td>
<td>This subset pin has no direct matching pin in the 144QFE but can be connected directly to the common 3.3V rail for the MCU.</td>
</tr>
<tr>
<td>61</td>
<td>VCC</td>
<td>87</td>
<td>VCC</td>
<td>Connection to this pin involves additional trace routing to prevent crossing traces.</td>
</tr>
</tbody>
</table>
**Table 2. Functional Pin Compatibility Mapping (continued)**

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name/Function</th>
<th>Pin Number</th>
<th>Pin Name/Function</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>62</td>
<td>CAN1TX</td>
<td>63</td>
<td>CAN1RX</td>
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</tr>
<tr>
<td>64</td>
<td>N2HET[24]</td>
<td>65</td>
<td>MibSPI1SIMO</td>
<td></td>
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<tr>
<td>66</td>
<td>MibSPI1SOMI</td>
<td>67</td>
<td>MibSPI1CLK</td>
<td></td>
</tr>
<tr>
<td>68</td>
<td>MibSPI1nENA</td>
<td>69</td>
<td>SPI2SOMI</td>
<td></td>
</tr>
<tr>
<td>70</td>
<td>SPI2SIMO</td>
<td>71</td>
<td>SPI2CLK</td>
<td>There is no SPI2 or MibSPI2 available in the 144QFP superset package; therefore the subset pins map to the MibSPI5 functionally equivalent pins. The SPI2 module on the subset device is limited to non-buffered 4-pin mode only.</td>
</tr>
<tr>
<td>72</td>
<td>VSS</td>
<td>73</td>
<td>MibSPI1nCS[0]</td>
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<td>TDO</td>
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<td>TCK</td>
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<td>RTCK</td>
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<td>82</td>
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<td>N2HET[10]</td>
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<td>94</td>
<td>LINRX (UARTRX)</td>
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<tr>
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</tbody>
</table>
4 Input/Output Considerations

There are some drive strength differences for output signals between the RM42x series vs the RM48x and RM46x series of microcontrollers. These are listed in Table 3.

Table 3. Output Drive-Strength Differences Between RM42x vs RM48x and RM46x

<table>
<thead>
<tr>
<th>Output Signal Name RM42x</th>
<th>Drive Strength on RM42x</th>
<th>Output Signal Name RM48x and RM46x</th>
<th>Drive Strength on RM48x and RM46x</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPI2CLK</td>
<td>2 mA/8 mA Selectable (8mA default)</td>
<td>MibSPI5CLK</td>
<td>8 mA</td>
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<td>SPI2SIMO</td>
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<td>MibSPI5SIMO</td>
<td>8 mA</td>
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<tr>
<td>SPI2SOMI</td>
<td>2 mA/8 mA Selectable (8mA default)</td>
<td>MibSPI5SOMI</td>
<td>8 mA</td>
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5 Module Compatibility Considerations

The RM42x series of microcontrollers are a subset of the features/functionality available on the RM46x and RM48x series of microcontrollers. As such, the majority of the software written for the superset devices, RM46x and RM48x, will be compatible with the RM42x series of microcontrollers. However, in some cases, features that are utilized in the superset devices will need to be considered either during development of the software or during the porting process to the subset device. In addition, the RM42x series of microcontrollers has similar enhancements to key peripherals as the RM46x series of microcontrollers. Some key feature differences and brief description of the peripheral enhancements are listed below.

5.1 Feature Differences on RM42x Series

The RM42x series of microcontrollers is a subset of the RM48x and RM46x series of microcontrollers. Some features are not included as a result of the simpler implementation.

5.1.1 Feature Implementation Differences for the RM42x Series

- Floating Point support
  The RM42x series of microcontrollers do not support floating point operation (R4 vs R4F).
- Flash EEPROM emulation bank
  The module IP used for the Flash EEPROM emulation is new on the RM42x series. This new bank is a 72-bit wide bank with slower access times than the bank used on super set series. The EWAIT parameter within the Flash Wrapper register set will need to be programmed according to the waitstates defines in the datasheet for RM42x series of microcontrollers.
- Pin muxing/IOMM configuration
  During development, the definition of the pin muxing control registers in the IOMM module required significant deviation from the pin muxing implemented on the super set series of devices. As a result, the PINMMR register assignments are unique to the RM42x series although there are some common muxed pin functions that are achievable.
- CPU BIST/STC implementation
  For the RM42x series of microcontrollers, the number of STC intervals is greater than the implementation on the superset devices. The total number of intervals to achieve maximum CPU BIST testing on the RM42x series is 26 vs 24 intervals on the superset devices. However, it is worth noting, that coverage >90% is achieved using only the 24 defined for the supersets.
- Time Base feature in the RTI module
  The Time Base feature is a feature that is primarily included on devices with FlexRay IP in order to synchronize timing between FlexRay network and the devices RTI counters. Given FlexRay is not included in the RM42x series, this feature is not implemented.
• IF3 Interrupt for DCAN1 and DCAN2
  The IF3 interrupt is used, primarily, in conjunction with the DMA controller to notify when a DMA
  transfer of an updated message can occur. Given the DMA module is not implemented in the RM42x
  series, this feature is not implemented.

• Full Auto and Semi-CPU modes within the CRC module
  The Full Auto and Semi-CPU modes of the CRC peripheral require the DMA controller. Given that
  DMA is not implemented in the RM42x series, these features are not supported in this series. Full CPU
  mode with the bus “snooper” feature are supported as described in the Technical Reference Manual.

• 5V ADC capability
  The ADC as implemented in the RM42x series, does not support 5V operation. The maximum ADC
  input is specified as 3.6V for this series of microcontrollers.

• ADREFHI/LO limitation
  In order to maximize the pin utilization in the 100pin QFP used for the RM42x series, the ADC supply
  pins were combined with the reference pins. This limits the ADREFHI to 3-3.6V and ADREFLO to
  VSSAD/GND.

• DMA transfers to/from peripheral RAMs
  As previously noted, the RM42x series of microcontrollers do not have a DMA controller. This means
  that accesses to/from the peripheral RAMS, must be made through the CPU with the exception of
  transfers to N2HET which can be made using the HTU module.

5.2 Module Enhancements on RM46x and RM42x Series
The RM46x and RM42x series of microcontrollers implements enhancements to two peripherals: the high-
end timer (N2HET) and the multi-buffered analog-to-digital converter (ADC).

5.2.1 N2HET Enhancements on RM46x and RM42x Series
• Selectable Hardware Angle Generator (HWAG) Toothed-Wheel Input
  The N2HET modules, on all of the series of microcontrollers, the RM48x, RM46x as well as the RM42x
  series of microcontrollers, supports an embedded HWAG. The function of the HWAG is to generate an
  angle value from a toothed-wheel input. This toothed-wheel input to the N2HET came from the
  N2HET[2] channel. This allocation was fixed and could not be programmed by the application on the
  RM448x series of microcontrollers. The HWAG on the RM46x and RM42x series now includes a
  programmable register that allows the application to select the N2HET channel that is used to provide
  the toothed-wheel input. This register still defaults to using N2HET[2] as the toothed-wheel input,
  thereby, maintaining backwards compatibility to the N2HET peripheral on RM48x.

• Input Capture Enhancements
  The N2HET input capture functionality is also enhanced on the RM46x and RM42x series of
  microcontrollers compared to the RM448x series. On the RM448x series, the input signal on an N2HET
  channel must follow these two rules:
  – The input signal period must be at least twice the N2HET loop-resolution-clock period, and
  – Each phase of the input signal must be at least one N2HET loop-resolution-clock period
  On the RM46x and RM42x series, the input signal on an N2HET channel must follow these two rules:
  – The input signal period must be at least one N2HET loop-resolution-clock period, and
  – Each phase of the input signal must be at least twice the N2HET high-resolution-clock period
  As can be seen, the N2HET on the RM46x and RM42x can be used to measure input pulse widths
  smaller than one loop-resolution-clock period.
5.2.2 ADC Enhancements on the RM46x and RM42x Series

- Enhanced Channel Selection Mode
  The ADC module on the RM48x series performs sequential conversions on the number of channels selected in any particular conversion group (event group, group1 or group2). This conversion starts with the lowest numbered channel selected and proceeds in ascending order until all selected channels have been converted. The RM46x and RM42x series introduces an enhanced channel selection mode, wherein, a look-up table is used to define the channel number to be converted. This provides the application the capability of repeatedly sampling the same analog input channel, or to define an arbitrary channel conversion sequence, or to switch the conversion sequence while conversions are already ongoing. For more details, see the ADC chapter of the RM46 16/32-Bit RISC Flash Microcontroller Technical Reference Manual (SPNU514) or the RM42x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual (SPNU516).

- RM46x also adds Support for External Analog Multiplexors
  The look-up table used to support the enhanced channel selection mode also allows the application to output external channel select and enable signals. These signals can then be connected to external analog multiplexors, thereby, increasing the number of analog input channels that can be converted by the ADC. The RM46x series supports connecting up to 4:1 external analog multiplexor on each of the 24 unique ADC input channels, effectively providing the ability to convert up to 96 input channels. This feature is not available on the RM42x series of microcontrollers.

5.3 RM42x Compatibility With the New Modules on the RM46x Series

The RM46x series introduces three new enhanced timing peripherals (eTPWM, eCAP and eQEP). The RM42x series of microcontrollers shares content for one of these modules (eQEP). In the RM42x series, as in the RM46x series, the terminals for this peripheral are multiplexed with existing functions and require additional configuration of the I/O multiplexing module to enable outputs. The multiplexing configuration and terminals that are associated with this peripheral are not implemented on common pins and will require adjustments in the PCB layout to accommodate the difference.

- Enhanced Quadrature Encoded Pulse Generator (eQEP)
  There is one eQEP module implemented on the RM42x series versus two on the RM46x series. The eQEP module uses a 32-bit position counter, supports low-speed measurement using the capture unit and high-speed measurement using a 32-bit unit timer. This module has a watchdog timer to detect motor stall and input error detection logic to identify simultaneous edge transition in QEP signals. In addition, There are several register configuration options within the PINMMR registers to configure input filtering and error notification routing. Since the RM42x series does not include the eCAP and eTPWM modules, the implementation of eQEP is done in a way that assumes N2HET use as a replacement for the functions associated with these enhanced timing modules.

6 References

- RM42x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual (SPNU516)
# Revision History

## Changes from Original (December 2012) to A Revision

<table>
<thead>
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<td>• Made updates to Table 2</td>
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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
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